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August 1989
Revised August 2000

100336
Low Power 4-Stage Counter/Shift Register

General Description

The 100336 operates as either a modulo-16 up/down counter or as a 4-bit bidirectional shift register. Three Select (S_n) inputs determine the mode of operation, as shown in the Function Select table. Two Count Enable ($\overline{CEP}$, $\overline{CET}$) inputs are provided for ease of cascading in multistage counters. One Count Enable ($\overline{CET}$) input also doubles as a Serial Data (D_0) input for shift-up operation. For shift-down operation, D_3 is the Serial Data input. In counting operations the Terminal Count ($\overline{TC}$) output goes LOW when the counter reaches 15 in the count/up mode or 0 (zero) in the count/down mode. In the shift modes, the $\overline{TC}$ output repeats the Q_3 output. The dual nature of this $\overline{TC}/Q_3$ output and the $D_0/\overline{CET}$ input means that one interconnection from one stage to the next higher stage serves as the link for multistage counting or shift-up operation. The individual Preset (P_n) inputs are used to enter data in parallel or to preset the counter in programmable counter applications. A HIGH signal on the Master Reset (MR) input overrides all other inputs and asynchronously clears the flip-flops. In addition, a synchronous clear is provided, as well as a complement function which synchronously inverts the contents of the flip-flops. All inputs have 50 kΩ pull-down resistors.

Features

- 40% power reduction of the 100136
- 2000V ESD protection
- Pin/function compatible with 100136
- Voltage compensated operating range = –4.2V to –5.7V
- Available to industrial grade temperature range

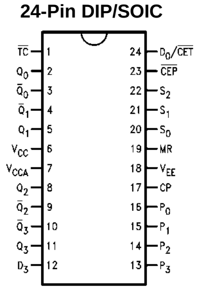
Ordering Code:

Order Number	Package Number	Package Description
100336SC	M24B	24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
100336PC	N24E	24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-010, 0.400 Wide
100336QC	V28A	28-Lead Plastic Lead Chip Carrier (PLCC), JEDEC MO-047, 0.450 Square
100336QI	V28A	28-Lead Plastic Lead Chip Carrier (PLCC), JEDEC MO-047, 0.450 Square Industrial Temperature Range (–40°C to +85°C)

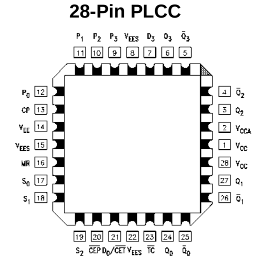
Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagrams

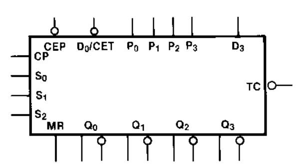
24-Pin DIP/SOIC



28-Pin PLCC



Logic Symbol



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Function Select Table

S_2	S_1	S_0	Function
L	L	L	Parallel Load
L	L	H	Complement
L	H	L	Shift Left
L	H	H	Shift Right
H	L	L	Count Down
H	L	H	Clear
H	H	L	Count Up
H	H	H	Hold

Pin Descriptions

Pin Names	Description
CP	Clock Pulse Input
$\overline{CEP}$	Count Enable Parallel Input (Active LOW)
$D_0/\overline{CET}$	Serial Data Input/Count Enable Trickle Input (Active LOW)
S_0–S_2	Select Inputs
MR	Master Reset Input
P_0–P_3	Preset Inputs
D_3	Serial Data Input
$\overline{TC}$	Terminal Count Output
Q_0–Q_3	Data Outputs
$\overline{Q_0}$–$\overline{Q_3}$	Complementary Data Outputs

Truth Table

Q_0 = LSB

Inputs								Outputs					
MR	S_2	S_1	S_0	$\overline{CEP}$	$D_0/\overline{CET}$	D_3	CP	Q_3	Q_2	Q_1	Q_0	$\overline{TC}$	Mode
L	L	L	L	X	X	X	↗	P_3	P_2	P_1	P_0	L	Preset (Parallel Load)
L	L	L	H	X	X	X	↗	$\overline{Q_3}$	$\overline{Q_2}$	$\overline{Q_1}$	$\overline{Q_0}$	L	Invert
L	L	H	L	X	X	X	↗	D_3	Q_3	Q_2	Q_1	D_3	Shift to LSB
L	L	H	H	X	X	X	↗	Q_2	Q_1	Q_0	D_0	Q_3 (Note 1)	Shift to MSB
L	H	L	L	L	L	X	↗	(Q_{0-3}) minus 1				1	Count Down
L	H	L	L	H	L	X	X	Q_3	Q_2	Q_1	Q_0	1	Count Down with $\overline{CEP}$ not active
L	H	L	L	X	H	X	X	Q_3	Q_2	Q_1	Q_0	H	Count Down with $\overline{CET}$ not active
L	H	L	H	X	X	X	↗	L	L	L	L	H	Clear
L	H	H	L	L	L	X	↗	(Q_{0-3}) plus 1				2	Count Up
L	H	H	L	H	L	X	X	Q_3	Q_2	Q_1	Q_0	2	Count Up with $\overline{CEP}$ not active
L	H	H	L	X	H	X	X	Q_3	Q_2	Q_1	Q_0	H	Count Up with $\overline{CET}$ not active
L	H	H	H	X	X	X	X	Q_3	Q_2	Q_1	Q_0	H	Hold
H	L	L	L	X	X	X	X	L	L	L	L	L	
H	L	L	H	X	X	X	X	L	L	L	L	L	
H	L	H	L	X	X	X	X	L	L	L	L	L	
H	L	H	H	X	X	X	X	L	L	L	L	L	Asynchronous
H	H	L	L	X	L	X	X	L	L	L	L	L	Master Reset
H	H	L	L	X	H	X	X	L	L	L	L	H	
H	H	L	H	X	X	X	X	L	L	L	L	H	
H	H	H	L	X	X	X	X	L	L	L	L	H	
H	H	H	H	X	X	X	X	L	L	L	L	H	

1 = L if Q_0–Q_3 = LLLL
H if Q_0–Q_3 ≠ LLLL
2 = L if Q_0–Q_3 = HHHH
H if Q_0–Q_3 ≠ HHHH
H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
↗ = LOW-to-HIGH Transition

Note 1: Before the clock, $\overline{TC}$ is Q_3

After the clock, $\overline{TC}$ is Q_2

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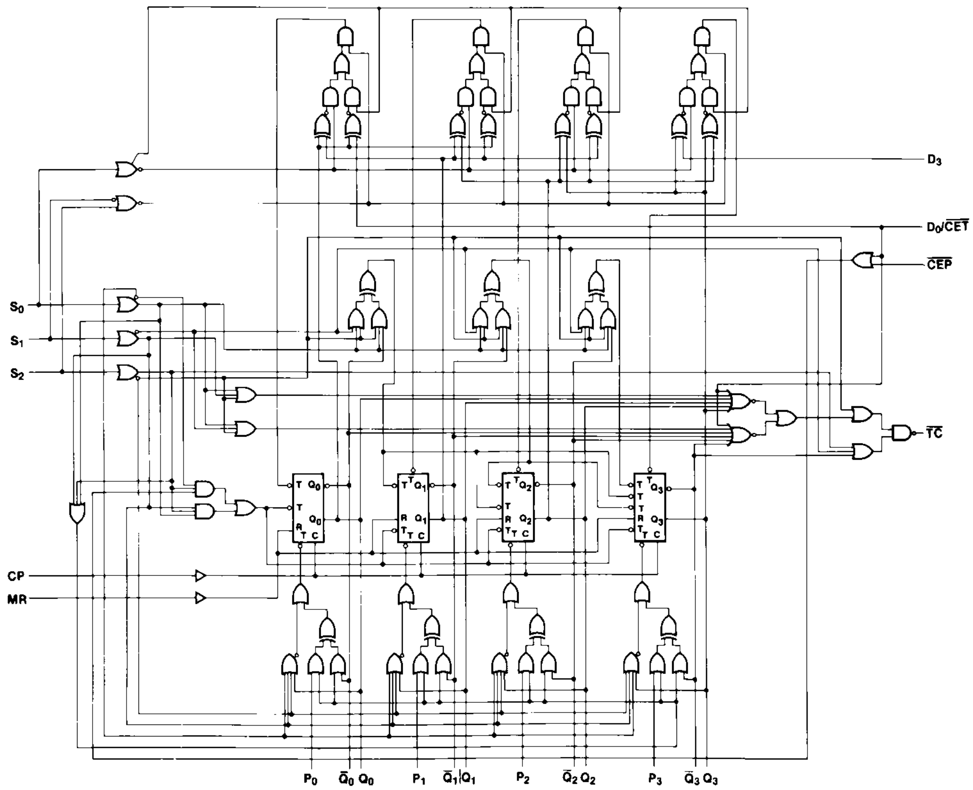
Logic Diagram



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Absolute Maximum Ratings (Note 2)

Storage Temperature (T_{STG})	−65°C to +150°C
Maximum Junction Temperature (T_J)	+150°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−50 mA
ESD (Note 3)	≥ 2000V

Recommended Operating Conditions

Case Temperature (T_C)	
Commercial	0°C to +85°C
Industrial	−40°C to +85°C
Supply Voltage (V_{EE})	−5.7V to −4.2V

Note 2: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 3: ESD testing conforms to MIL-STD-883, Method 3015.

Commercial Version

DC Electrical Characteristics (Note 4)

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C

Symbol	Parameter	Min	Typ	Max	Units	Conditions	
V_{OH}	Output HIGH Voltage	−1025	−955	−870	mV	V_{IN} = $V_{IH (Max)}$	Loading with
V_{OL}	Output LOW Voltage	−1830	−1705	−1620	mV	or $V_{IL (Min)}$	50Ω to −2.0V
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = $V_{IH(Min)}$	Loading with
V_{OLC}	Output LOW Voltage			−1610	mV	or $V_{IL (Max)}$	50Ω to −2.0V
V_{IH}	Input HIGH Voltage	−1165		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = V_{IL} (Min)	
I_{IH}	Input HIGH Current			240	μA	V_{IN} = V_{IH} (Max)	
I_{EE}	Power Supply Current	−165		−80		Inputs Open	

Note 4: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

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Commercial Version (Continued)
DIP AC Characteristics

V_{EE} = –4.2V to –5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
f_{SHIFT}	Shift Frequency	300		300		300		MHz	Figures 2, 3
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n, $\overline{Q}_n$	1.00	2.00	1.00	2.00	1.00	2.00	ns	Figures 1, 3 (Note 5)
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{TC}$ (Shift)	2.10	3.50	2.10	3.50	2.10	3.70	ns	Figures 1, 7, 8 (Note 5)
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{TC}$ (Count)	2.40	4.40	2.40	4.40	2.60	4.70	ns	Figures 1, 9 (Note 5)
t_{PLH} t_{PHL}	Propagation Delay MR to Q_n, $\overline{Q}_n$	1.40	2.50	1.40	2.50	1.50	2.60	ns	Figures 1, 4 (Note 5)
t_{PLH} t_{PHL}	Propagation Delay MR to $\overline{TC}$ (Count)	2.80	5.10	2.90	5.20	3.10	5.50	ns	Figures 1, 12 (Note 5)
t_{PHL}	Propagation Delay MR to $\overline{TC}$ (Shift)	2.40	4.00	2.40	4.00	2.50	4.10	ns	Figures 1, 10, 11 (Note 5)
t_{PLH} t_{PHL}	Propagation Delay $D_0/\overline{CET}$ to $\overline{TC}$	1.80	3.10	1.80	3.10	1.90	3.30	ns	Figures 1, 5 (Note 5)
t_{PLH} t_{PHL}	Propagation Delay S_n to $\overline{TC}$	1.90	4.10	1.90	4.10	2.10	4.40	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.35	1.20	0.35	1.20	0.35	1.20	ns	Figures 1, 3
t_S	Setup Time							ns	Figures 6, 4
	D_3	1.00		1.00		1.00			
	P_n	1.50		1.50		1.50			
	$D_0/\overline{CET}$	1.30		1.30		1.30			
	$\overline{CEP}$	1.40		1.40		1.40			
	S_n	3.40		3.40		3.40			
	MR (Release Time)	2.60		2.60		2.60			
t_H	Hold Time							ns	Figure 6
	D_3	0.40		0.40		0.40			
	P_n	0.30		0.30		0.30			
	$D_0/\overline{CET}$	0.30		0.30		0.30			
	$\overline{CEP}$	0.20		0.20		0.20			
	S_n	0.10		0.10		0.10			
t_{PW}(H)	Pulse Width HIGH CP, MR	2.00		2.00		2.00		ns	Figures 3, 4

Note 5: The propagation delay specified is for single output switching. Delays may vary up to 250 ps with multiple outputs switching.

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SOIC and PLCC AC Electrical Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = 0°C$ Min	$T_C = 0°C$ Max	$T_C = +25°C$ Min	$T_C = +25°C$ Max	$T_C = +85°C$ Min	$T_C = +85°C$ Max	Units	Conditions
f_{SHIFT}	Shift Frequency	350		350		350		MHz	Figures 2, 3
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n, $\overline{Q}_n$	1.00	1.80	1.00	1.80	1.00	1.80	ns	Figures 1, 2 (Note 6)
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{TC}$ (Shift)	2.10	3.30	2.10	3.30	2.10	3.50	ns	Figures 1, 7, 8 (Note 6)
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{TC}$ (Count)	2.40	4.20	2.40	4.20	2.60	4.50	ns	Figures 1, 9 (Note 6)
t_{PLH} t_{PHL}	Propagation Delay MR to Q_n, $\overline{Q}_n$	1.40	2.30	1.40	2.30	1.50	2.40	ns	Figures 1, 4 (Note 6)
t_{PLH} t_{PHL}	Propagation Delay MR to $\overline{TC}$ (Count)	2.80	4.90	2.90	5.00	3.10	5.30	ns	Figures 1, 12 (Note 6)
t_{PHL}	Propagation Delay MR to $\overline{TC}$ (Shift)	2.40	3.80	2.40	3.80	2.50	3.90	ns	Figures 1, 10, 11 (Note 6)
t_{PLH} t_{PHL}	Propagation Delay $D_0/\overline{CET}$ to $\overline{TC}$	1.80	2.90	1.80	2.90	1.90	3.10	ns	Figures 1, 5 (Note 6)
t_{PLH} t_{PHL}	Propagation Delay S_n to $\overline{TC}$	1.90	3.90	1.90	3.90	2.10	4.20	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.35	1.10	0.35	1.10	0.35	1.10	ns	Figures 1, 3
t_S	Setup Time							ns	Figures 4, 6
	D_3	0.90		0.90		0.90			
	P_n	1.40		1.40		1.40			
	$D_0/\overline{CET}$	1.20		1.20		1.20			
	$\overline{CEP}$	1.30		1.30		1.30			
	S_n	3.30		3.30		3.30			
	MR (Release Time)	2.50		2.50		2.50			
t_H	Hold Time							ns	Figure 6
	D_3	0.30		0.30		0.30			
	P_n	0.20		0.20		0.20			
	$D_0/\overline{CET}$	0.20		0.20		0.20			
	$\overline{CEP}$	0.10		0.10		0.10			
	S_n	0.00		0.00		0.00			
$t_{PW}(H)$	Pulse Width HIGH CP, MR	2.00		2.00		2.00		ns	Figures 3, 4
t_{OSHL}	Maximum Skew Common Edge Output-to-Output Variation Clock to Output Path		200		200		200	ps	PLCC Only (Note 7)
t_{OSLH}	Maximum Skew Common Edge Output-to-Output Variation Clock to Output Path		200		200		200	ps	PLCC Only (Note 7)
t_{OST}	Maximum Skew Opposite Edge Output-to-Output Variation Clock to Output Path		230		230		230	ps	PLCC Only (Note 7)
t_{PS}	Maximum Skew Pin (Signal) Transition Variation Clock to Output Path		245		245		245	ps	PLCC Only (Note 7)

Note 6: The propagation delay specified is for single output switching. Delays may vary up to 250 ps with multiple outputs switching.

Note 7: Output-to-Output Skew is defined as the absolute value of the difference between the actual propagation delay for any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction either HIGH-to-LOW (t_{OSHL}), or LOW-to-HIGH (t_{OSLH}), or in opposite directions both HL and LH (t_{OST}). Parameters t_{OST} and t_{ps} guaranteed by design

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Industrial Version

PLCC DC Electrical Characteristics (Note 8)

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = −40°C to +85°C

Symbol	Parameter	T_C = −40°C		T_C = 0°C to +85°C		Units	Conditions	
		Min	Max	Min	Max			
V_{OH}	Output HIGH Voltage	−1085	−870	−1025	−870	mV	$V_{IN} = V_{IH (Max)}$	Loading with
V_{OL}	Output LOW Voltage	−1830	−1575	−1830	−1620	mV	or $V_{IL (Min)}$	50Ω to −2.0V
V_{OHC}	Output HIGH Voltage	−1095		−1035		mV	$V_{IN} = V_{IH(Min)}$	Loading with
V_{OLC}	Output LOW Voltage		−1565		−1610	mV	or $V_{IL (Max)}$	50Ω to −2.0V
V_{IH}	Input HIGH Voltage	−1170	−870	−1165	−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830	−1480	−1830	−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50		0.50		μA	$V_{IN} = V_{IL}$ (Min)	
I_{IH}	Input HIGH Current		240		240	μA	$V_{IN} = V_{IH}$ (Max)	
I_{EE}	Power Supply Current	−165	−75	−165	−80	mA	Inputs Open	

Note 8: The specified limits represent the “worst case” value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under “worst case” conditions.

PLCC AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = −40°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
f_{SHIFT}	Shift Frequency	325		350		350		MHz	Figures 2, 3
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n, $\overline{Q}_n$	1.00	1.80	1.00	1.80	1.00	1.80	ns	Figures 1, 3 (Note 9)
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{TC}$ (Shift)	2.00	3.30	2.10	3.30	2.10	3.50	ns	Figures 1, 7, 8 (Note 9)
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{TC}$ (Count)	2.40	4.20	2.40	4.20	2.60	4.50	ns	Figures 1, 9 (Note 9)
t_{PLH} t_{PHL}	Propagation Delay MR to Q_n, $\overline{Q}_n$	1.40	2.30	1.40	2.30	1.50	2.40	ns	Figures 1, 4 (Note 9)
t_{PLH} t_{PHL}	Propagation Delay MR to $\overline{TC}$ (Count)	2.80	4.90	2.90	5.00	3.10	5.30	ns	Figures 1, 12 (Note 9)
t_{PHL}	Propagation Delay MR to $\overline{TC}$ (Shift)	2.40	3.80	2.40	3.80	2.50	3.90	ns	Figures 1, 10, 11 (Note 9)
t_{PLH} t_{PHL}	Propagation Delay $D_0/\overline{CET}$ to $\overline{TC}$	1.70	2.90	1.80	2.90	1.90	3.10	ns	Figures 1, 5 (Note 9)
t_{PLH} t_{PHL}	Propagation Delay S_n to $\overline{TC}$	1.80	3.90	1.90	3.90	2.10	4.20	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.20	1.90	0.35	1.10	0.35	1.10	ns	Figures 1, 3
t_S	Setup Time D_3 P_n $D_0/\overline{CET}$ $\overline{CEP}$ S_n MR (Release Time)	 1.40 1.70 1.80 1.80 3.30 2.60		 0.90 1.40 1.20 1.30 3.30 2.50		 0.90 1.40 1.20 1.30 3.30 2.50		ns	Figure 6
t_H	Hold Time D_3 P_n $D_0/\overline{CET}$ $\overline{CEP}$ S_n	 0.90 1.00 0.70 0.60 0.00		 0.30 0.20 0.20 0.10 0.00		 0.30 0.20 0.20 0.10 0.00		ns	Figure 6
t_{PW}(H)	Pulse Width HIGH CP, MR	2.20		2.00		2.00		ns	Figures 3, 4

Note 9: The propagation delay specified is for single output switching. Delays may vary up to 250 ps with multiple outputs switching.

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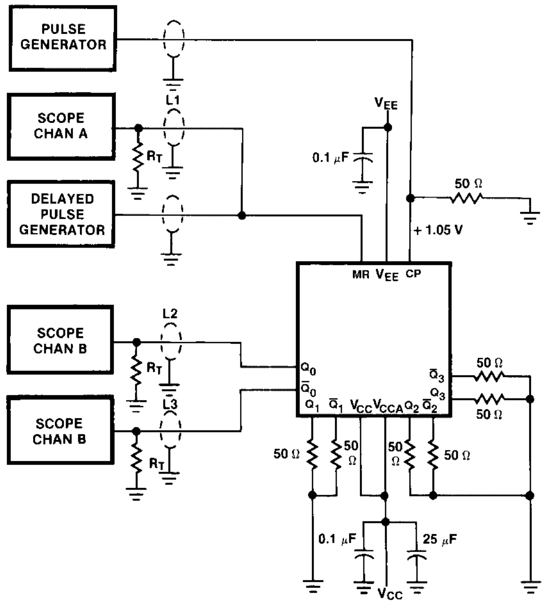
Test Circuitry



Notes:

V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V

L1, L2 and L3 = equal length 50Ω impedance lines

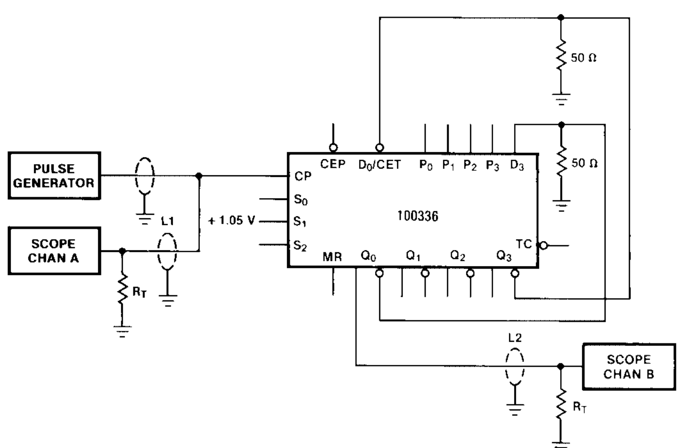
R_T = 50Ω terminator internal to scope

Decoupling 0.1 µF from GND to V_{CC} and V_{EE}

All unused outputs are loaded with 50Ω to GND

C_L = Fixture and stray capacitance ≤ 3 pF

FIGURE 1. AC Test Circuit



Notes:

For shift right mode, +1.05V is applied at S_0.

The feedback path from output to input should be as short as possible.

FIGURE 2. Shift Frequency Test Circuit (Shift Left)

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Switching Waveforms

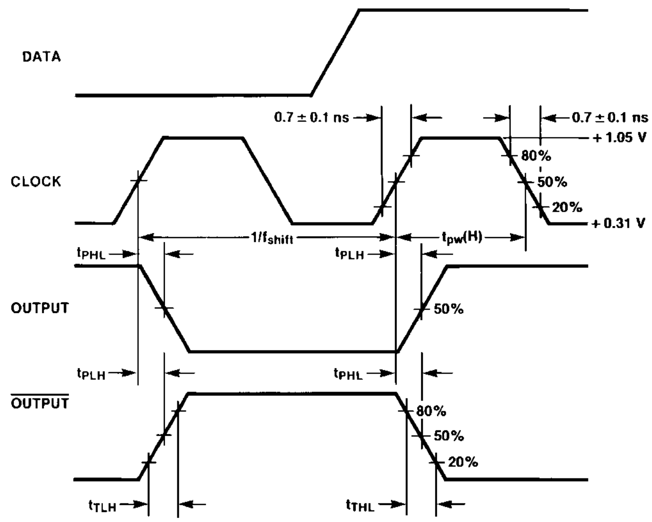

FIGURE 3. Propagation Delay (Clock) and Transition Times

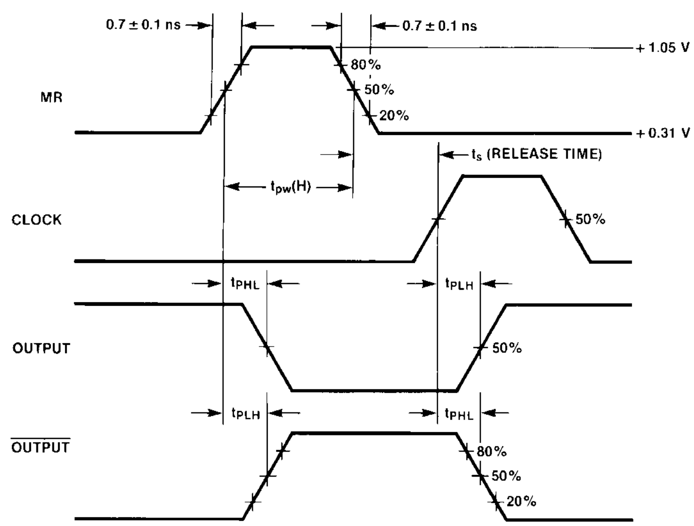

FIGURE 4. Propagation Delay (Reset)

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Switching Waveforms (Continued)

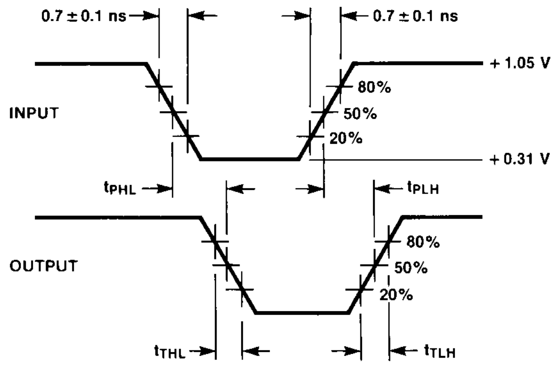
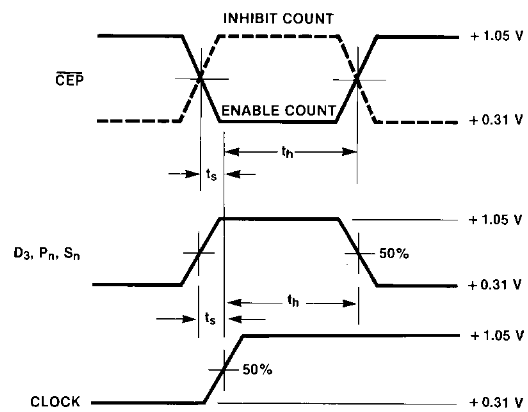


FIGURE 5. Propagation Delay (Serial Data, Selects)

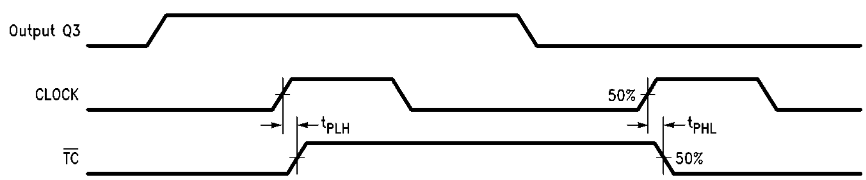


Notes:

t_S is the minimum time before the transition of the clock that information must be present at the data input.

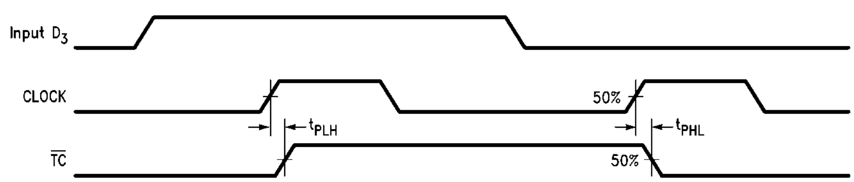
t_H is the minimum time after the transition of the clock that information must remain unchanged at the data input.

FIGURE 6. Setup and Hold Time



Note: Shift Right Mode; S_0 = H, S_1 = H, S_2 = L.

FIGURE 7. Propagation Delay, Clock to Terminal Count (Shift Right Mode)



Note: Shift Left Mode; S_0 = L, S_1 = H, S_2 = L.

FIGURE 8. Propagation Delay, Clock to Terminal Count (Shift Left Mode)

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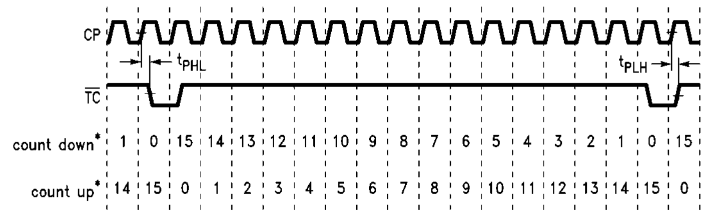
Switching Waveforms (Continued)



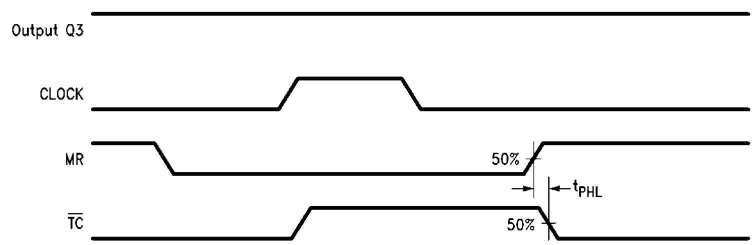
Note:

*Decimal representation of binary outputs.

Count Up: S_0 = L, S_1 = H, S_2 = H; Count Down: S_0 = L, S_1 = L, S_2 = H.

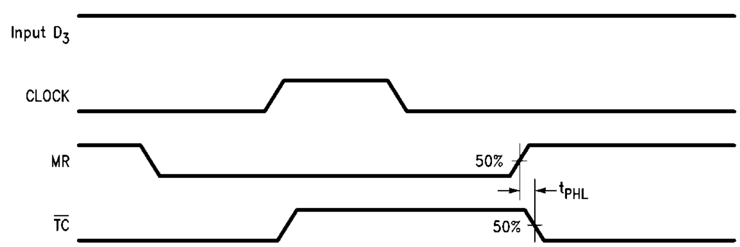
Measurement taken at 50% point of waveform.

FIGURE 9. Propagation Delay, Clock to Terminal Count (Count Up and Count Down Modes)



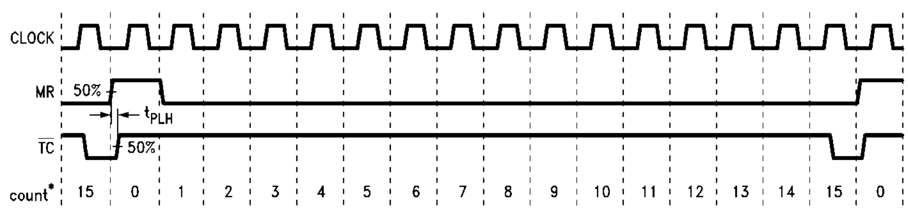
Note: Shift Right Mode; S_0 = H, S_1 = H, S_2 = L.

FIGURE 10. Propagation Delay, Master Reset to Terminal Count (Shift Right Mode)



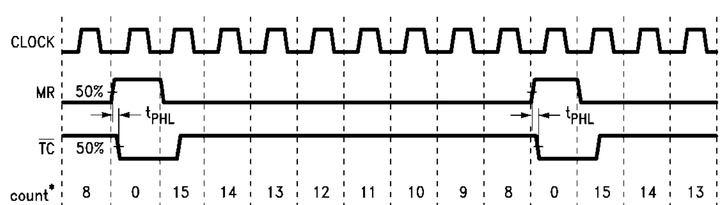
Note: Shift Left Mode; S_0 = L, S_1 = H, S_2 = L.

FIGURE 11. Propagation Delay, Master Reset to Terminal Count (Shift Left Mode)



Note:

*Decimal representation of binary outputs. Count Up Mode: S_0 = L, S_1 = H, S_2 = H.



Note:

*Decimal representation of binary outputs. Count Down Mode: S_0 = L, S_1 = L, S_2 = H.

FIGURE 12. Propagation Delay, Master Reset to Terminal Count (Count Up and Count Down Modes)

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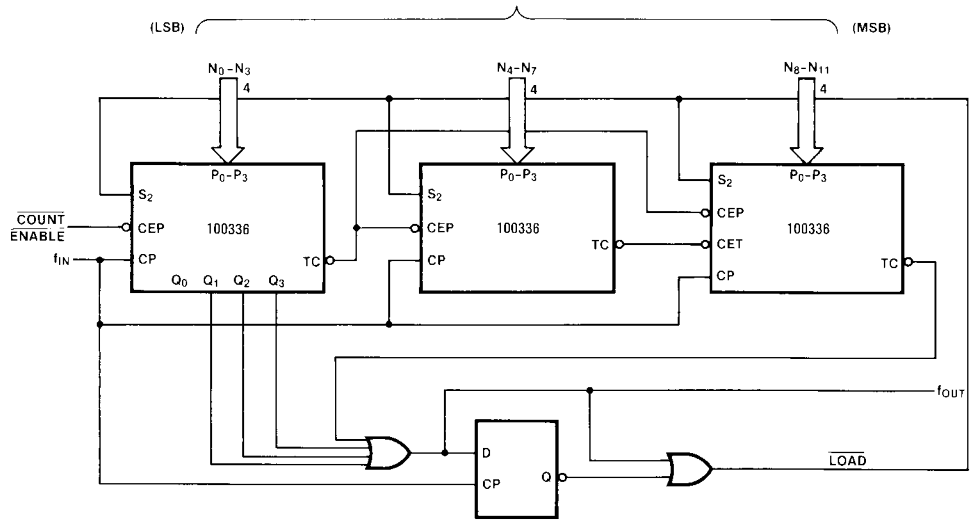
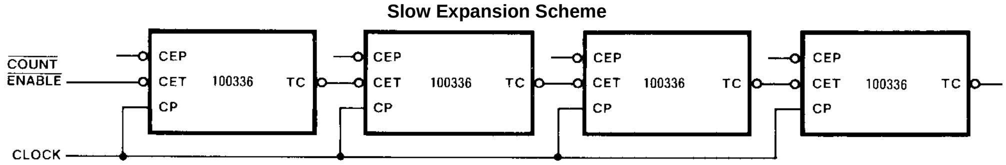
Applications

3-Stage Divider, Preset Count Down Mode

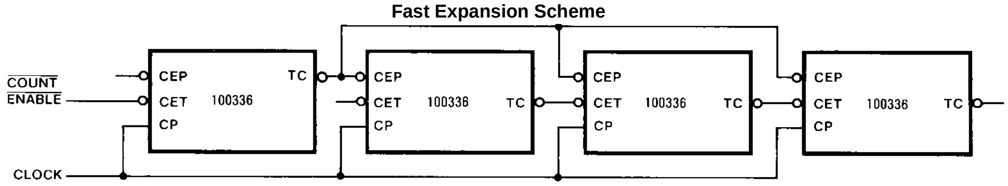


Note: If $S_0 = S_1 = S_2$ = LOW, then T_C = LOW

Slow Expansion Scheme



Fast Expansion Scheme



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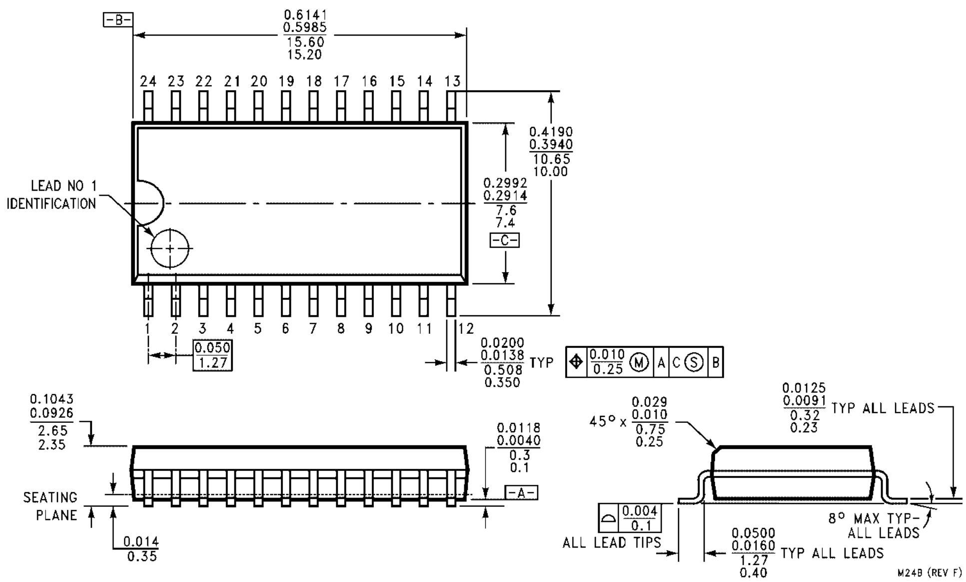
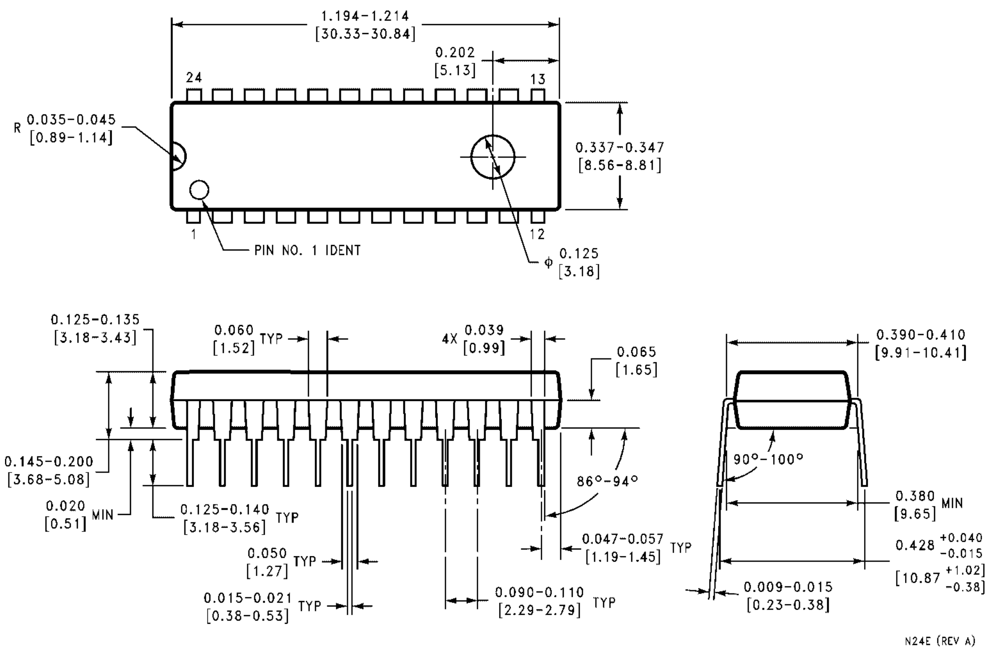
Physical Dimensions inches (millimeters) unless otherwise noted



24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
Package Number M24B



24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-010, 0.400 Wide
Package Number N24E

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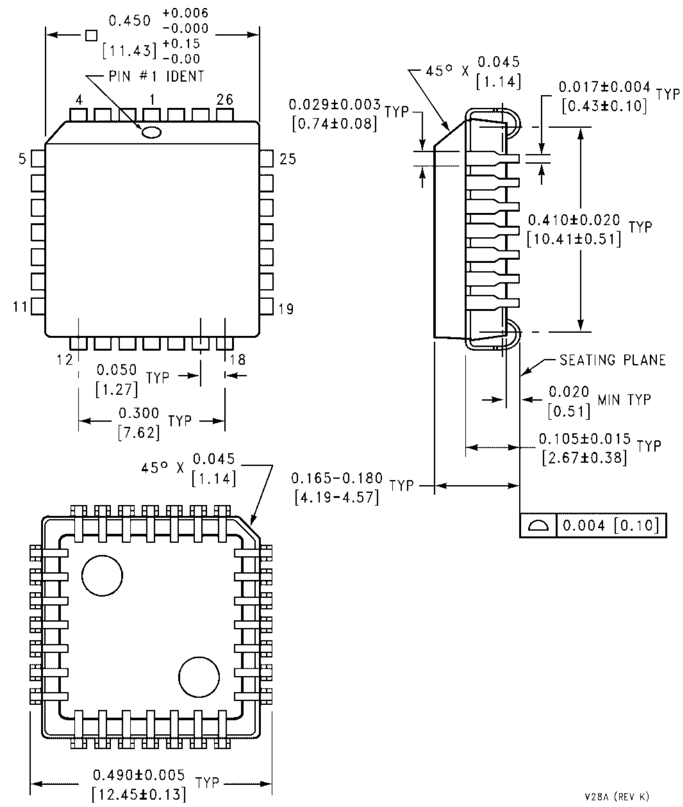
Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



28-Lead Plastic Lead Chip Carrier (PLCC), JEDEC MO-047, 0.450 Square
Package Number V28A

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