

## Low forward voltage Transil™, transient voltage suppressor

Datasheet – production data

### Features

- Strong ESD and EOS protection
- Very low clamping factor  $V_{CL}/V_{BR}$
- Unidirectional device
- Fast response time
- Very thin package
- Very small PCB area
- RoHS compliant

### Complies with the following standards:

- IEC 61000-4-2 level 4
  - ±15 kV (air discharge)
  - ±8 kV (contact discharge)

### Description

The LFTVS18-1F3 is a single line diode designed specifically for the protection of integrated circuits in portable equipment and miniaturized electronics devices subject to ESD and EOS transient overvoltages.

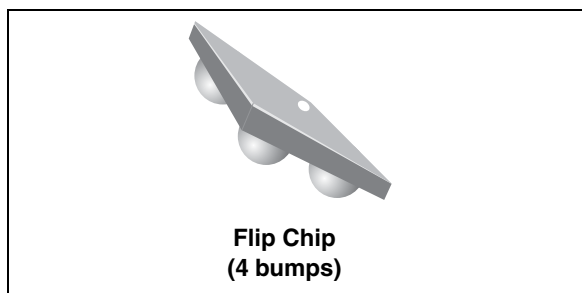


Figure 1. Pin configuration (bump side)

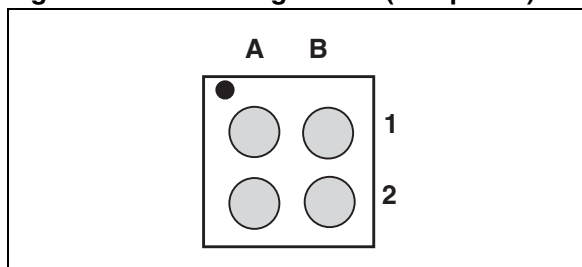
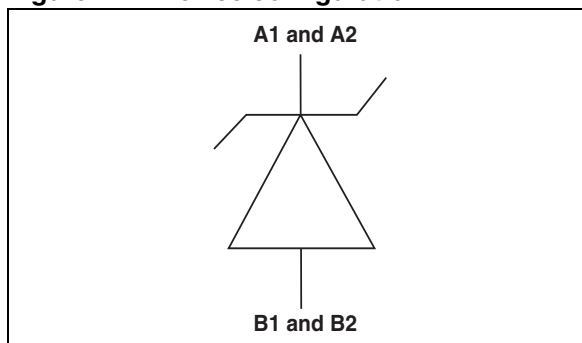


Figure 2. Device configuration



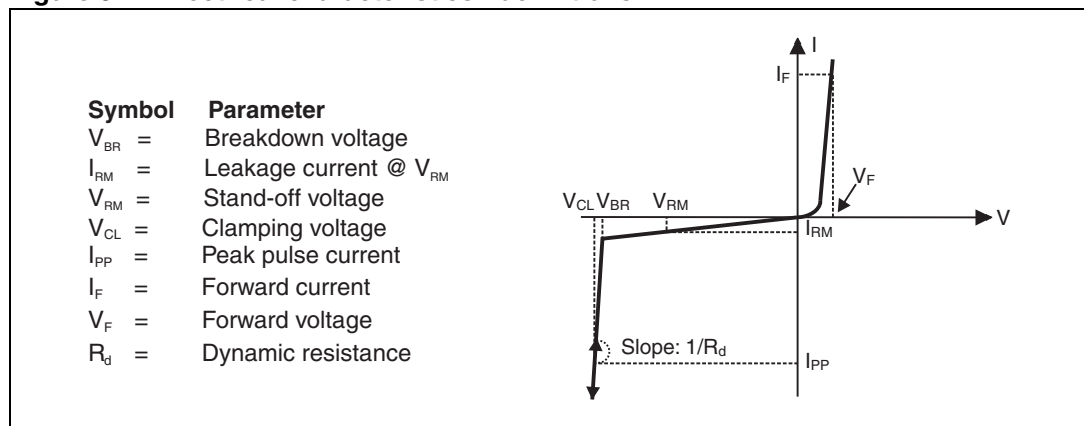
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# 1 Characteristics

**Table 1. Absolute maximum ratings ( $T_{amb} = 25\text{ }^{\circ}\text{C}$ )**

Symbol	Parameter	Test condition	Value	Unit
$P_{PP}$	Peak pulse power dissipation (8/20 $\mu\text{s}$ pulse)	$T_j$ initial = $T_{amb}$	350	W
$I_{FSM}$	Non repetitive surge peak forward current	$t_p = 10\text{ ms}$ , $T_j$ initial = $T_{amb}$	5	A
$T_j$	Maximum operating junction temperature		125	$^{\circ}\text{C}$
$T_{stg}$	Storage temperature range		-55 to +150	$^{\circ}\text{C}$

**Figure 3. Electrical characteristics - definitions**

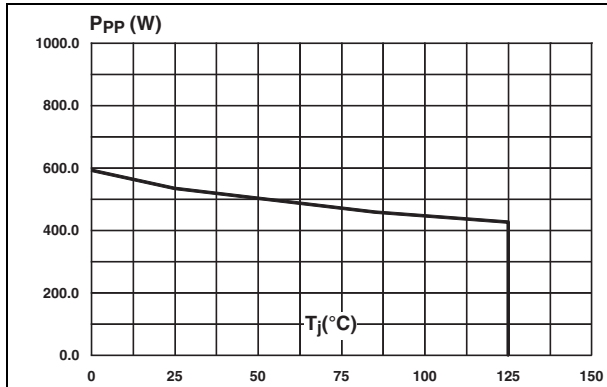


**Table 2. Electrical characteristics - values ( $T_{amb} = 25\text{ }^{\circ}\text{C}$ )**

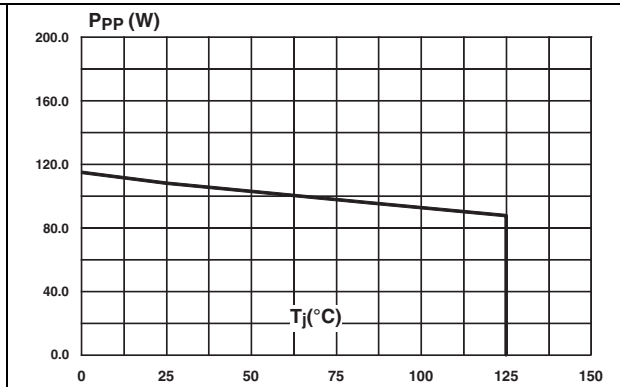
Symbol	Test conditions	Min.	Typ.	Max.	Unit
$V_{BR}$	$I_R = 1\text{ mA}$	16			V
$I_{RM}$	$V_{RM} = 12\text{ V}$			250	nA
$V_{CL}$	$I_{PP} = 1\text{ A}^{(1)}$			19	V
$V_F$	$I_F = 850\text{ mA}$			1.3	V
$C_{line}$	$V_R = 0\text{ V}$ , $V_{OSC} = 30\text{ mV}$ , $F = 1\text{ MHz}$		175		pF

1. 8 / 20  $\mu\text{s}$  pulse waveform

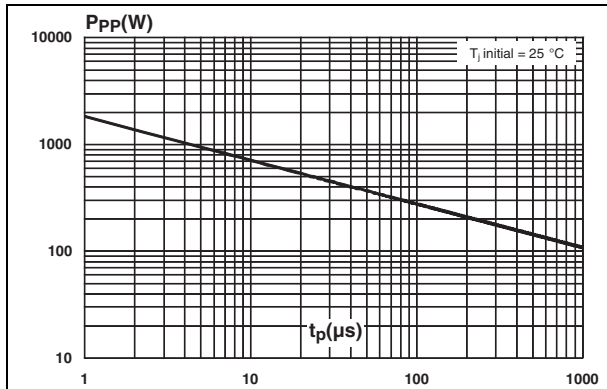
**Figure 4. Peak pulse power versus initial junction temperature (pulse 8/20  $\mu$ s)**



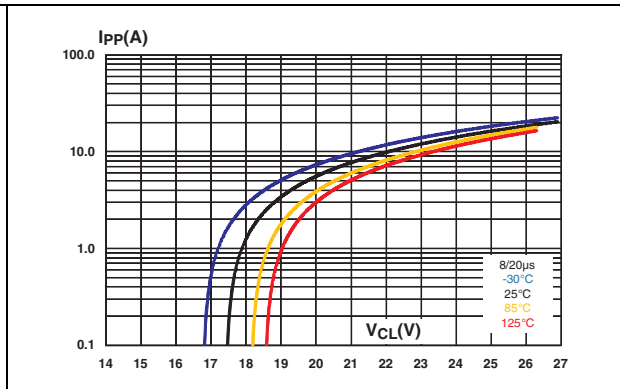
**Figure 5. Peak pulse power versus initial junction temperature (pulse 10/1000  $\mu$ s)**



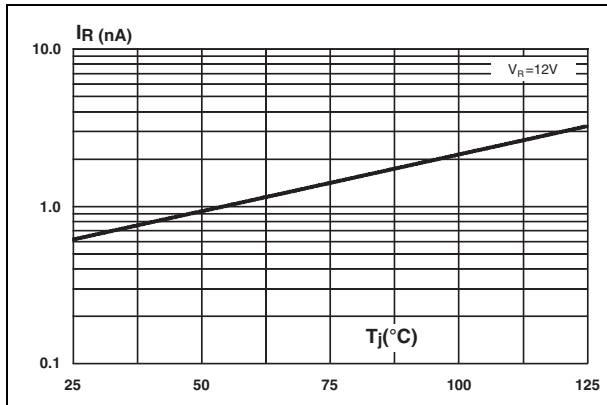
**Figure 6. Peak pulse power versus exponential pulse duration**



**Figure 7. Clamping voltage versus peak pulse current (8/20  $\mu$ s, typical values)**



**Figure 8. Leakage current versus junction temperature (typical values)**



**Figure 9. Forward voltage drop versus peak forward current (typical values)**

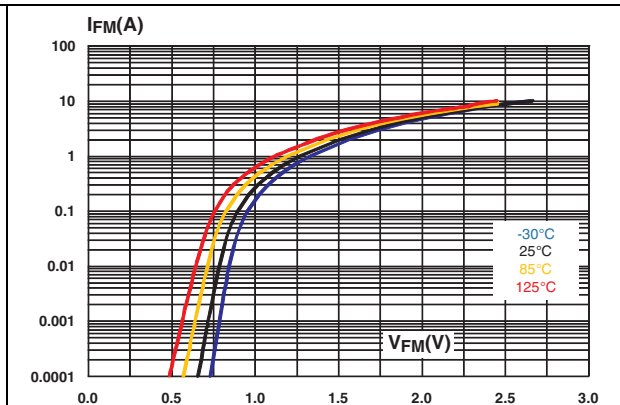


Figure 10. Junction capacitance versus line voltage (typical values)

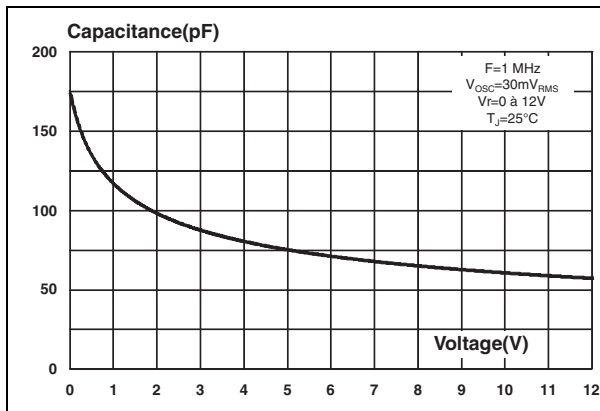


Figure 11. Junction capacitance versus frequency for different bias voltages (P = -12 dBm)

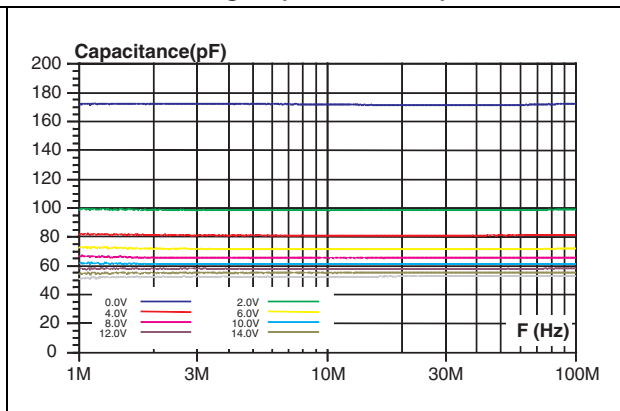


Figure 12. Breakdown voltage versus initial junction temperature (typical value)

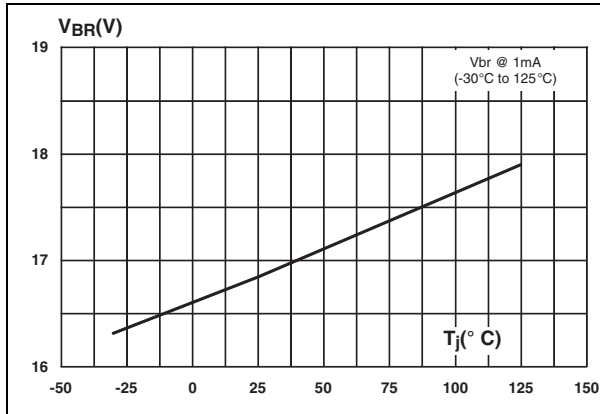


Figure 13. S21 insertion losses versus frequency response

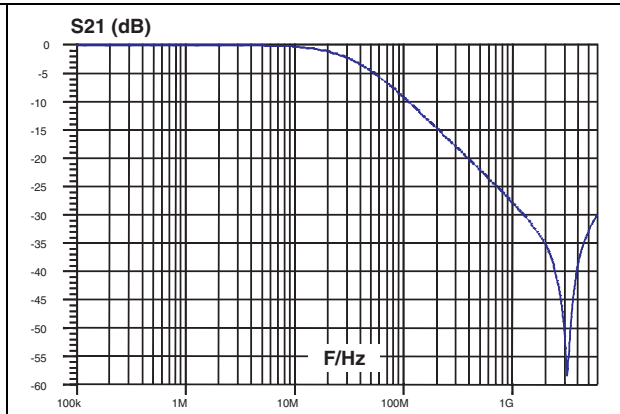


Figure 14. ESD response to IEC 61000-4-2 (+8 kV contact discharge)

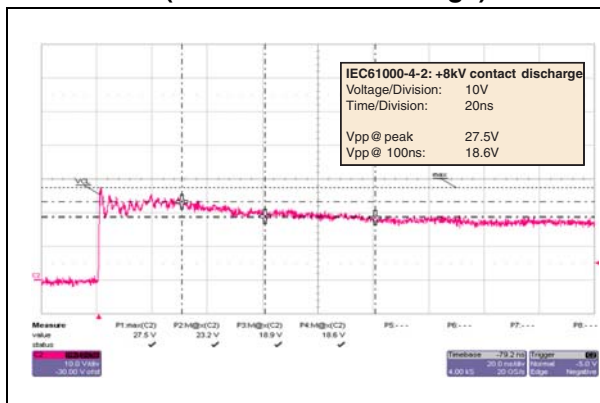
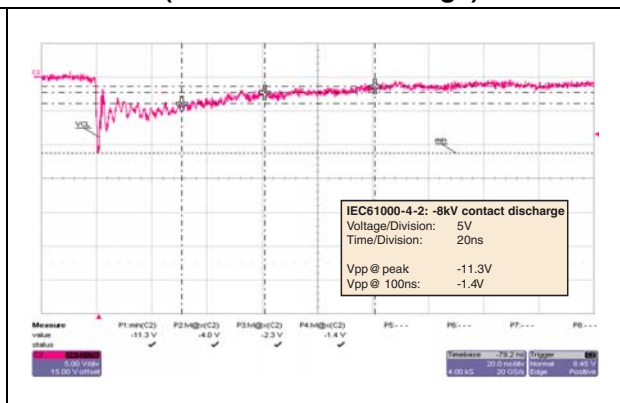
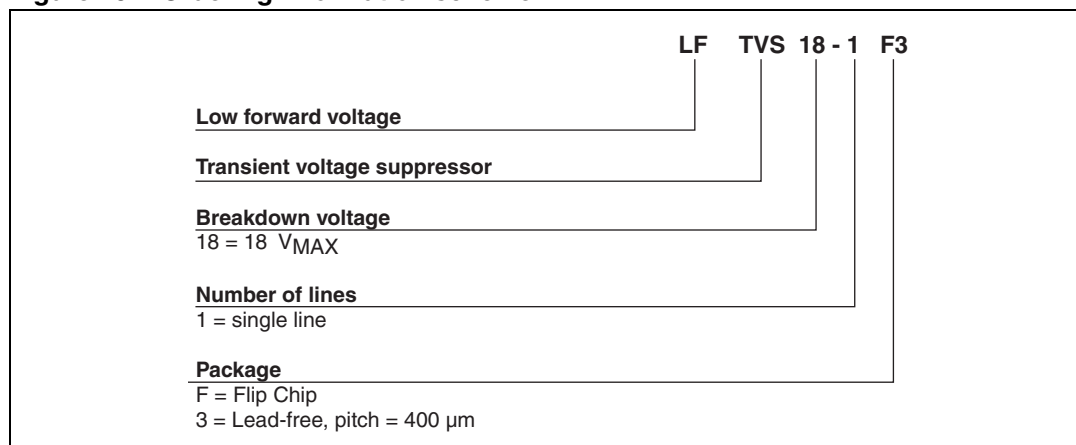


Figure 15. ESD response to IEC 61000-4-2 (-8 kV contact discharge)



## 2 Ordering information scheme

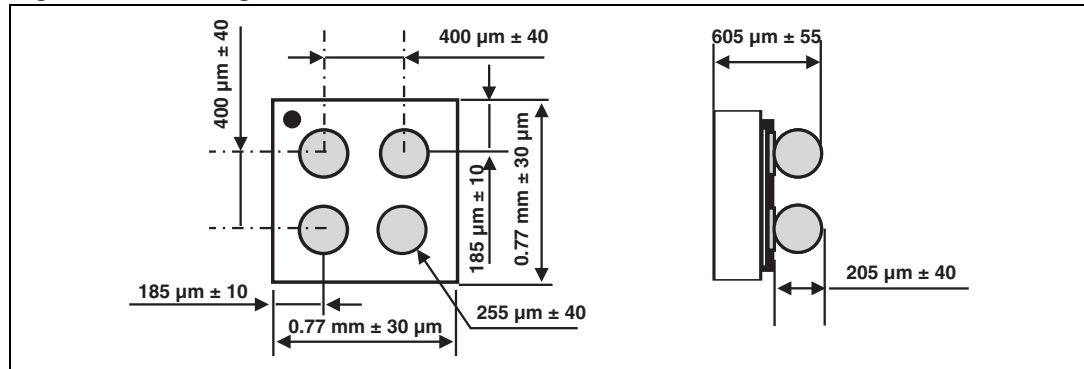
Figure 16. Ordering information scheme



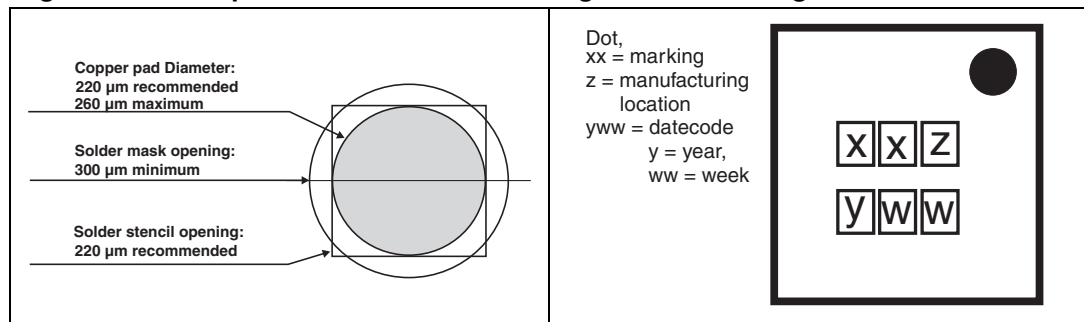
### 3 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

**Figure 17. Package dimensions**



**Figure 18. Foot print recommendations**     **Figure 19. Marking**



**Note:** Product marking may be rotated by 90° for assembly plant differentiation. In no case should this product marking be used to orient the component for its placement on a PCB. Only pin 1 mark is to be used for this purpose.



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