



# BUK9M42-60E

N-channel 60 V, 42 mΩ logic level MOSFET in LFAK33

30 March 2020

Product data sheet

## 1. General description

Logic level N-channel MOSFET in an LFAK33 (Power33) package using TrenchMOS technology. This product has been designed and qualified to AEC Q101 standard for use in high performance automotive applications.

## 2. Features and benefits

- Q101 compliant
- Repetitive avalanche rated
- Suitable for thermally demanding environments due to 175 °C rating
- True logic level gate with  $V_{GS(th)}$  rating of greater than 0.5 V at 175 °C

## 3. Applications

- 12 V automotive systems
- Motors, lamps and solenoid control
- Transmission control
- Ultra high performance power switching

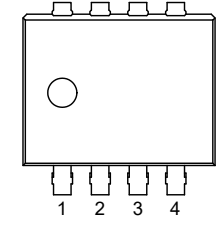
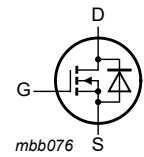
## 4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	-	60	V
$I_D$	drain current	$V_{GS} = 5\text{ V}; T_{mb} = 25\text{ °C};$ <a href="#">Fig. 2</a>	-	-	22	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C};$ <a href="#">Fig. 1</a>	-	-	44	W
<b>Static characteristics</b>						
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 5\text{ V}; I_D = 5\text{ A}; T_j = 25\text{ °C};$ <a href="#">Fig. 11</a>	-	34	42	mΩ
<b>Dynamic characteristics</b>						
$Q_{GD}$	gate-drain charge	$I_D = 5\text{ A}; V_{DS} = 48\text{ V}; V_{GS} = 5\text{ V};$ $T_j = 25\text{ °C};$ <a href="#">Fig. 13</a> ; <a href="#">Fig. 14</a>	-	3.4	-	nC

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	Source	 <p>LFAK33 (SOT1210)</p>	
2	S	Source		
3	S	Source		
4	G	Gate		
mb	D	Mounting base; connected to drain		

## 6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK9M42-60E	LFAK33	Plastic, single ended surface mounted package (LFAK33); 8 leads; 0.65 mm pitch	SOT1210

## 7. Marking

Table 4. Marking codes

Type number	Marking code
BUK9M42-60E	94260E

## 8. Limiting values

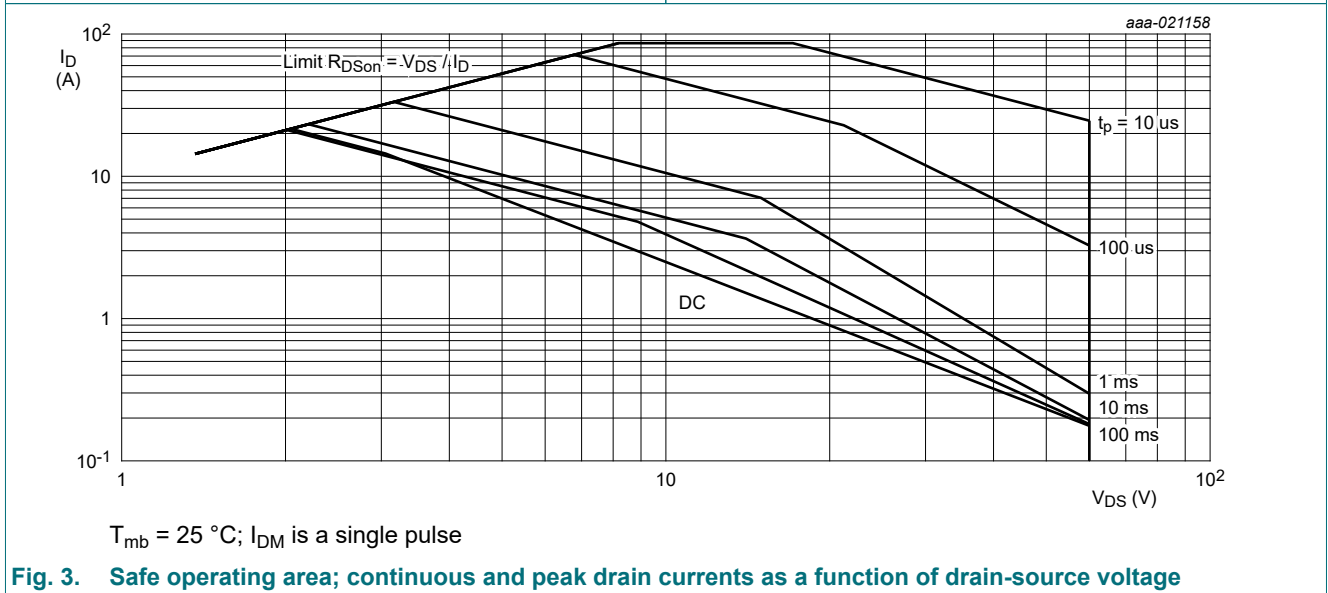
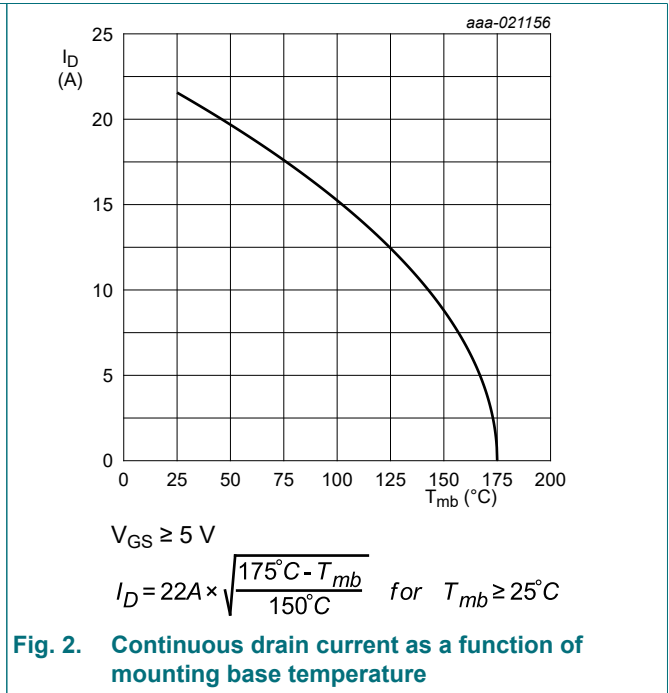
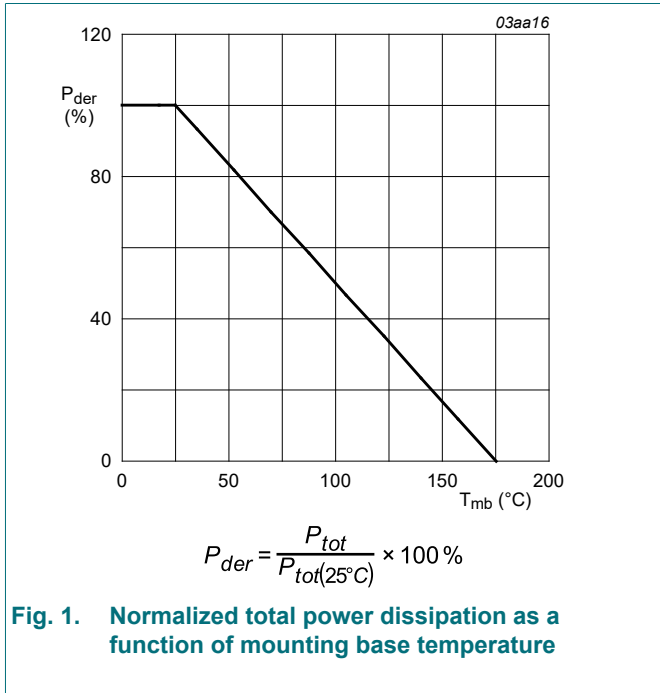
Table 5. Limiting values

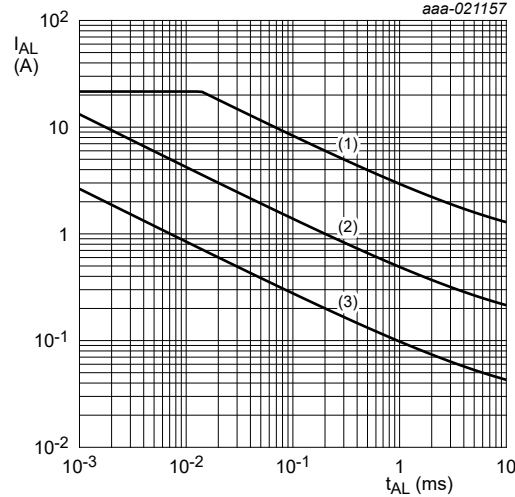
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	60	V
$V_{DGR}$	drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$	-	60	V
$V_{GS}$	gate-source voltage	DC; $T_j \leq 175\text{ °C}$	-10	12	V
		Pulsed; $T_j \leq 175\text{ °C}$	[1] [2] -15	15	V
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; Fig. 1	-	44	W
$I_D$	drain current	$V_{GS} = 5\text{ V}$ ; $T_{mb} = 25\text{ °C}$ ; Fig. 2	-	22	A
		$V_{GS} = 5\text{ V}$ ; $T_{mb} = 100\text{ °C}$ ; Fig. 2	-	15.2	A
$I_{DM}$	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; $T_{mb} = 25\text{ °C}$ ; Fig. 3	-	86	A
$T_{stg}$	storage temperature		-55	175	°C
$T_j$	junction temperature		-55	175	°C
<b>Source-drain diode</b>					
$I_S$	source current	$T_{mb} = 25\text{ °C}$	-	22	A
$I_{SM}$	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; $T_{mb} = 25\text{ °C}$	-	86	A

Symbol	Parameter	Conditions	Min	Max	Unit	
<b>Avalanche ruggedness</b>						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 22\text{ A}$ ; $V_{sup} \leq 60\text{ V}$ ; $R_{GS} = 50\ \Omega$ ; $V_{GS} = 5\text{ V}$ ; $T_{j(\text{init})} = 25\text{ }^\circ\text{C}$ ; unclamped; <a href="#">Fig. 4</a>	[3] [4]	-	11.7	mJ

- [1] Accumulated pulse duration up to 50 hours delivers zero defect ppm.
- [2] Significantly longer life times are achieved by lowering  $T_j$  and or  $V_{GS}$
- [3] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.
- [4] Refer to application note AN10273 for further information.





(1)  $T_{j\text{(init)}} = 25\text{ °C}$ ; (2)  $T_{j\text{(init)}} = 150\text{ °C}$ ; (3) Repetitive Avalanche

Fig. 4. Avalanche rating; avalanche current as a function of avalanche time

### 9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5	-	2.77	3.4	K/W

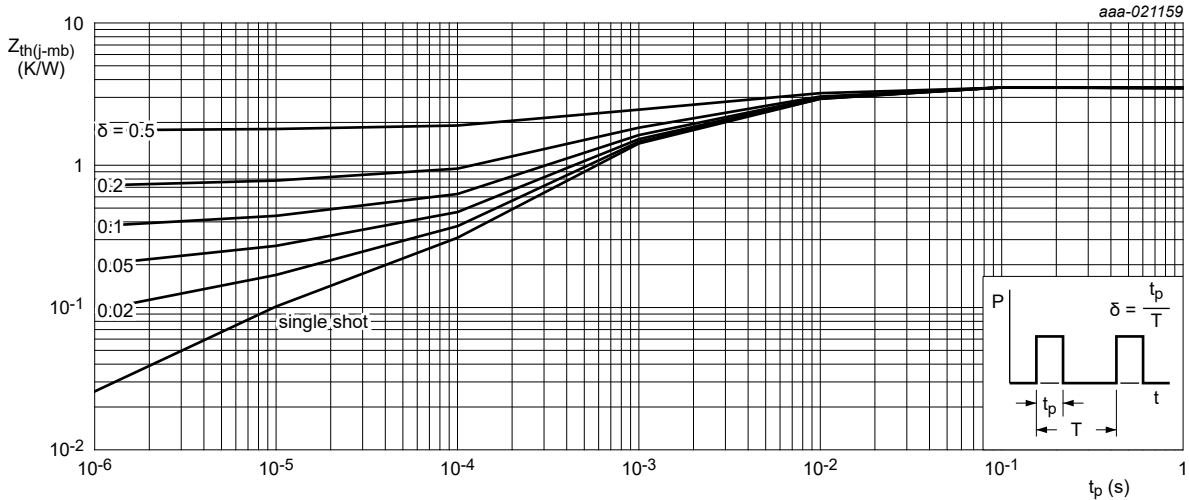


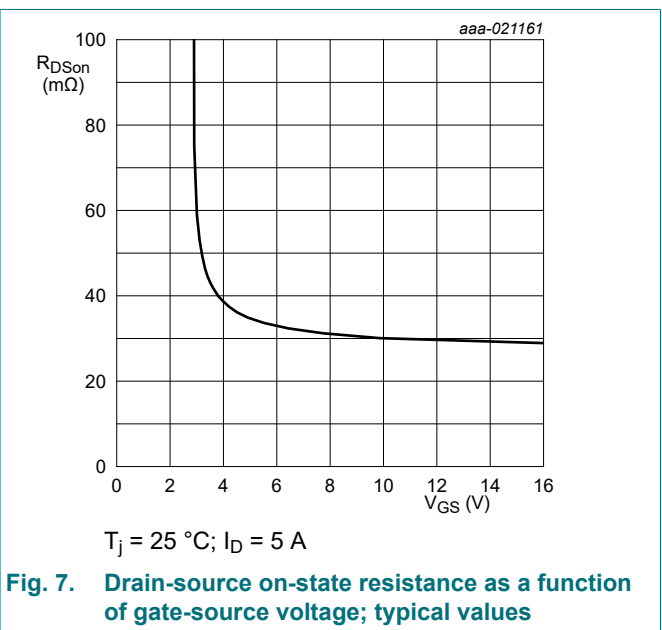
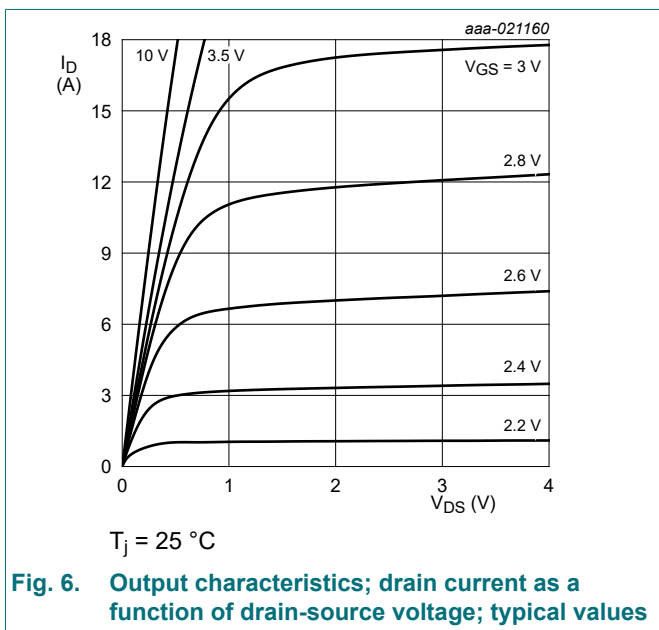
Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

### 10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250\text{ }\mu\text{A}; V_{GS} = 0\text{ V}; T_j = 25\text{ °C}$	60	-	-	V
		$I_D = 250\text{ }\mu\text{A}; V_{GS} = 0\text{ V}; T_j = -55\text{ °C}$	54	-	-	V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ\text{C};$ Fig. 9; Fig. 10	1.4	1.7	2.1	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ\text{C};$ Fig. 10	-	-	2.45	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ\text{C};$ Fig. 10	0.5	-	-	V
$I_{DSS}$	drain leakage current	$V_{DS} = 60 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	0.01	1	$\mu\text{A}$
		$V_{DS} = 60 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 \text{ }^\circ\text{C}$	-	-	500	$\mu\text{A}$
$I_{GSS}$	gate leakage current	$V_{GS} = 12 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	2	100	nA
		$V_{GS} = -10 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	2	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 5 \text{ V}; I_D = 5 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$ Fig. 11	-	34	42	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 5 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$ Fig. 11	-	30	37	mΩ
		$V_{GS} = 5 \text{ V}; I_D = 5 \text{ A}; T_j = 175 \text{ }^\circ\text{C};$ Fig. 12	-	-	95	mΩ
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$I_D = 5 \text{ A}; V_{DS} = 48 \text{ V}; V_{GS} = 5 \text{ V}; T_j = 25 \text{ }^\circ\text{C};$ Fig. 13; Fig. 14	-	8.3	-	nC
$Q_{GS}$	gate-source charge		-	1.7	-	nC
$Q_{GD}$	gate-drain charge		-	3.4	-	nC
$C_{iss}$	input capacitance	$V_{DS} = 25 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ\text{C};$ Fig. 15	-	652	867	pF
$C_{oss}$	output capacitance		-	75	90	pF
$C_{rss}$	reverse transfer capacitance		-	47	64	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 45 \text{ V}; R_L = 5 \text{ } \Omega; V_{GS} = 5 \text{ V}; R_{G(ext)} = 5 \text{ } \Omega; T_j = 25 \text{ }^\circ\text{C}$	-	6.2	-	ns
$t_r$	rise time		-	9.7	-	ns
$t_{d(off)}$	turn-off delay time		-	12.9	-	ns
$t_f$	fall time		-	8.4	-	ns
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = 5 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C};$ Fig. 16	-	0.82	1.2	V
$t_{rr}$	reverse recovery time	$I_S = 5 \text{ A}; dI_S/dt = -100 \text{ A}/\mu\text{s}; V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	15.6	-	ns
$Q_r$	recovered charge		-	11.4	-	nC



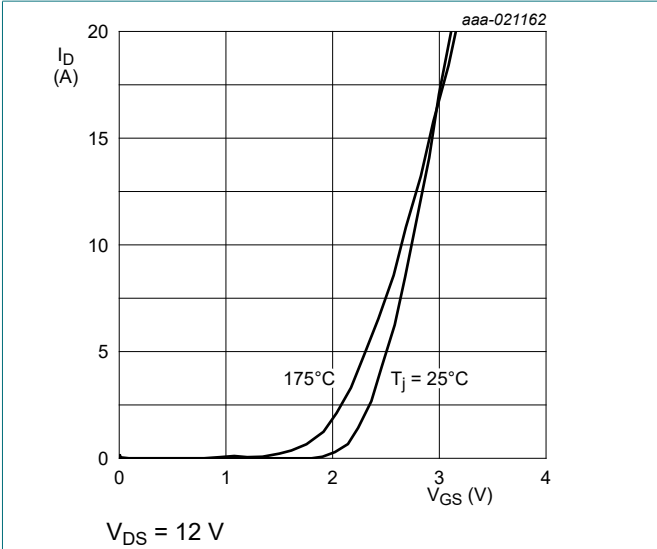


Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values

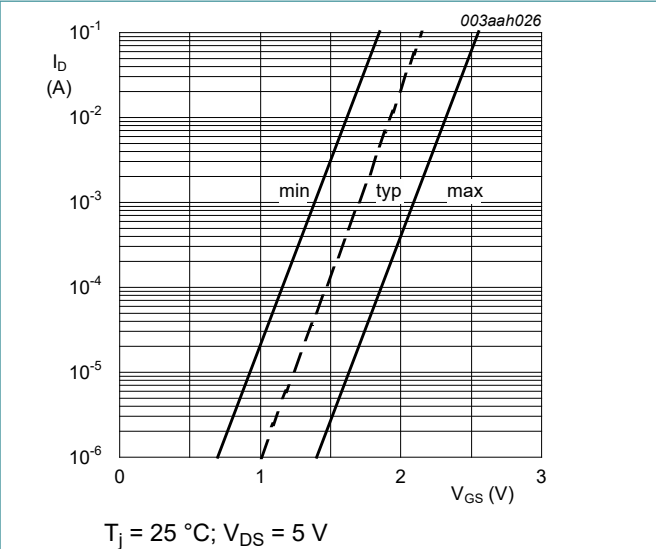


Fig. 9. Sub-threshold drain current as a function of gate-source voltage

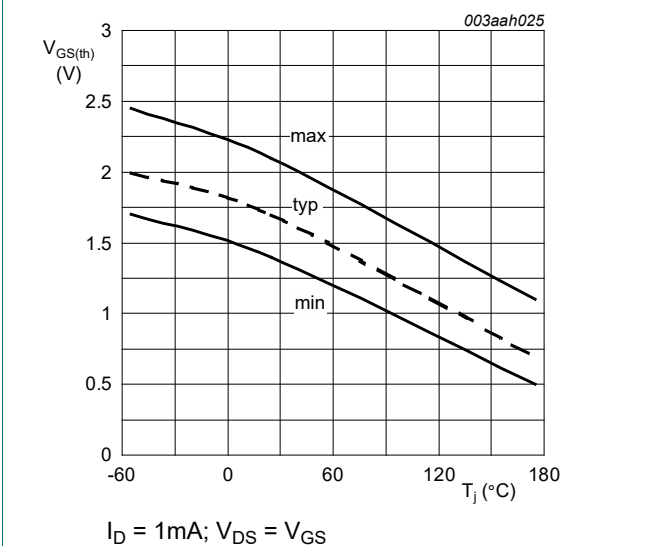


Fig. 10. Gate-source threshold voltage as a function of junction temperature

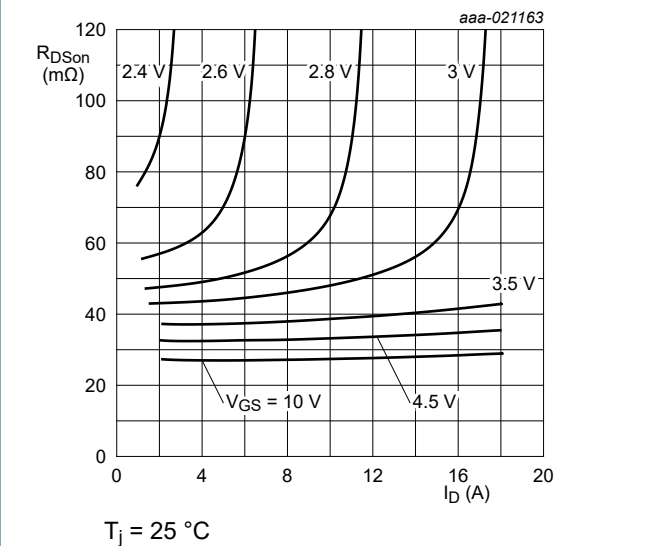
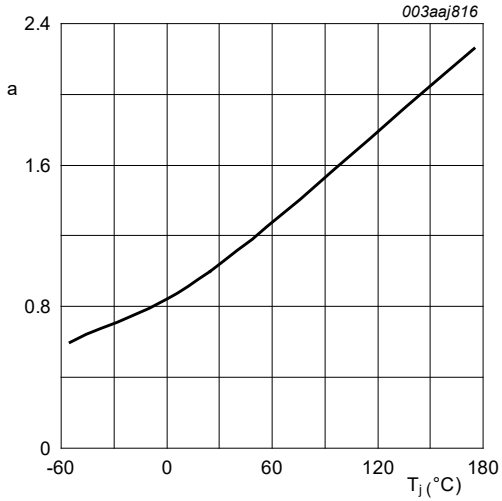
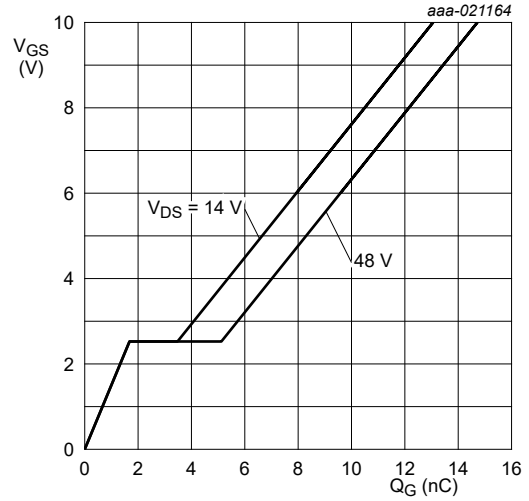


Fig. 11. Drain-source on-state resistance as a function of drain current; typical values



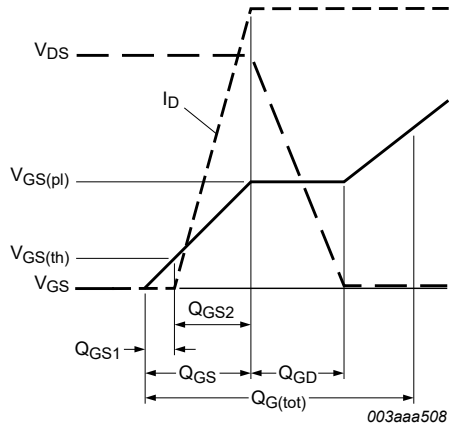
$$a = \frac{R_{DSon}}{R_{DSon}(25^{\circ}\text{C})}$$

**Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature**

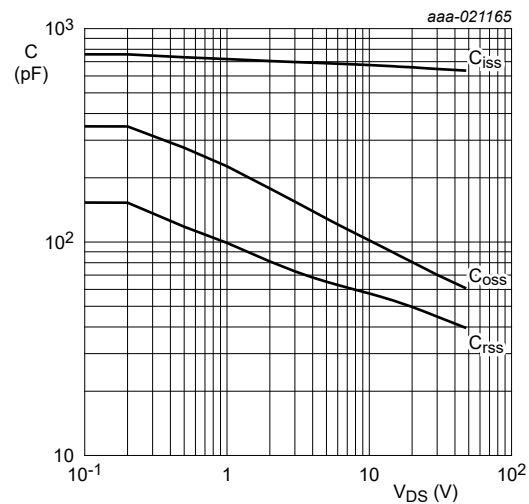


$T_j = 25^{\circ}\text{C}; I_D = 5\text{ A}$

**Fig. 13. Gate-source voltage as a function of gate charge; typical values**

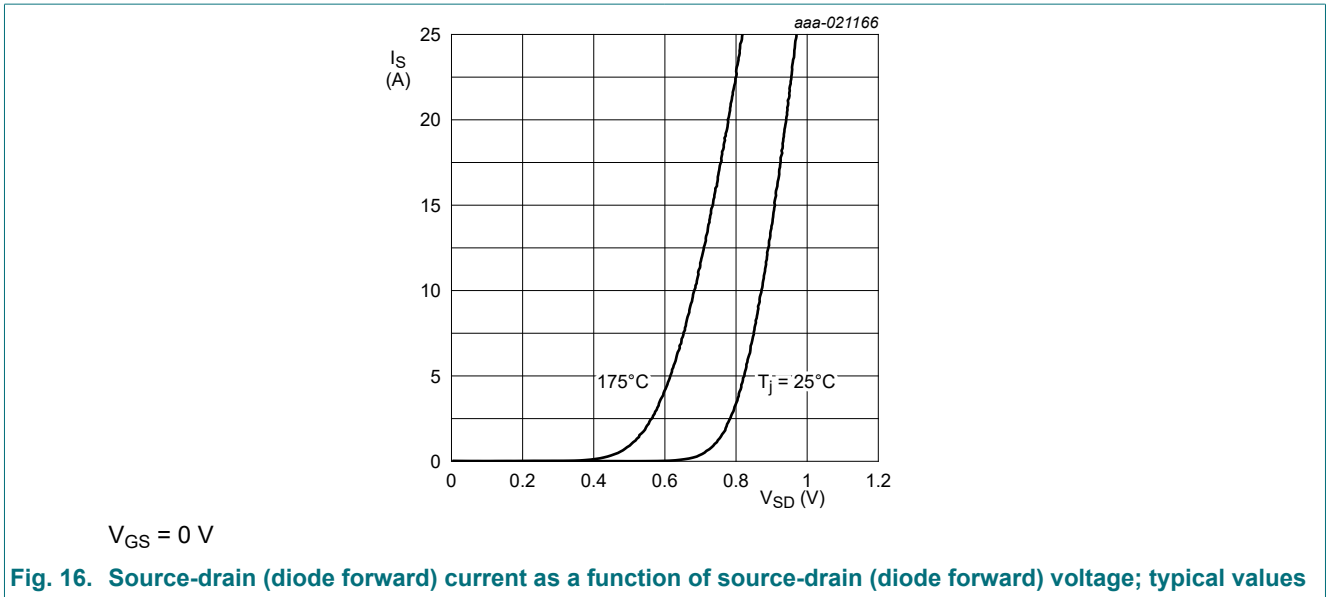


**Fig. 14. Gate charge waveform definitions**



$V_{GS} = 0\text{ V}; f = 1\text{ MHz}$

**Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**

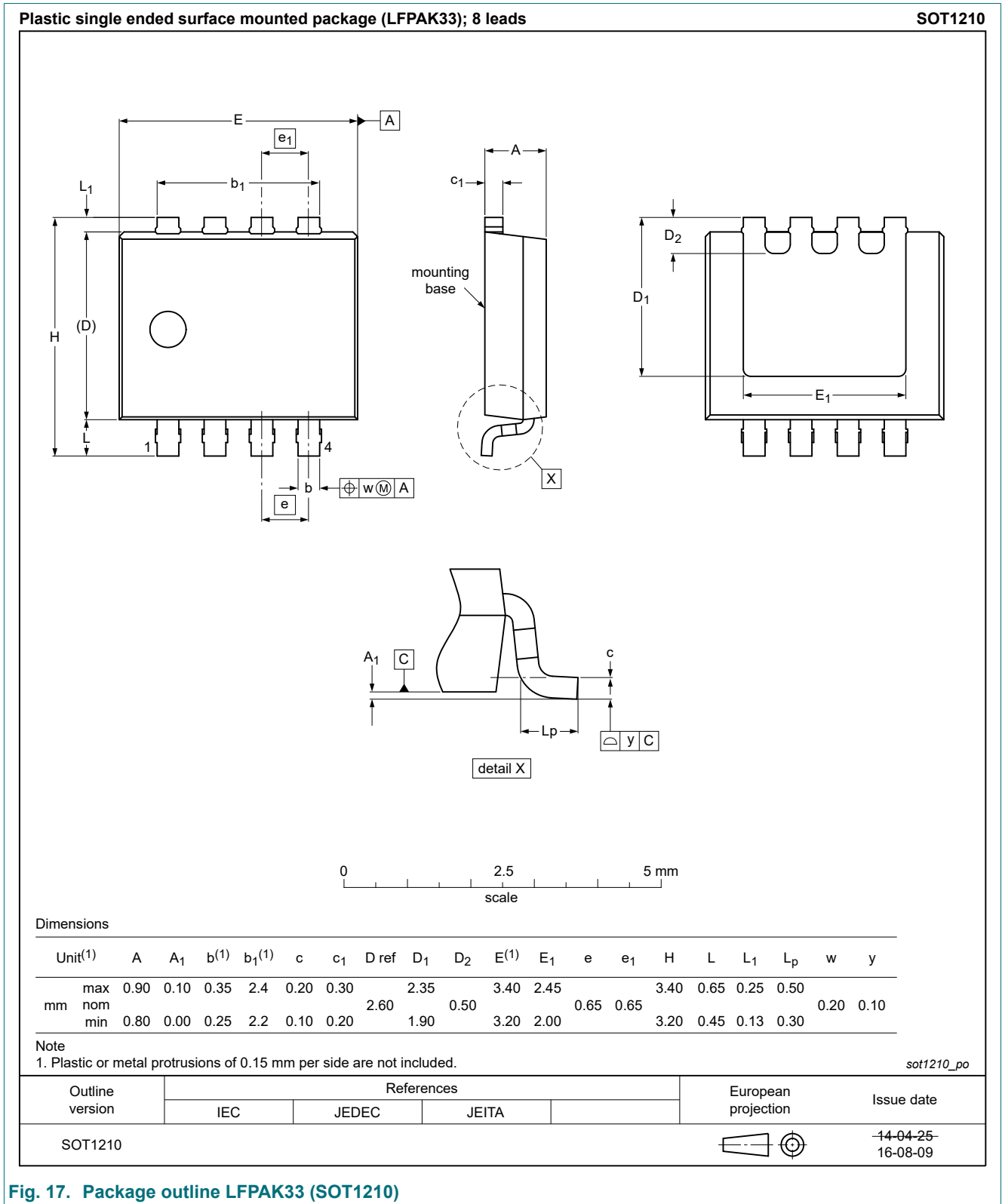


## 11. Application information

For guidance on how to use and understand this datasheet, please refer to application note [AN11158](#) "Understanding power MOSFET datasheet parameters".

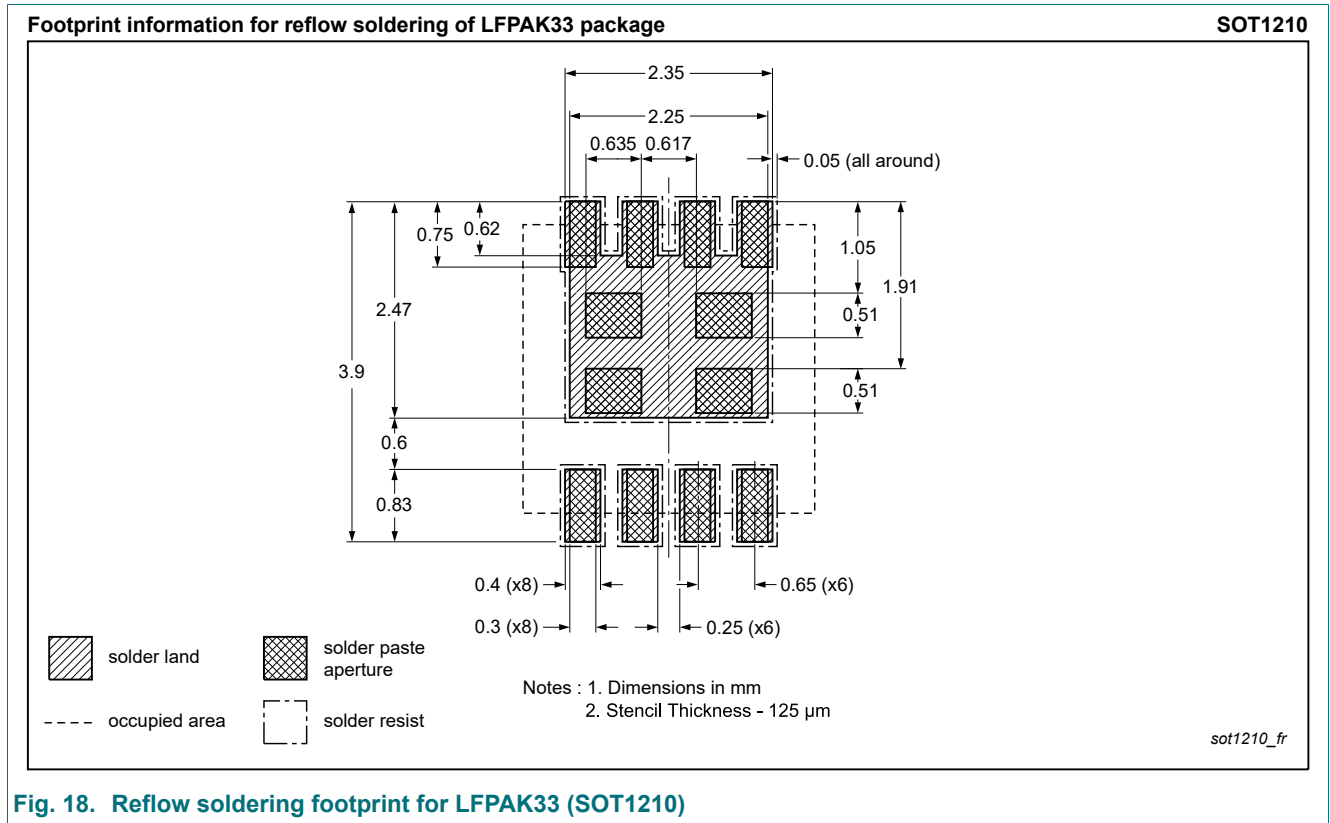


## 12. Package outline



**Fig. 17. Package outline LPAK33 (SOT1210)**

### 13. Soldering



**Fig. 18. Reflow soldering footprint for LFPAK33 (SOT1210)**

## 14. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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