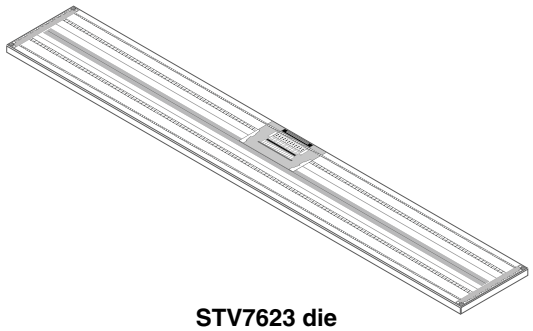
STV7623

480 output high-voltage gate driver

Features

- 2-level high voltage output gate driver
- 480 channels with -40/+35 mA source/sink output current capability
- 75 V output swing within +/- 45 V limits
- 3.0 to 3.6 V digital power supply
- 1.8 V CMOS input signal compatibility
- Selectable 480 or 400 outputs
- Direct input to bidirectional shift registers
- Selectable polarity and blanking function
- High voltage BCD process technology
- Bumped dice in tray
- Output stage similar to STV7622
- PCB-less compatible dice



STV7623 die

Description

The STV7623 is a 1-bit x 480 shift register with dual rail high voltage/medium current output, with global blank and polarity control.

The maximum shift frequency starts from 1 MHz for a 1.8 V type input signal, up to 10 MHz for a 3.3 V type input signal. This generic device can be used for segmented/dot matrix electroluminescent displays to drive an array of organic electronic transistors, or for technologies related to e-Paper/e-Reader/digital signage solutions.

The device can be daisy-chained for various display resolutions.

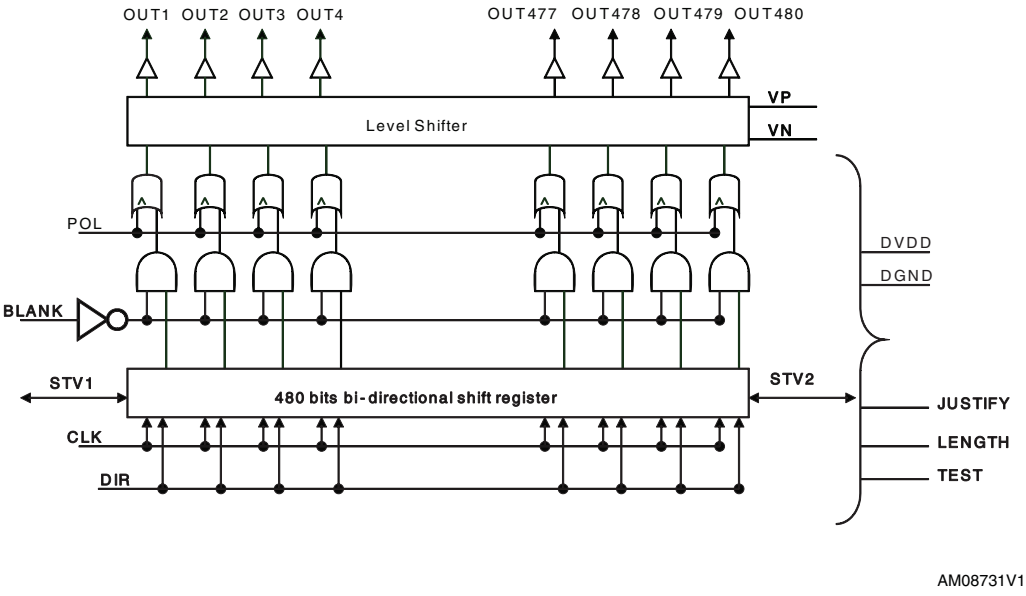
Table 1. Device summary

Order code	Temperature	Package	Packing
STV7623WPB3	-25°C to +70°C	Bumped dice	3-inch tray

Contents

1 Description

Figure 1. STV7623 block diagram



1.1 Pin description

Figure 2. PCB-Less COF pinout diagram

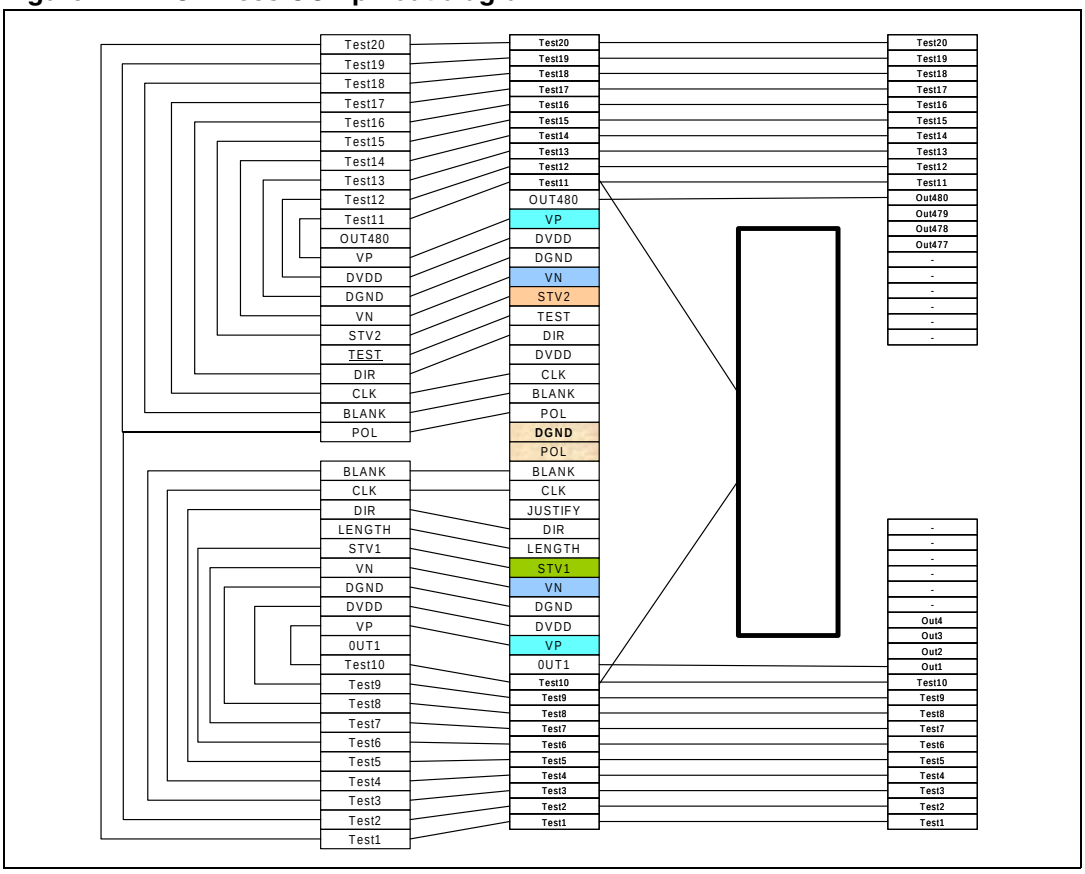


Figure 2 shows the possible design of a custom COF with wire on array (WOA) routing (PCB-less). This example supports only 480 outputs.

Table 2. Pin description

Pin name	I/O	Function	Description
CLK	In	Shift clock Input	Clock input for the chip internal shift register. Data is shifted at each rising edge of this clock.
DIR	In	Shift direction Control pin	This pin controls the output shifting direction.
STV1 STV2	I/O	Start pulse input/output pin	These pins are used to control the channel start pulse input or output pin. The function of these two pins depends on the status of DIR pin (refer to the *Section 3: Truth tables*)
BLANK	In	Output enable control	This pin is used to control the channel output. When BLANK is high, the shift register is bypassed (overriden) and all driver outputs are fixed to VN level instantly, (when POL= L). It is assumed this signal affect few outputs

Table 2. Pin description (continued)

Pin name	I/O	Function	Description
POL	In	Polarity pin	When POL is low, VP and VN are swapped functionally at the output pins level. This signal is assumed static.
OUT1..OUT480	Out	Driver output pins	The output voltage is either VP or VN for driving the gate electrode, depending on the data stored in the shift register. It is assumed that only up to 4 outputs are changing level simultaneously.
VP	Power	Power supply	High voltage supply (eg +50 V)
DVDD	Power	Power supply	Digital power supply
DGND	Power	Power supply	Digital ground
VN	Power	Power supply	Negative supply
TEST	In	Test pin	Test pin (must be grounded in application)
LENGTH	In	Nb of active outputs	When LENGTH =0, enable 480 outputs When LENGTH =1, enable 400 outputs This signal is assumed static
JUSTIFY	In	Partial output justify mode	Only applicable when LENGTH=1 When JUSTIFY = 0, use outputs 0 to 399 When JUSTIFY = 1, use outputs 80 to 479 This signal is assumed static.

In the pinout diagram:

- TEST is used to test the device.

2 Functional description

The STV7623 includes all the logic and power circuits necessary to drive the thin-film transistor (TFT) of an active matrix display backplane. A low-voltage logic block manages data information, and a high-voltage block converts the low-voltage information stored in the logic block into high-voltage signals applied to the display gate lines.

2.1 Device operation

In the condition of DIR=L, the STV1 start pulse input is sensed at the rising edge of CLK and stored in the first stage of shift register, which causes the first scan signal is outputted from the OUT1 output pin. While stored data is transferred to the next stage of the shift register at the rising edge of the CLK signal, new data of STV1 is sensed and stored simultaneously.

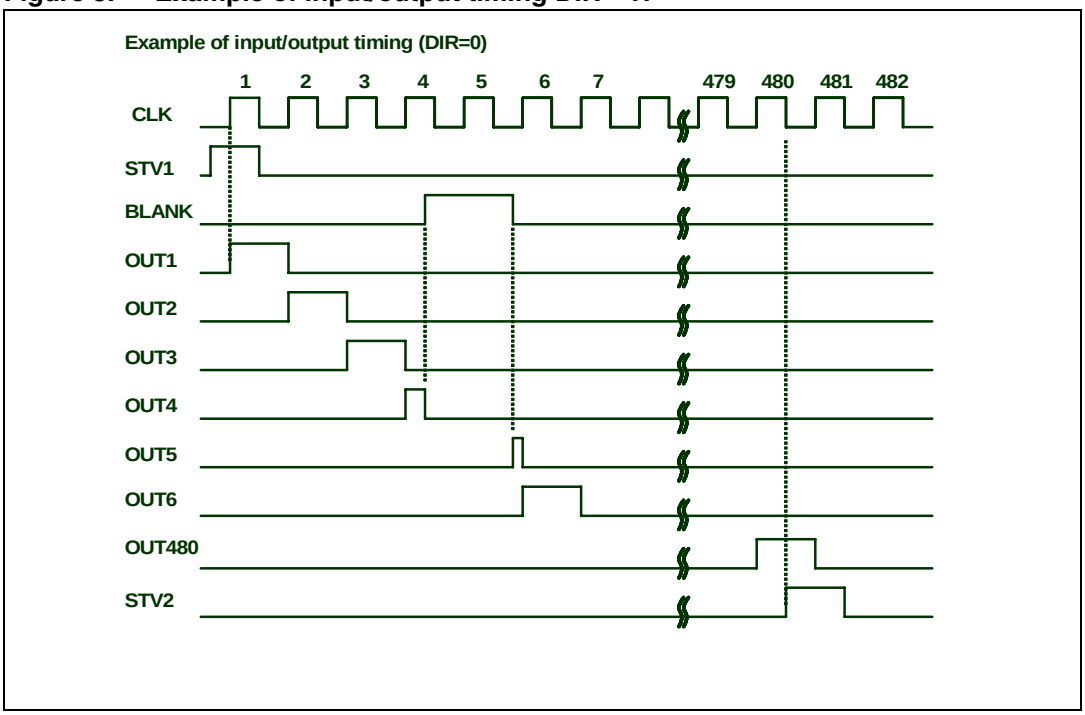
The output pin (OUT1 to OUT480) supplies VP or VN voltage to the gate lines depending on the data stored in the shift register. For normal operation, a VP voltage is outputted one by one like a shift token from OUT1 to OUT480, in sync with CLK pulse.

STV2 goes up to high level at the 400/480th falling edge of CLK and goes down to low level at the 401/481th falling edge of CLK. This STV2 is connected to the next driver IC STV1 signal to cascade (daisy chain) them.

When STV2 is an output, the signal is activated for 1/2 clock later.

When the chip is configured in 400 output mode, only the first 400 bits entering the shift register are used, the remaining 80 outputs are removed from the shift register.

Figure 3. Example of input/output timing DIR = H

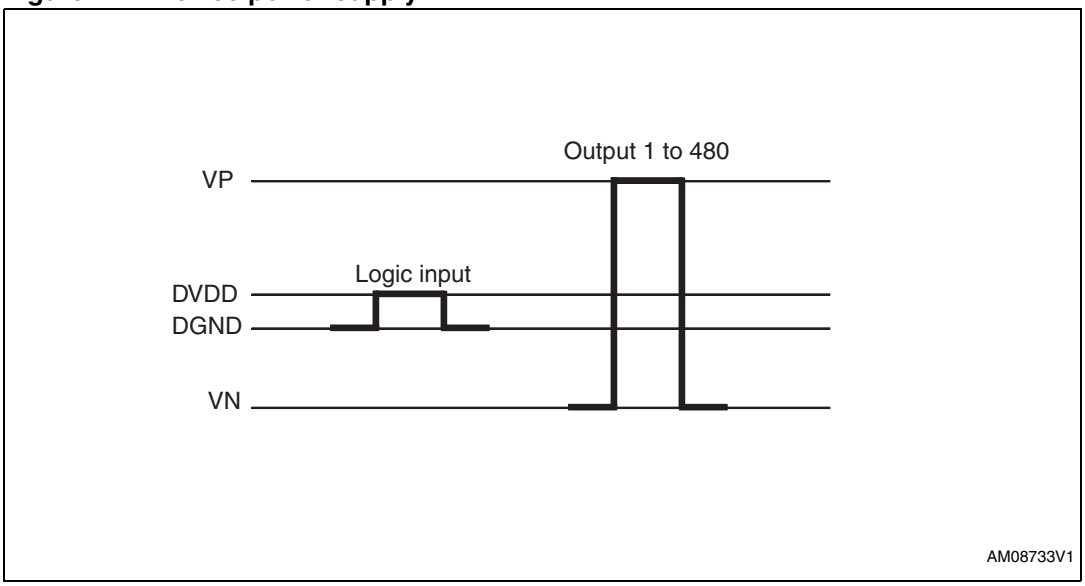


2.2 Device power supply

The STV7623 must be used with the following conditions when operating:

- VP - VN < 75 V
- VP-DGND > 10 V
- DGND-VN > 10V

Figure 4. Device power supply

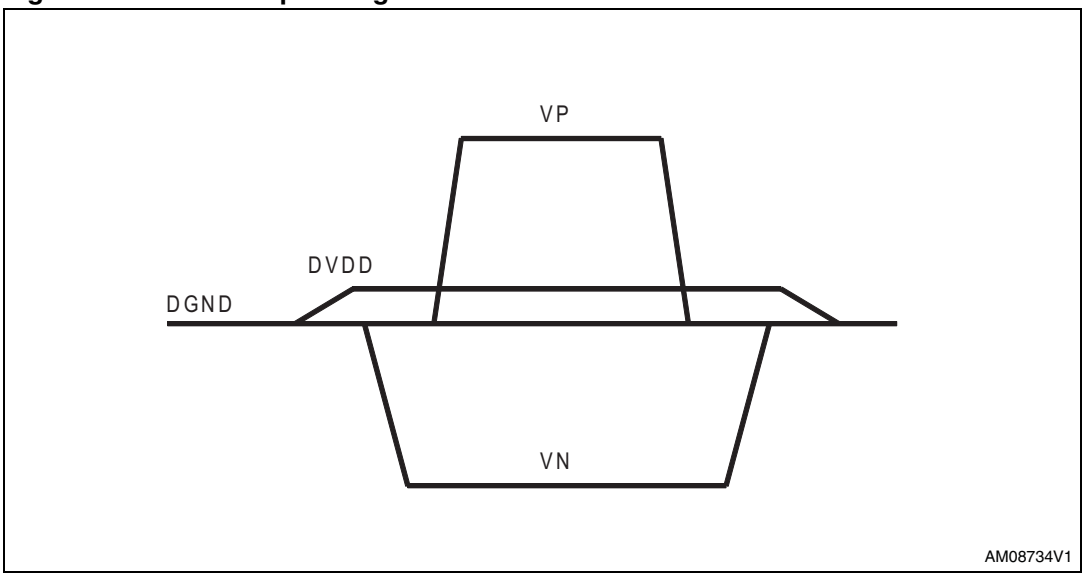


2.3 Power sequencing

To prevent the device from being damaged by latchup, the power ON/OFF sequence it is recommended to follow the procedure below:

- Power OFF => ON: DVDD -> VN -> VP
- Power ON => OFF, VP -> VN -> DVDD

Figure 5. Power sequencing



3 Truth tables

Table 3. Output level truth table

Input pins			
Data bit	**Blank**	**POL**	**OUTn**
0	0	1	VP (+)
1	0	1	VN (-)
X	1	1	VP (+)
X	1	0	VN (-)
1	0	0	VP (+)
0	0	0	VN (-)

Table 4. Output ordering truth table

Configurations							Comments
Length	**Justify**	**Dir**	**In**	**First**	**Last**	**Out**	
0	0	0	STV1	OUT1	OUT480	STV2	All outputs
0	1	0	STV1	OUT1	OUT480	STV2	All outputs
1	0	0	STV1	OUT1	OUT400	STV2	1..400
1	1	0	STV1	OUT81	OUT480	STV2	81..480
0	0	1	STV2	OUT480	OUT1	STV1	All outputs
0	1	1	STV2	OUT480	OUT1	STV1	All outputs
1	0	1	STV2	OUT400	OUT1	STV1	1..400
1	1	1	STV2	OUT480	OUT81	STV1	81..480

When only 400 outputs are used, the remaining 80 outputs remain static.

4 Absolute maximum rating

Stressing the device above the rating listed in the “absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 5. Absolute maximum ratings (V_{SS} = 0 V, 25 °C)

Symbol	Parameter	Value	Unit
V_{DD}	Digital supply range	-0.3 to +4.0	V
VP	Positive voltage supply	-0.3 to +50	V
VN	Negative voltage supply	+0.3 to -50	V
Vp-Vn	Voltage difference	90	V
V_{IN}	Logic input voltage range	-0.3 to DV_{DD}+0.3	mV
I_{pout}	Driver output current x(1) (2) (3)	- 70 to +35	mA
I_{dout}	Diode output current(1) (2) (3)	-200 to +300	mA
V_{out}	Output voltage range	-0.3 to +90	V
V_{ESD}	ESD susceptibility, human body model (100 pF discharged through 1.5 KΩ), on all except the V_{CC} pins(4)	2	kV
T_{jmax}	Maximum junction temperature	-40 to +100	°C
T_{stg}	Storage temperature range (die)	-65 to +150	°C

1. Measurements done on one single output, x. The other outputs are either not used or are connected to output x. Assumes junction temperature remains less than Tjmax during measurement.
2. All transient current measurements are made under conditions close to those encountered in a typical application (that is, with duration of any output current spike always less than 300 ns).
3. These parameters are measured during STMicroelectronics’ internal qualification which includes temperature characterization on standard as well as corner batches of the process. These parameters are not tested in production.

5 Electrical characteristics

5.1 DC electrical characteristics (D_{GND} = 0 V)

D_{VDD} = 3.3 V, V_P = 30 V, V_N = -45V, T_{AMB} = 25 °C, f_{CLK} = 1 MHz, unless otherwise specified.

Table 6. Electrical characteristics - supply

Symbol	Parameter	Value			Unit
		Min	Typ	Max	
D_{VDD}	Digital supply voltage	3.0	3.3	3.6	V
I_{DD}	Digital supply current(1)	–	60	–	µA
I_{DDL}	Digital dynamic supply current (CLK1 freq = 1 MHz)(2)	–	900	–	µA
I_{DD}	Digital supply current at V_{IH} = 2.0 V	–	80	–	µA
V_P	DC power output positive supply voltage	+10	–	–	V
V_N	DC power output negative supply voltage	–	–	-10	V
V_P-V_N	Voltage gap Vp-Vn	20	–	80	V
I_{PPH}	Power output supply current (steady outputs)	–	–	500	µA

1. For 3.3V CMOS input logic levels (0 or 3.3 V)
2. All input data is switched at 0.5 MHz rate.

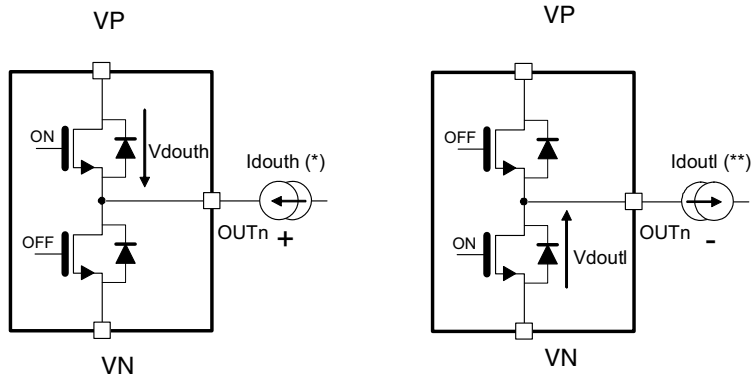
Table 7. Electrical characteristics - OUT1 to OUT480

Symbol	Parameter	Value			Unit
		Min	Typ	Max	
Vpouth	Power output high level (voltage drop versus VP) at Ipouth = -20 mA and VP = 30 V	–	4	–	V
Vpoutl	Power output low level at Ipoutl = +20 mA, VN=-45 V	–	6	–	V
Vdouth	Output upper diode voltage drop at Idouth = +30 mA	–	1	2	V
Vdoutl	Output lower diode voltage drop at Idoutl = -30 mA	-2	-1	–	V

Table 8. Electrical characteristics - standard mode, TTL/LVCMOS inputs: CLK, DIR, blank, POL, STV1, STV2, length, justify

Symbol	Parameter	Value			Unit
		Min	Typ	Max	
V_{IH}	High level input voltage	1.2	–	D_{VDD}	V
V_{IL}	Low level input voltage	D_{GND}	–	0.6	V
V_{OH}	High level output voltage I_{OH} = 200 µA	D_{VDD}-0.3	–	DVdd	V
V_{OL}	Low level output voltage I_{OH} = 200 µA	D_{GND}	–	D_{GND}+0.3	V
I_{IH}	High level input current ($V_{IH} \geq 2.0$ V)	-1	–	1	µA
I_{IL}	Low level input current (V_{IL} = 0 V)	-1	–	1	µA

Figure 6. Output test configuration

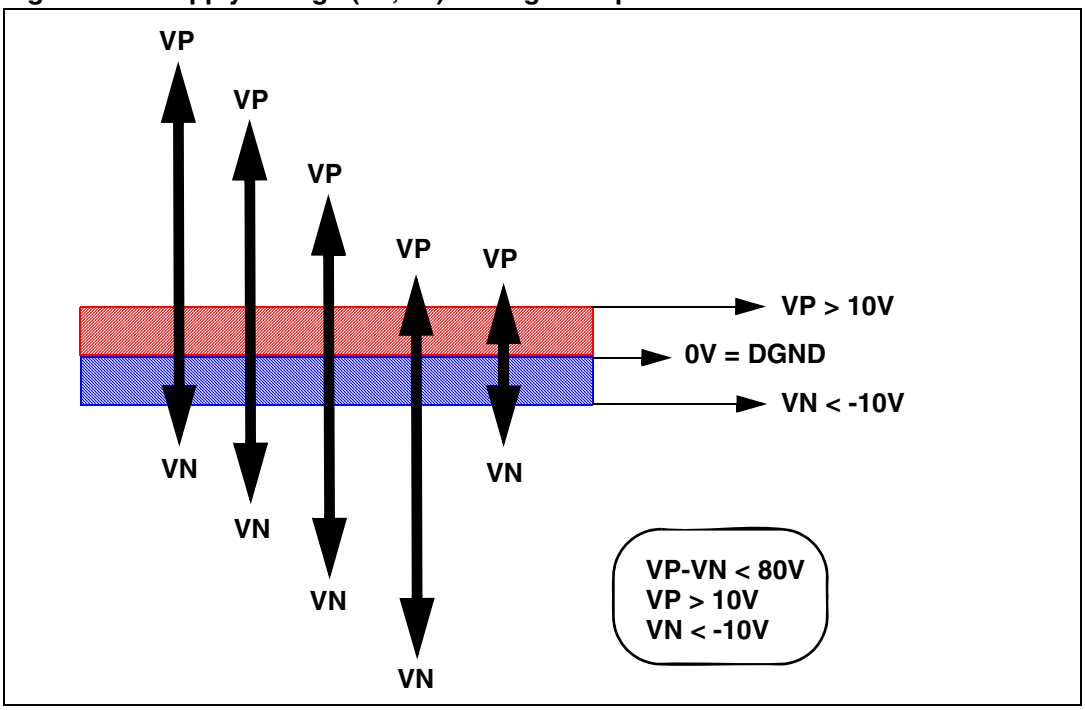


(*) Output sinking current is considered as positive.

(**) Output sourcing current is considered as negative.

AM04132V1

Figure 7. Supply voltage (VP,VN) setting examples



5.2 AC characteristics

D_{VDD} = 3.3 V to 3.6 V, T_{amb} = -20°C to +85°C, input signal edge maximum rise and fall times (tr, tf) = 3 ns load condition: 68 pF, 3.9 kΩ, 333 pF.

Table 9. AC timing requirements

Symbol	Parameter	Value			Unit
		Min	Typ	Max	
t_{CLK}	Data clock period	0.1	–	–	µs
F_{CLK}	Max clock frequency	–	200k	1M/10M(1)(2)	Hz
t_{WHCLK}	Duration of clock pulse at high level	400, 40(2)	–	–	ns
t_{WLCLK}	Duration of clock pulse at low level	400, 40(2)	–	–	ns
t_{SDAT}	Input data set-up time before low-to-high clock transition	25	–	–	ns
t_{HDAT}	Input data hold-time after low-to-high clock transition	25	–	–	ns

1. If the digital inputs are 3.3V +/-10%, max clock frequency can be 10 MHz
2. Output blanked during data shift.

Test condition: 25 °C ambient, VP = +30, VN = -45 V, D_{VDD} = 3.3 V.

5.3 Timing requirements

D_{VDD} = 3.3 V, V_P = +30 V, V_N = -45 V, T_{amb} = 25 °C, F_{clk}= 1 MHz, $V_{ILmax} = 0.2 \times D_{VDD}$, $V_{IHmin} = 0.8 \times D_{VDD}$

Table 10. AC timing characteristics

Symbol	Parameter	Value			Unit
		Min	Typ	Max	
t_{PHL1} t_{PLH1}	Delay of power output change after CLK transition - High to low - Low to high	–	100	–	ns
t_{PHL2} t_{PLH2}	Delay of power output change after POL transition - High to low - Low to high	–	100	–	ns
t_{PHL3} t_{PLH3}	Delay of power output change after BLANK transition - High to low - Low to high	–	100	–	ns

6 Packing information

Figure 8. Tray (top view)

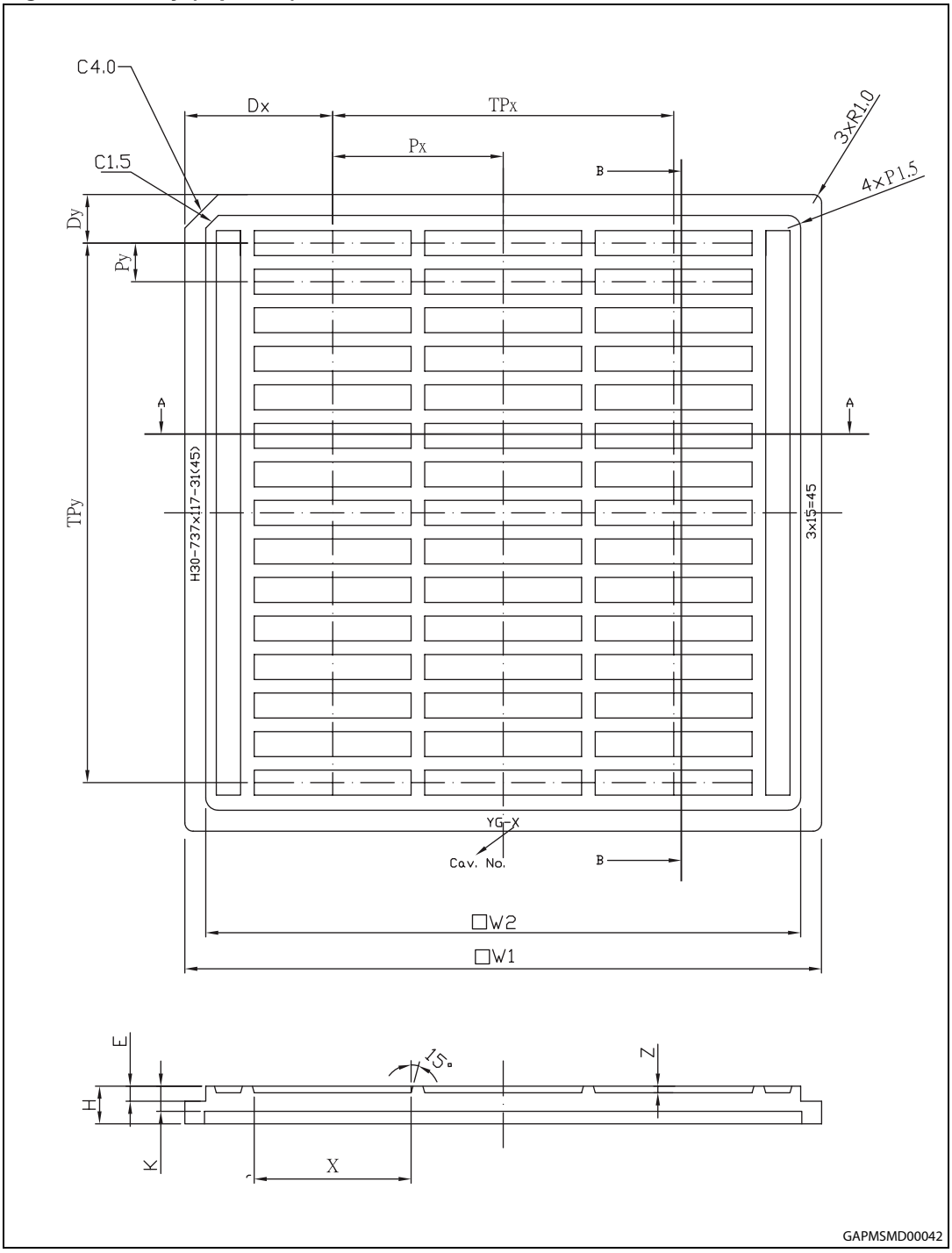
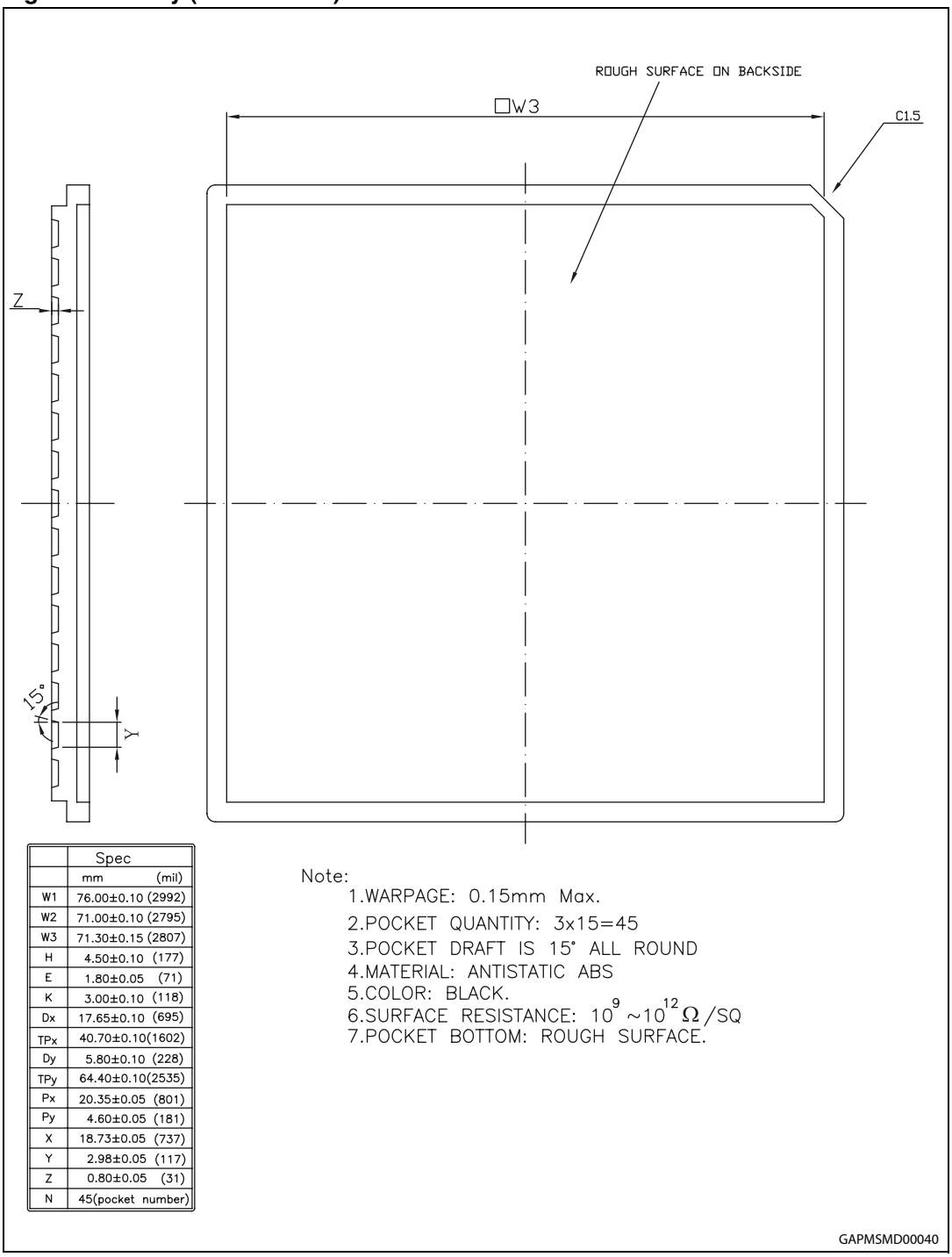


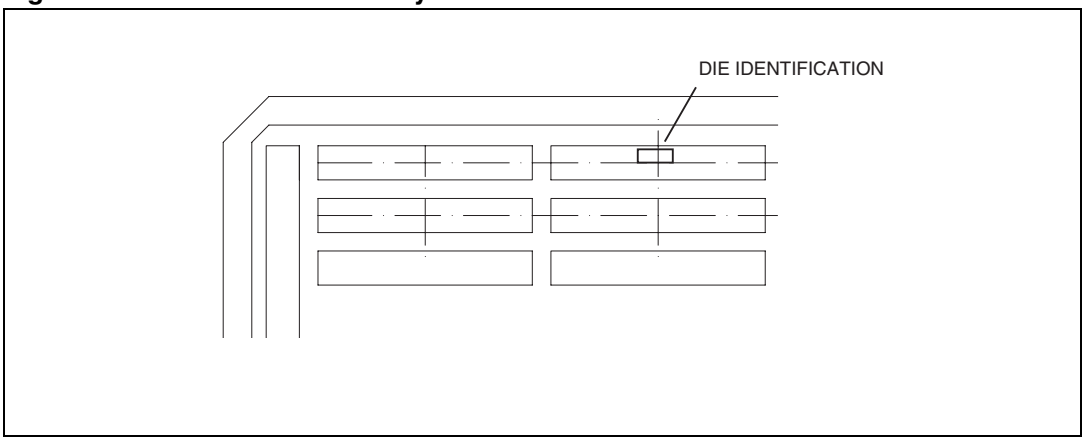
Figure 9. Tray (bottom view)



	Spec mm (mil)
W1	76.00±0.10 (2992)
W2	71.00±0.10 (2795)
W3	71.30±0.15 (2807)
H	4.50±0.10 (177)
E	1.80±0.05 (71)
K	3.00±0.10 (118)
Dx	17.65±0.10 (695)
TPx	40.70±0.10(1602)
Dy	5.80±0.10 (228)
TPy	64.40±0.10(2535)
Px	20.35±0.05 (801)
Py	4.60±0.05 (181)
X	18.73±0.05 (737)
Y	2.98±0.05 (117)
Z	0.80±0.05 (31)
N	45(pocket number)

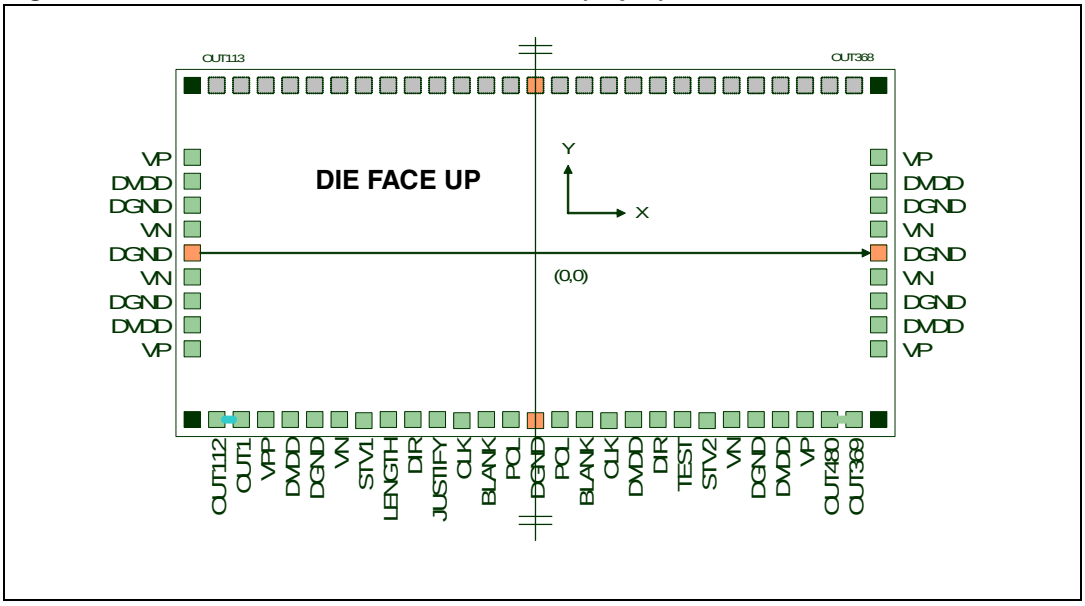
Note:
1.WARPAGE: 0.15mm Max.
2.POCKET QUANTITY: 3x15=45
3.POCKET DRAFT IS 15° ALL ROUND
4.MATERIAL: ANTISTATIC ABS
5.COLOR: BLACK.
6.SURFACE RESISTANCE: $10^{9} \sim 10^{12}\ \Omega/SQ$
7.POCKET BOTTOM: ROUGH SURFACE.

Figure 10. Die orientation in tray



7 Pad information

Figure 11. Pad dimensions and coordinates (in µm)



The reference (x=0, y=0) is the centre of the die. Output pad pitch is 68 µm.

Stress relief pads are connected to V_N (V_{SS}).

Pad size:

- Type 1: (north/south pads) 51 x 51 µm, 68 µm linear pitch, passivation opening 34 x 34 µm.
- Type 2: (east/west) pads
- Type 3: stress relief die corner pads

Alignment: 2 alignment marks, using 2 metals across the input long edge of the die.

Die size = 51 mm^2, with special reticle/wafer map adjustments.

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*                      *
*   PADS extraction    *
*                      *
************************

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CHIP NAME:    STV7623_Top_ICPack


All dimensions are in Microns.
Pad Placement values correspond to each pad center coordinates.
Pad Placement Origin is the center of the die.
LEAD PAD NAME     PAD PLACEMENTS          PAD DIMENSIONS
                  X =          Y =        X =         Y =

Note: vss! == VN line
```

vss!	**-8803.79**	**1251.455**	**73.1**	**73.1 (stress relief bump)**
OUT<113>	**-8670.0**	**1145.46**	**51.0**	**51.0**
OUT<114>	-8602.0	1145.46	51.0	51.0
OUT<115>	-8534.0	1145.46	51.0	51.0
OUT<116>	-8466.0	1145.46	51.0	51.0
OUT<117>	-8398.0	1145.46	51.0	51.0
OUT<118>	-8330.0	1145.46	51.0	51.0
OUT<119>	-8262.0	1145.46	51.0	51.0
OUT<120>	-8194.0	1145.46	51.0	51.0
OUT<121>	-8126.0	1145.46	51.0	51.0
OUT<122>	-8058.0	1145.46	51.0	51.0
OUT<123>	-7990.0	1145.46	51.0	51.0
OUT<124>	-7922.0	1145.46	51.0	51.0
OUT<125>	-7854.0	1145.46	51.0	51.0
OUT<126>	-7786.0	1145.46	51.0	51.0
OUT<127>	-7718.0	1145.46	51.0	51.0
OUT<128>	-7650.0	1145.46	51.0	51.0
OUT<129>	-7582.0	1145.46	51.0	51.0
OUT<130>	-7514.0	1145.46	51.0	51.0
OUT<131>	-7446.0	1145.46	51.0	51.0
OUT<132>	-7378.0	1145.46	51.0	51.0
OUT<133>	-7310.0	1145.46	51.0	51.0
OUT<134>	-7242.0	1145.46	51.0	51.0
OUT<135>	-7174.0	1145.46	51.0	51.0
OUT<136>	-7106.0	1145.46	51.0	51.0
OUT<137>	-7038.0	1145.46	51.0	51.0
OUT<138>	-6970.0	1145.46	51.0	51.0
OUT<139>	-6902.0	1145.46	51.0	51.0
OUT<140>	-6834.0	1145.46	51.0	51.0
OUT<141>	-6766.0	1145.46	51.0	51.0
OUT<142>	-6698.0	1145.46	51.0	51.0
OUT<143>	-6630.0	1145.46	51.0	51.0
OUT<144>	-6562.0	1145.46	51.0	51.0
OUT<145>	-6494.0	1145.46	51.0	51.0
OUT<146>	-6426.0	1145.46	51.0	51.0
OUT<147>	-6358.0	1145.46	51.0	51.0
OUT<148>	-6290.0	1145.46	51.0	51.0
OUT<149>	-6222.0	1145.46	51.0	51.0
OUT<150>	-6154.0	1145.46	51.0	51.0
OUT<151>	-6086.0	1145.46	51.0	51.0
OUT<152>	-6018.0	1145.46	51.0	51.0
OUT<153>	-5950.0	1145.46	51.0	51.0
OUT<154>	-5882.0	1145.46	51.0	51.0
OUT<155>	-5814.0	1145.46	51.0	51.0
OUT<156>	-5746.0	1145.46	51.0	51.0
OUT<157>	-5678.0	1145.46	51.0	51.0
OUT<158>	-5610.0	1145.46	51.0	51.0
OUT<159>	-5542.0	1145.46	51.0	51.0
OUT<160>	-5474.0	1145.46	51.0	51.0
OUT<161>	-5406.0	1145.46	51.0	51.0
OUT<162>	-5338.0	1145.46	51.0	51.0
OUT<163>	-5270.0	1145.46	51.0	51.0
OUT<164>	-5202.0	1145.46	51.0	51.0
OUT<165>	-5134.0	1145.46	51.0	51.0
OUT<166>	-5066.0	1145.46	51.0	51.0
OUT<167>	-4998.0	1145.46	51.0	51.0
OUT<168>	-4930.0	1145.46	51.0	51.0
OUT<169>	-4862.0	1145.46	51.0	51.0
OUT<170>	-4794.0	1145.46	51.0	51.0
OUT<171>	-4726.0	1145.46	51.0	51.0
OUT<172>	-4658.0	1145.46	51.0	51.0
OUT<173>	-4590.0	1145.46	51.0	51.0
OUT<174>	-4522.0	1145.46	51.0	51.0
OUT<175>	-4454.0	1145.46	51.0	51.0
OUT<176>	-4386.0	1145.46	51.0	51.0
OUT<177>	-4318.0	1145.46	51.0	51.0
OUT<178>	-4250.0	1145.46	51.0	51.0
OUT<179>	-4182.0	1145.46	51.0	51.0
OUT<180>	-4114.0	1145.46	51.0	51.0
OUT<181>	-4046.0	1145.46	51.0	51.0
OUT<182>	-3978.0	1145.46	51.0	51.0

OUT<183>	-3910.0	1145.46	51.0	51.0
OUT<184>	-3842.0	1145.46	51.0	51.0
OUT<185>	-3774.0	1145.46	51.0	51.0
OUT<186>	-3706.0	1145.46	51.0	51.0
OUT<187>	-3638.0	1145.46	51.0	51.0
OUT<188>	-3570.0	1145.46	51.0	51.0
OUT<189>	-3502.0	1145.46	51.0	51.0
OUT<190>	-3434.0	1145.46	51.0	51.0
OUT<191>	-3366.0	1145.46	51.0	51.0
OUT<192>	-3298.0	1145.46	51.0	51.0
OUT<193>	-3230.0	1145.46	51.0	51.0
OUT<194>	-3162.0	1145.46	51.0	51.0
OUT<195>	-3094.0	1145.46	51.0	51.0
OUT<196>	-3026.0	1145.46	51.0	51.0
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OUT<367>	8602.0	1145.46	51.0	51.0
OUT<368>	8670.0	1145.46	51.0	51.0
vss!_1	**8803.79**	**1251.455**	**73.1**	**73.1 (die corner, stress relief pad)**
vss!_2	**8908.34**	**1151.24**	**73.1**	**73.1 (die corner, stress relief pad)**
VP	8916.415	997.73	51.0	51.0
VP_1	8916.415	929.73	51.0	51.0
vdd!	8916.415	752.93	51.0	51.0
vdd!_1	8916.415	684.93	51.0	51.0
gnd!	8916.415	508.13	51.0	51.0
gnd!_1	8916.415	440.13	51.0	51.0
vss!_3	8916.415	263.33	51.0	51.0
vss!_4	8916.415	195.33	51.0	51.0
gnd!_2	8916.415	0.0	51.0	51.0
vss!_5	8916.415	-195.33	51.0	51.0
vss!_6	8916.415	-263.33	51.0	51.0
gnd!_3	8916.415	-440.13	51.0	51.0
gnd!_4	8916.415	-508.13	51.0	51.0
vdd!_2	8916.415	-684.93	51.0	51.0
vdd!_3	8916.415	-752.93	51.0	51.0
VP_2	8916.415	-929.73	51.0	51.0
VP_3	8916.415	-997.73	51.0	51.0
vss!_7	**8908.34**	**-1151.24**	**73.1**	**73.1 (die corner, stress relief pad)**
vss!_8	**8803.79**	**-1251.455**	**73.1**	**73.1 (die corner, stress relief pad)**
OUT<369>	8670.0	-1145.46	51.0	51.0
OUT<370>	8602.0	-1145.46	51.0	51.0
OUT<371>	8534.0	-1145.46	51.0	51.0
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OUT<375>	8262.0	-1145.46	51.0	51.0
OUT<376>	8194.0	-1145.46	51.0	51.0
OUT<377>	8126.0	-1145.46	51.0	51.0
OUT<378>	8058.0	-1145.46	51.0	51.0
OUT<379>	7990.0	-1145.46	51.0	51.0
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OUT<381>	7854.0	-1145.46	51.0	51.0
OUT<382>	7786.0	-1145.46	51.0	51.0
OUT<383>	7718.0	-1145.46	51.0	51.0
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OUT<385>	7582.0	-1145.46	51.0	51.0
OUT<386>	7514.0	-1145.46	51.0	51.0
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OUT<402>	6426.0	-1145.46	51.0	51.0
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OUT<458>	2618.0	-1145.46	51.0	51.0
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VP_4	***1023.655***	***-1145.46***	***51.0***	***51.0***
vdd!_4	955.655	-1145.46	51.0	51.0
vdd!_5	887.655	-1145.46	51.0	51.0
gnd!_5	808.605	-1145.46	51.0	51.0
gnd!_6	740.605	-1145.46	51.0	51.0
vss!_9	661.555	-1145.46	51.0	51.0
vss!_10	593.555	-1145.46	51.0	51.0
STV2	512.465	-1145.46	51.0	51.0
TEST	440.215	-1145.46	51.0	51.0
DIR	367.965	-1145.46	51.0	51.0
vdd!_6	295.715	-1145.46	51.0	51.0
CLK	223.465	-1145.46	51.0	51.0
BLK	151.215	-1145.46	51.0	51.0
POL	78.965	-1145.46	51.0	51.0
gnd!_7	0.0	-1145.46	51.0	51.0
POL_1	-78.965	-1145.46	51.0	51.0
BLK_1	-151.215	-1145.46	51.0	51.0
CLK_1	-223.465	-1145.46	51.0	51.0
JUST	-295.715	-1145.46	51.0	51.0
DIR_1	-367.965	-1145.46	51.0	51.0
LTH	-440.215	-1145.46	51.0	51.0
STV1	-512.465	-1145.46	51.0	51.0
vss!_11	-593.555	-1145.46	51.0	51.0
vss!_12	-661.555	-1145.46	51.0	51.0
gnd!_8	-740.605	-1145.46	51.0	51.0
gnd!_9	-808.605	-1145.46	51.0	51.0
vdd!_7	-887.655	-1145.46	51.0	51.0
vdd!_8	-955.655	-1145.46	51.0	51.0
VP_5	***-1023.655***	***-1145.46***	***51.0***	***51.0***
OUT<1>	***-1122.0***	***-1145.46***	***51.0***	***51.0***
OUT<2>	-1190.0	-1145.46	51.0	51.0
OUT<3>	-1258.0	-1145.46	51.0	51.0
OUT<4>	-1326.0	-1145.46	51.0	51.0
OUT<5>	-1394.0	-1145.46	51.0	51.0
OUT<6>	-1462.0	-1145.46	51.0	51.0
OUT<7>	-1530.0	-1145.46	51.0	51.0
OUT<8>	-1598.0	-1145.46	51.0	51.0
OUT<9>	-1666.0	-1145.46	51.0	51.0
OUT<10>	-1734.0	-1145.46	51.0	51.0
OUT<11>	-1802.0	-1145.46	51.0	51.0
OUT<12>	-1870.0	-1145.46	51.0	51.0
OUT<13>	-1938.0	-1145.46	51.0	51.0
OUT<14>	-2006.0	-1145.46	51.0	51.0
OUT<15>	-2074.0	-1145.46	51.0	51.0
OUT<16>	-2142.0	-1145.46	51.0	51.0

OUT<17>	-2210.0	-1145.46	51.0	51.0
OUT<18>	-2278.0	-1145.46	51.0	51.0
OUT<19>	-2346.0	-1145.46	51.0	51.0
OUT<20>	-2414.0	-1145.46	51.0	51.0
OUT<21>	-2482.0	-1145.46	51.0	51.0
OUT<22>	-2550.0	-1145.46	51.0	51.0
OUT<23>	-2618.0	-1145.46	51.0	51.0
OUT<24>	-2686.0	-1145.46	51.0	51.0
OUT<25>	-2754.0	-1145.46	51.0	51.0
OUT<26>	-2822.0	-1145.46	51.0	51.0
OUT<27>	-2890.0	-1145.46	51.0	51.0
OUT<28>	-2958.0	-1145.46	51.0	51.0
OUT<29>	-3026.0	-1145.46	51.0	51.0
OUT<30>	-3094.0	-1145.46	51.0	51.0
OUT<31>	-3162.0	-1145.46	51.0	51.0
OUT<32>	-3230.0	-1145.46	51.0	51.0
OUT<33>	-3298.0	-1145.46	51.0	51.0
OUT<34>	-3366.0	-1145.46	51.0	51.0
OUT<35>	-3434.0	-1145.46	51.0	51.0
OUT<36>	-3502.0	-1145.46	51.0	51.0
OUT<37>	-3570.0	-1145.46	51.0	51.0
OUT<38>	-3638.0	-1145.46	51.0	51.0
OUT<39>	-3706.0	-1145.46	51.0	51.0
OUT<40>	-3774.0	-1145.46	51.0	51.0
OUT<41>	-3842.0	-1145.46	51.0	51.0
OUT<42>	-3910.0	-1145.46	51.0	51.0
OUT<43>	-3978.0	-1145.46	51.0	51.0
OUT<44>	-4046.0	-1145.46	51.0	51.0
OUT<45>	-4114.0	-1145.46	51.0	51.0
OUT<46>	-4182.0	-1145.46	51.0	51.0
OUT<47>	-4250.0	-1145.46	51.0	51.0
OUT<48>	-4318.0	-1145.46	51.0	51.0
OUT<49>	-4386.0	-1145.46	51.0	51.0
OUT<50>	-4454.0	-1145.46	51.0	51.0
OUT<51>	-4522.0	-1145.46	51.0	51.0
OUT<52>	-4590.0	-1145.46	51.0	51.0
OUT<53>	-4658.0	-1145.46	51.0	51.0
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OUT<55>	-4794.0	-1145.46	51.0	51.0
OUT<56>	-4862.0	-1145.46	51.0	51.0
OUT<57>	-4930.0	-1145.46	51.0	51.0
OUT<58>	-4998.0	-1145.46	51.0	51.0
OUT<59>	-5066.0	-1145.46	51.0	51.0
OUT<60>	-5134.0	-1145.46	51.0	51.0
OUT<61>	-5202.0	-1145.46	51.0	51.0
OUT<62>	-5270.0	-1145.46	51.0	51.0
OUT<63>	-5338.0	-1145.46	51.0	51.0
OUT<64>	-5406.0	-1145.46	51.0	51.0
OUT<65>	-5474.0	-1145.46	51.0	51.0
OUT<66>	-5542.0	-1145.46	51.0	51.0
OUT<67>	-5610.0	-1145.46	51.0	51.0
OUT<68>	-5678.0	-1145.46	51.0	51.0
OUT<69>	-5746.0	-1145.46	51.0	51.0
OUT<70>	-5814.0	-1145.46	51.0	51.0
OUT<71>	-5882.0	-1145.46	51.0	51.0
OUT<72>	-5950.0	-1145.46	51.0	51.0
OUT<73>	-6018.0	-1145.46	51.0	51.0
OUT<74>	-6086.0	-1145.46	51.0	51.0
OUT<75>	-6154.0	-1145.46	51.0	51.0
OUT<76>	-6222.0	-1145.46	51.0	51.0
OUT<77>	-6290.0	-1145.46	51.0	51.0
OUT<78>	-6358.0	-1145.46	51.0	51.0
OUT<79>	-6426.0	-1145.46	51.0	51.0
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OUT<81>	-6562.0	-1145.46	51.0	51.0
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OUT<84>	-6766.0	-1145.46	51.0	51.0
OUT<85>	-6834.0	-1145.46	51.0	51.0
OUT<86>	-6902.0	-1145.46	51.0	51.0
OUT<87>	-6970.0	-1145.46	51.0	51.0
OUT<88>	-7038.0	-1145.46	51.0	51.0
OUT<89>	-7106.0	-1145.46	51.0	51.0
OUT<90>	-7174.0	-1145.46	51.0	51.0
OUT<91>	-7242.0	-1145.46	51.0	51.0
OUT<92>	-7310.0	-1145.46	51.0	51.0
OUT<93>	-7378.0	-1145.46	51.0	51.0
OUT<94>	-7446.0	-1145.46	51.0	51.0
OUT<95>	-7514.0	-1145.46	51.0	51.0
OUT<96>	-7582.0	-1145.46	51.0	51.0
OUT<97>	-7650.0	-1145.46	51.0	51.0
OUT<98>	-7718.0	-1145.46	51.0	51.0
OUT<99>	-7786.0	-1145.46	51.0	51.0
OUT<100>	-7854.0	-1145.46	51.0	51.0
OUT<101>	-7922.0	-1145.46	51.0	51.0
OUT<102>	-7990.0	-1145.46	51.0	51.0
OUT<103>	-8058.0	-1145.46	51.0	51.0
OUT<104>	-8126.0	-1145.46	51.0	51.0
OUT<105>	-8194.0	-1145.46	51.0	51.0
OUT<106>	-8262.0	-1145.46	51.0	51.0
OUT<107>	-8330.0	-1145.46	51.0	51.0
OUT<108>	-8398.0	-1145.46	51.0	51.0

OUT<109>	-8466.0	-1145.46	51.0	51.0
OUT<110>	-8534.0	-1145.46	51.0	51.0
OUT<111>	-8602.0	-1145.46	51.0	51.0
OUT<112>	-8670.0	-1145.46	51.0	51.0
vss!_13	**-8803.79**	**-1251.455**	**73.1**	**73.1 (die corner, stress relief pad)**
vss!_14	**-8908.34**	**-1151.24**	**73.1**	**73.1 (die corner, stress relief pad)**
VP_6	-8916.415	-997.73	51.0	51.0
VP_7	-8916.415	-929.73	51.0	51.0
vdd!_9	-8916.415	-752.93	51.0	51.0
vdd!_10	-8916.415	-684.93	51.0	51.0
gnd!_10	-8916.415	-508.13	51.0	51.0
gnd!_11	-8916.415	-440.13	51.0	51.0
vss!_15	-8916.415	-263.33	51.0	51.0
vss!_16	-8916.415	-195.33	51.0	51.0
gnd!_12	-8916.415	0.0	51.0	51.0
vss!_17	-8916.415	195.33	51.0	51.0
vss!_18	-8916.415	263.33	51.0	51.0
gnd!_13	-8916.415	440.13	51.0	51.0
gnd!_14	-8916.415	508.13	51.0	51.0
vdd!_11	-8916.415	684.93	51.0	51.0
vdd!_12	-8916.415	752.93	51.0	51.0
VP_8	-8916.415	929.73	51.0	51.0
VP_9	-8916.415	997.73	51.0	51.0
vss!_19	**-8908.34**	**1151.24**	**73.1**	**73.1 (die corner, stress relief pad)**

8 Revision history

Table 11. Document revision history

Date	Revision	Changes
17-Aug-2011	1	Initial release.

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