AND8182/D

100 Watt Universal Input PFC Boost Using NCP1601A

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APPLICATION NOTE

INTRODUCTION

This application note presents a Power Factor Correction (PFC) boost regulator example circuit using NCP1601A in Figure 1 with the design steps and measurement. The measurement shows that the circuit has a greater than 0.9 Power Factor under the universal input (85 to 265 Vac). The NCP1601A is one of the latest ON Semiconductor low−power PFC products which can operate in both Discontinuous Conduction Mode (DCM) and Critical Mode (CRM). The DCM feature limits the maximum switching frequency for easier front−ended EMI filter design and the CRM feature limits the current stress on inductor, MOSFET and diode for better cost, size, and reliability.

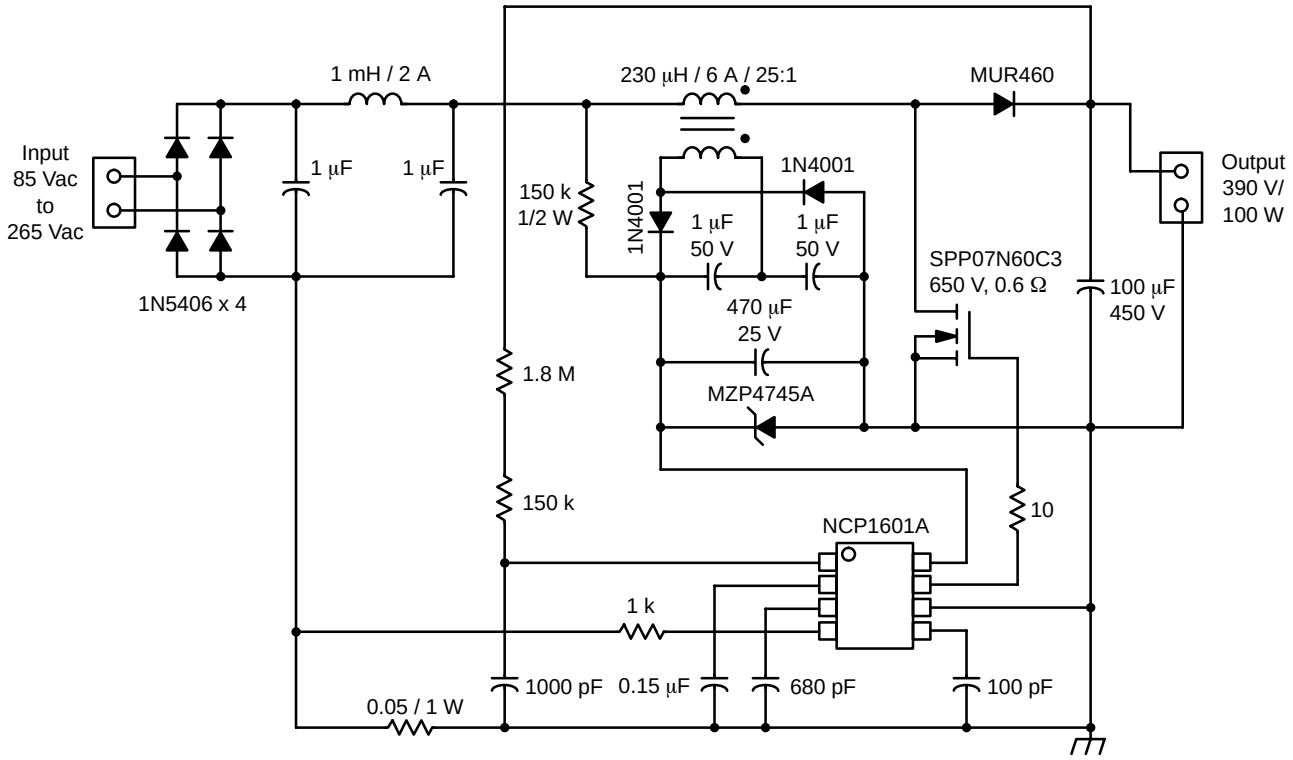

Figure 1. Application Schematic of the Example Circuit

Common low−power PFC method is usually presented in Critical Mode (CRM) which is with changing switching frequency. The CRM switching frequency can become dramatically very high at the zero−crossing moment of the sinusoidal waveform. Sometimes, the high switching frequency makes CRM not desirable due to EMI problem. However, CRM has an advantage over fixed−frequency DCM for lower peak current which is important so that CRM is preferable in the high current stress moment. As a result, the NCP1601 is developed to have both DCM and CRM. The converter using NCP1601 is intended to operate in CRM in the most stressful moment and in DCM in the zero−crossing moment. The mode of operation of NCP1601 is summarized in Figure 2.

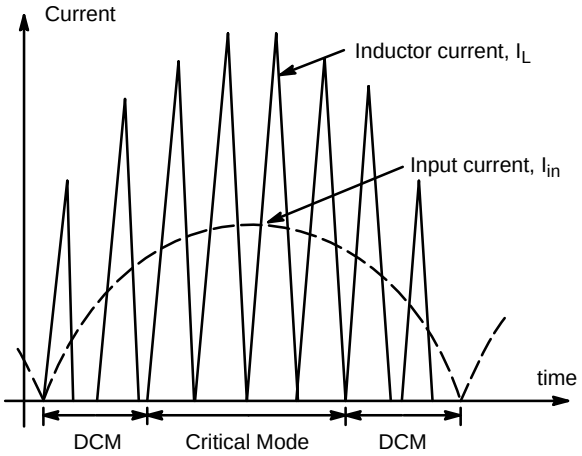

Figure 2. Mode of Operation of NCP1601

DESIGN STEPS

Step 1. Define the Specifications

Table 1. Specifications

Input	85 Vac to 265 Vac, 50 Hz
Output	100 W, 390 Vdc
Switching frequency	Around 100 kHz

The maximum overvoltage threshold is limited to 225 μA which corresponds to 225 μA ×1.95 MΩ + 5 V = 443.75 V when feedback resistor R_{FB} is 1.95 MΩ (1.8 MΩ + 150 kΩ) and a 5 V maximum offset of the feedback pin of the NCP1601. Hence, a 450 V output capacitor can be used in the output of the circuit. Then, the nominal output voltage is set at 390 V.

$$V_{out} = 200\ \mu \times 1.95\ M\Omega = 390\ V$$

Step 2. Bias Supply Design

A 1/2 W axial 150 kΩ resistor is used to charge up the V_{CC} capacitor in startup. The worst case power dissipation on this resistor is 0.47 W which is smaller than 1/2 W.

$$Power = \frac{V^2}{R} = \frac{265^2}{150 \times 10^3} = 0.47\ W$$

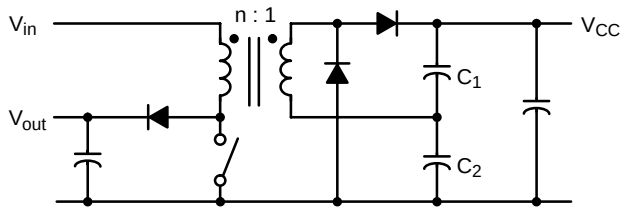

Figure 3. Auxiliary Winding Bias Supply.

The auxiliary winding bias supply in Figure 3 is to provide a V_{CC} bias voltage after startup. The V_{CC} needs to be higher than its minimum operating voltage $V_{CC(off)}$ (9 V typical). When the PFC stage MOSFET is on, the primary winding is with a voltage V_{in} and the secondary winding is with a voltage V_{in} / n. This voltage goes to capacitor C_1. When the PFC stage diode is on, the primary winding is with a voltage ($V_{out} - V_{in}$) and the secondary winding is with a voltage ($V_{out} - V_{in}$) / n. This voltage goes to capacitor C_2. As a result, the V_{CC} biasing voltage will be V_{out} / n which is almost constant and independent of the 50 Hz variation of the input voltage.

$$V_{CC} = V_{C1} + V_{C2} = \frac{V_{in}}{n} + \frac{V_{out} - V_{in}}{n}$$

$$= \frac{V_{out}}{n} > V_{CC(off)}$$

Hence, the auxiliary winding turn ratio n is selected as 25:1 so that V_{CC} is 15.6 V.

$$V_{CC} = \frac{V_{out}}{n} = \frac{390}{25} = 15.6\ V$$

A 470 μF V_{CC} capacitor is experimentally found to be enough for the circuit startup transient t_{start} = 893 ms in the worst case of 85 Vac input given that it consumes typical 2.5 mA for an UVLO margin 4.75 V in NCP1601A.

$$t_{start} = \frac{CdV}{I} = \frac{470 \times 10^{-6} \cdot 4.75}{2.5 \times 10^{-3}} = 893\ ms$$

For protection purpose, a clamping Zener MZP4745A is added to prevent any unwanted transient overvoltage damage.

It is noted that the circuit needs typical 11.4 sec to let the V_{CC} capacitor reach the starting threshold (13.75 typical) in the worst condition V_{in} = 85 Vac.

$$t_{start} = \frac{CdV}{I} = \frac{470 \times 10^{-6} \cdot 13.75}{85/15 \times 10^{-3}} = 11.4\ s$$

Step 3. Take an Assumption on Efficiency

The efficiency η is usually assumed to be 90%. Then, the input power P_{in} is 111 W. This input power will be frequently used in the next few design steps.

$$\eta = 90\%$$

$$P_{in} = \frac{P_{out}}{\eta} = \frac{100}{90\%} = 111\ W$$

Step 4. Calculate the Current Stress

The worst case input current rating happens when input is 85 Vac. The input RMS current I_{ac} is 1.31 Aac. The suffix ac denotes that it is RMS value. This current stress is mainly on the front−ended rectifier.

$$I_{ac} = \frac{P_{in}}{V_{ac}} = \frac{111}{85} = 1.31\ Aac$$

The instantaneous maximum current stress in the PFC stage will be 3.7 A in critical mode.

$$I_{pk} = 2\sqrt{2}\, I_{ac} = 3.7\ A$$

This current stress affects the component selections on the current sense resistor, MOSFET, diode, and inductor.

Step 5. Oscillator Capacitor Design

The switching frequency can be set by either oscillator mode or synchronization mode in the NCP1601. In this application, it is set at oscillator mode. Figure 34 in the NCP1601 data sheet shows that a 100 pF capacitor can set the frequency to 107 kHz. Actually, this frequency is only valid for the DCM operation because CRM is with a lower switching frequency. However, this frequency provides a reference on calculating the inductor for CRM in the next design step.

$$f = 107\ \text{kHz}$$

$$T = \frac{1}{f} = 9.35\ \mu\text{s}$$

Step 6. Inductor Design

The minimum CRM inductance $L_{(CRM)}$ at low line is obtained as follows:

$$L_{(CRM)} = \frac{V_{out} - V_{in}}{V_{out}} \frac{V_{in}}{I_{pk}} \frac{1}{f}$$

$$= \frac{390 - \sqrt{2}85}{390} \frac{\sqrt{2}85}{3.7} \frac{1}{107 \times 10^3} = 210\ \mu\text{H}$$

The maximum value of $L_{(CRM)}$ is at low line. Hence, a value greater than $L_{(CRM)}$ can make the circuit to operate in CRM. The inductor L is therefore set to be 230 μH. The switching frequency is 99 kHz and it is in CRM.

$$L = 230\ \mu\text{H}$$

$$\text{freq} = \frac{V_{out} - V_{in}}{V_{out}} \frac{V_{in}}{I_{pk}} \frac{1}{L}$$

$$= \frac{390 - \sqrt{2}85}{390} \frac{\sqrt{2}85}{3.7} \frac{1}{230 \times 10^{-6}} = 98\ \text{kHz} < 107\ \text{kHz}$$

Step 7. Ramp Capacitor Design

Maximum power can be obtained when $V_{control}$ = 1 V. Worst case is at low line 85 Vac.

$$C_{ramp} > \frac{P_{in}}{V_{ac}^2} \cdot 2LI_{ch}$$

$$= \frac{111}{85^2} \cdot 2 \cdot 230 \times 10^{-6} \cdot 100 \times 10^{-6} = 706\ \text{pF}$$

There is a typical 20 pF background capacitance on the ramp pin in the NCP1601. The C_{ramp} is selected to be as small as possible to limit the maximum power transfer. Marginally, an external 680 pF capacitor is good enough for this application.

$$C_{ramp} = 680\ \text{pF}$$

With this value of C_{ramp}, the control voltage $V_{control}$ in high line and low line condition are obtained.

In low line 85 Vac,

$$V_{control} = \frac{2LI_{ch}P_{in}}{C_{ramp}V_{ac}^2}$$

$$= \frac{2 \cdot 230 \times 10^{-6} \cdot 100 \times 10^{-6} \cdot 111}{(680 + 20) \times 10^{-12} \cdot 85^2} = 1.01\ \text{V}$$

In high line 265 Vac,

$$V_{control} = \frac{2LI_{ch}P_{in}}{C_{ramp}V_{ac}^2}$$

$$= \frac{2 \cdot 230 \times 10^{-6} \cdot 100 \times 10^{-6} \cdot 111}{(680 + 20) \times 10^{-12} \cdot 265^2} = 0.1\ \text{V}$$

Step 8. Check the Switching Periods to Ensure CRM in the Sinusoidal Peaks

In low line 85 Vac, the switching period ($t_1 + t_2$) and MOSFET on time (t_1) are as followed.

$$t_1 + t_2 = \frac{V_{out}}{V_{out} - V_{in}} \frac{C_{ramp}V_{control}}{I_{ch}}$$

$$= \frac{390}{390 - \sqrt{2}85} \frac{700 \times 10^{-12} \cdot 1.01}{100 \times 10^{-6}}$$

$$= 10.22\ \mu\text{s} > T$$

$$t_1 = \frac{C_{ramp}V_{control}}{I_{ch}} = \frac{700 \times 10^{-12} \cdot 1.01}{100 \times 10^{-6}} = 7.07\ \mu\text{s}$$

In high line 265 Vac, the switching period ($t_1 + t_2$) and MOSFET on time (t_1) are as followed.

$$t_1 + t_2 = \frac{V_{out}}{V_{out} - V_{in}} \frac{C_{ramp}V_{control}}{I_{ch}}$$

$$= \frac{390}{390 - \sqrt{2}265} \frac{700 \times 10^{-12} \cdot 0.1}{100 \times 10^{-6}}$$

$$= 17.92\ \mu\text{s} > T$$

$$t_1 = \frac{C_{ramp}V_{control}}{I_{ch}} = \frac{700 \times 10^{-12} \cdot 0.1}{100 \times 10^{-6}} = 0.7\ \mu\text{s}$$

As long as the switching period is larger than the DCM switching period T, the circuit operates in CRM and the maximum current stress is minimized.

Step 9. Current Sense Resistors Design

The settings of current sense resistor R_{CS} and sense resistor R_S defines the zero current threshold $I_{L(ZCD)}$ and overcurrent protection threshold $I_{L(OCP)}$ by the following two design equations.

$$I_{L(OCP)} = \frac{R_S \cdot 200\ \mu\text{A} - 3.2\ \text{mV}}{R_{CS}}$$

$$I_{L(ZCD)} = \frac{R_S \cdot 14\ \mu A - 7.5\ mV}{R_{CS}}$$

Because the $I_{L(ZCD)}$ has to be greater than zero, R_S has to be greater than 535.7 Ω which gives $I_{L(ZCD)} > 0$. When R_S is very close to 535.7 Ω (say R_S = 536 Ω), $I_{L(OCP)} / I_{L(ZCD)}$ = 26000 and $I_{L(ZCD)}$ can be very small with a finite $I_{L(OCP)}$. For example, if the maximum stress is 3.7 A, then R_{CS} is 28 mΩ and $I_{L(ZCD)}$ is 143 μA.

$$R_{CS} = \frac{R_S \cdot 200\ \mu A - 3.2\ mV}{I_{L(OCP)}}$$

$$= \frac{536 \cdot (200 \times 10^{-6}) - 0.0032}{3.7} = 0.028\ \Omega$$

$$I_{L(ZCD)} = \frac{R_S \cdot 14\ \mu A - 7.5\ mV}{R_{CS}}$$

$$= \frac{536 \cdot (14 \times 10^{-6}) - 0.0075}{0.028} = 143\ \mu A$$

However, tolerance exists in real world and the actual design can only be closed to this one.

When the value of R_{CS} is 0.05 Ω, its power dissipation P_d is 129 mW.

$$R_{CS} = 0.05\ \Omega$$

$$P_d = I^2_{ac} \cdot R_{CS} \cdot 1.5 = 1.31^2 \cdot 0.05 \cdot 1.5 = 129\ mW$$

In order to have $I_{L(OCP)}$ = 3.7 A, the R_S will be 941 Ω.

$$R_S = \frac{R_{CS} \cdot I_{L(OCP)} + 3.2\ mV}{200\ \mu A}$$

$$= \frac{0.05 \cdot 3.7 + 0.0032}{(200 \times 10^{-6})} = 941\ \Omega$$

941 Ω is not a standard size of a resistor. If the R_S is 1 kΩ then $I_{L(OCP)}$ and $I_{L(ZCD)}$ are also obtained.

$$R_S = 1\ k\Omega$$

$$I_{L(OCP)} = \frac{R_S \cdot 200\ \mu A - 3.2\ mV}{R_{CS}}$$

$$= \frac{1000 \cdot (200 \times 10^{-6}) - 0.0032}{0.05} = 3.936\ A$$

$$I_{L(ZCD)} = \frac{R_S \cdot 14\ \mu A - 7.5\ mV}{R_{CS}}$$

$$= \frac{1000 \cdot (14 \times 10^{-6}) - 0.0075}{0.05} = 130\ mA$$

Step 10. Output Capacitor Design

The choice of output capacitance is usually dictated by the required hold−up time or the acceptable output ripple voltage for a given application. As a rule of thumb, output capacitance is generally set at 1 μF/W. Hence, a 100 W application needs 100 μF output capacitance.

$$C = 100\ \mu F$$

The hold−up time t_{HOLD} which is the time a power supply needs to maintain its voltage with the specified range after a dropout of the line voltage.

$$C = \frac{2P_{out} \cdot t_{HOLD}}{V_{out\_min}^2 - V_{OP\_min}^2}$$

where V_{out_min} is the minimum value of the regulated output voltage at full load and V_{op_min} is the minimum input voltage of the driven load of the PFC. Because there is no particular specification on the hold−up time, this term is not further studied here.

The major output ripple component in a PFC circuit is usually its rectified line frequency because it cannot be easily filtered out by inductors and capacitors. The CCM or DCM operations mainly affect the switching frequency ripple which is always much smaller than the rectified line frequency ripple and hence generally neglected.

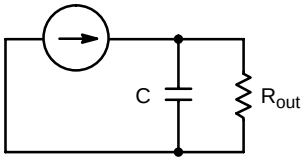

Figure 4. Low−Frequency Equivalent Circuit of the Output Stage

The low frequency output stage of a PFC stage can be simplified into Figure 4. The line frequency current source is a rectified sinusoidal (if only low frequency is considered) and its rms value $I_{out(rms)}$ is simply P_{out}/V_{out}. Hence, peak−to−peak value $I_{out(pk-pk)}$ is as follow:

$$I_{out(pk - pk)} = \sqrt{2}\, I_{out(rms)}$$

$$= \frac{\sqrt{2}\, P_{out}}{V_{out}} = \frac{\sqrt{2}\, 100}{390} = 0.363\ A$$

Now that the capacitor is the only energy storage media in the circuit in Figure 4 and the discharging time is one−fourth of the line frequency as shown in Figure 5.

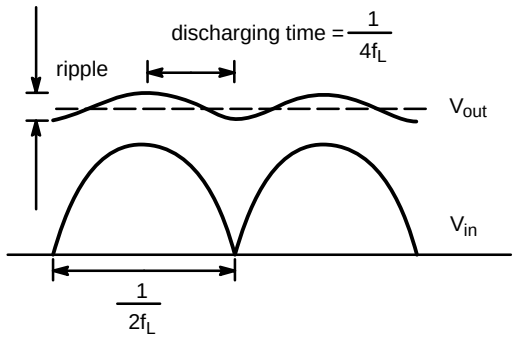

Figure 5. Output Voltage Ripple

Hence, the low frequency output ripple can be obtained as following:

$$dv = \frac{Idt}{C} = \frac{0.354 \cdot \frac{1}{4} \cdot \frac{1}{50}}{100 \times 10^{-6}} = 17.7\ V$$

For the sake of safety, 450 V rating output capacitor is always recommended if the nominal output voltage of the circuit is 400 V.

On the other hand, in a NCP1601 PFC circuit the instantaneous output voltage affects the instantaneous control voltage $V_{control}$. If the output voltage ripple is too high, it will make a large ripple on control voltage and the power factor can be dramatically reduced for highly dynamic control voltage.

Step 11. Input Filter Design

CRM and/or DCM PFC circuit needs an input filtering circuit to bypass the high frequency current so that the input current consists of the low frequency part only. The simplest filtering circuit is a capacitor C_F across the input lines in Figure 6. An input impedance Z_{in} is assumed to be with the input AC source but the value of the input impedance is usually unavailable and negligible in most of the application. Hence, a differential mode filtering inductor L_F is added in the calculation of the currents in Figure 6. This differential mode inductor usually exists in the form of common mode inductors.

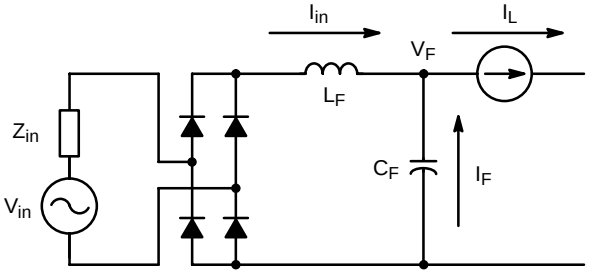

Figure 6. Filtering Capacitor Circuit

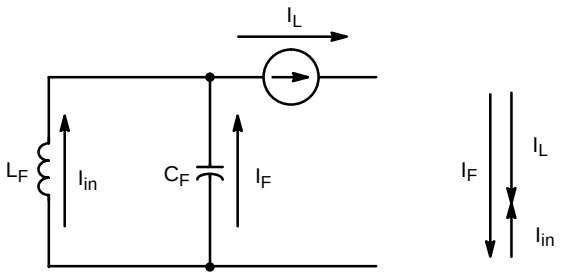

Figure 7. High−Frequency Equivalent Circuit and Phasor Diagram

The high frequency source in Figure 6 is the inductor current I_L. A high frequency equivalent circuit of Figure 6 is shown in Figure 7. Therefore, the phasor diagram is drawn and the percentage of the high frequency current (I_L) getting into the input side (I_{in}) is as follows.

$$\frac{I_{in}}{I_L} = \frac{1/(2\pi f C_F)}{2\pi f L_F - 1/(2\pi f C_F)} = \frac{1}{4\pi^2 f^2 L_F C_F - 1}$$

$$= \frac{1}{4\pi^2 \cdot \left(\frac{1}{11.10 \times 10^{-6}}\right)^2 \cdot 1000 \times 10^{-6} \cdot 1 \times 10^{-6} - 1}$$

$$= 0.31\%$$

when L_F = 1 mH and C_F = 1 μF.

On the other hand, the addition of the filtering capacitor C_F also draws a low frequency (i.e., line frequency f_L) current I_F in Figure 8. It increases the overall magnitude of the input current I_{in} for the same power I_L. The low frequency equivalent circuit of Figure 6 is shown in Figure 8. The equivalent resistance R_{eq} is the PFC circuit equivalent resistance which can be modeled to be purely resistive for its PFC property and R_{eq} is expressed as follows.

$$R_{eq} = \frac{V_{in}^2}{P_{in}} = \frac{V_{in}^2 \cdot \eta}{P_{out}}$$

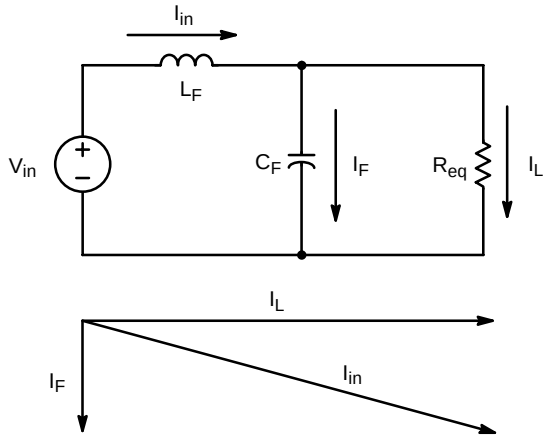

Figure 8. Low−Frequency Equivalent Circuit and Phasor Diagram

Therefore, the percentage of the increase of the input current due to the addition of the filtering capacitor is obtained.

$$\frac{I_{in}}{I_L} = \sqrt{1 + \left(\frac{R_{eq}}{1/(2\pi f_L C_F)}\right)^2} = \sqrt{1 + \left(\frac{V_{in}^2 \eta 2\pi f_L C_F}{P_{out}}\right)^2}$$

$$= \sqrt{1 + \left(\frac{265^2 \cdot 0.9 \cdot 2 \cdot \pi \cdot 50 \cdot 1 \times 10^{-6}}{100}\right)^2}$$

$$= 101.95\%$$

Step 12. Layout Design

Figures 9 and 10 illustrate the layout of the 100 W circuit. As one of the layout rules, the control circuit is located at a corner of the PCB to prevent any unwanted high frequency noise from the main power switching circuit. The NCP1601A is associated with a bunch of pF order capacitors which are very sensitive. The best way to handle them is to minimize the PCB trace distance. Hence, this bunch of pF capacitors are ideally located at the bottom layer of the NCP1601A.

The PCB trace connected to the low impedance current sense resistor is a major source of noise or error. It is recommended to minimize this PCB trace distance. Finally, the circuit is layout in a single PCB layer board. As a result, a 10 Ω resistor is added between the MOSFET gate and the NCP1601A output. This circuit path provides a large amount of high current ac noise so that the nearby trace on the output feedback is easily polluted. Hence, some surface mounted decoupling capacitors are located there for the noise.

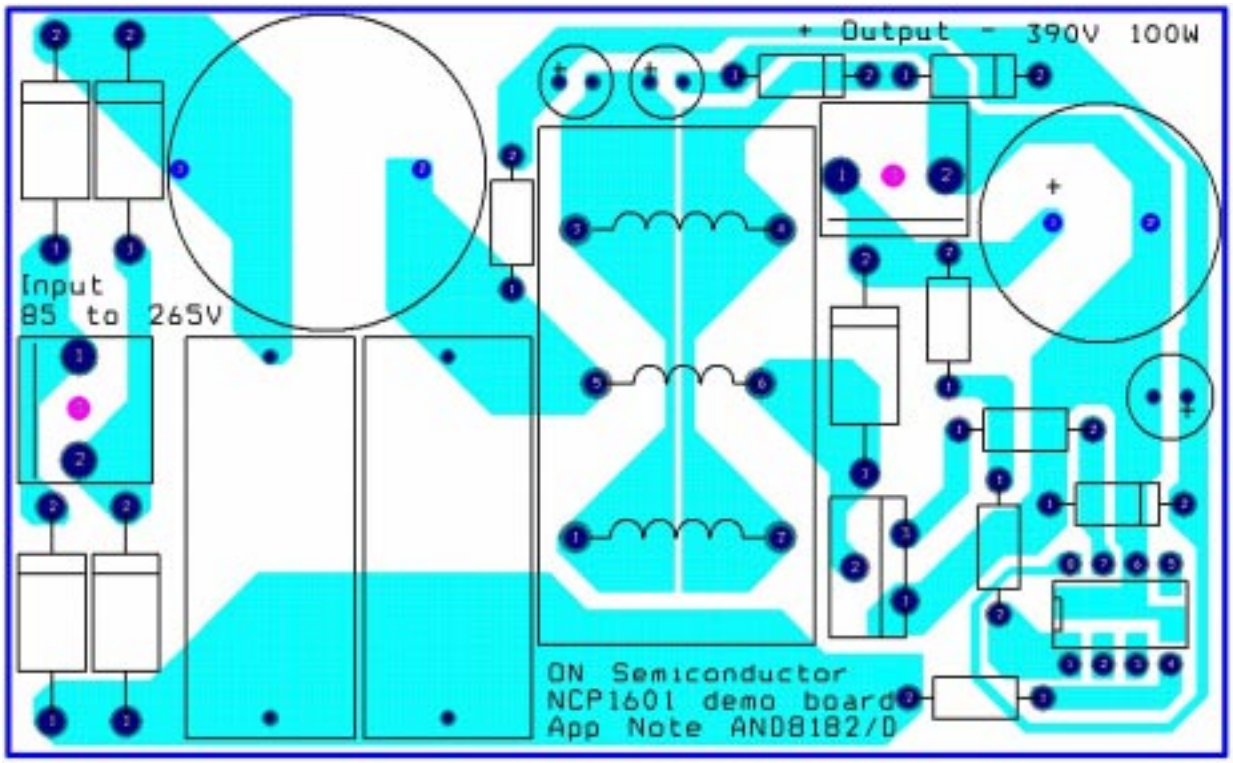

Figure 9. Demo Circuit Top Layer Layout

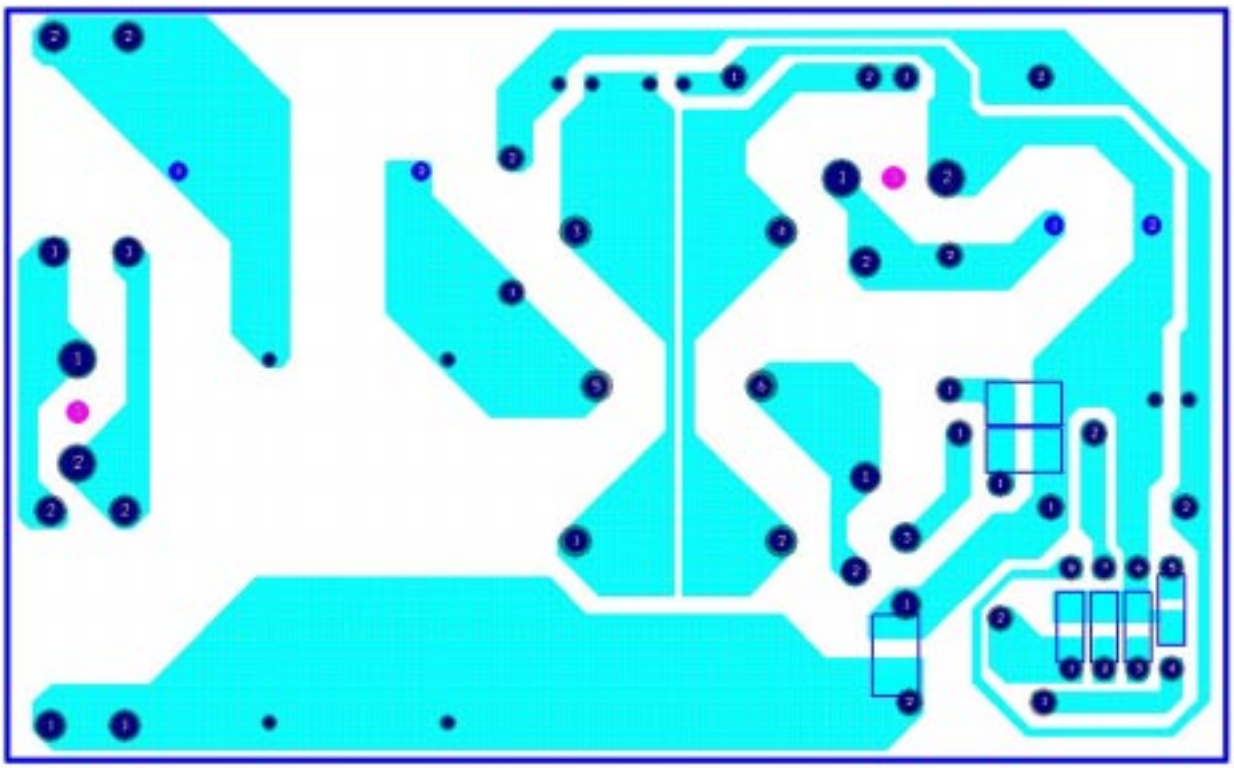

Figure 10. Demo Circuit Bottom Layer Layout

Step 13. Fine Tuning Capacitor on $V_{control}$ Pin

The unity power factor in the NCP1601 PFC circuit greatly relies on how steady the control voltage in the $V_{control}$ pin (pin 2). A large external capacitor on this pin can help to reduce the noise and dynamics of this voltage and give a decent power factor. However, if the capacitor is too large, it will reduce the dynamic response or startup transient of the circuit.

MEASUREMENT

The performance of the example PFC circuit is listed in Table 2. The waveforms with different input voltages are also shown in Figures 11 to 14. In Figures 11 to 14, the upper trace is the input current with 1 A/div. The center trace is the output voltage with 100 V/div. And the lower trace is the boost input voltage with 100V/div. The output voltage of the circuit is set by a (1.8 MΩ + 150 kΩ) × 200 μA = 390 V. There is roughly 374 V (96% × 390) to 390 V (100%) regulation window in the NCP1601. It explains the variation of the output voltage over the wide input range in Table 2. The THD can be improved by 2 or 3% if the front−ended 1 μF capacitor is reduced.

Table 2. Experimental Measurement of the Circuit.

Input	Output	Efficiency	PF/ THD
85 Vac 108.2 W	370.5 V 100.8 W	93.17%	0.995 / 8.3%
110 Vac 107.9 W	384.8 V 101.2 W	93.83%	0.991 / 12.8%
120 Vac 105.8 W	385.2 V 99.8 W	94.33%	0.990 / 11.3%
180 Vac 104.6 W	391.2 V 99.8 W	95.41%	0.975 / 11.9%
220 Vac 104.7 W	394.2 V 100.1 W	95.63%	0.952 / 16.7%
230 Vac 104.4 W	394.8 V 100.3 W	96.05%	0.945 / 21.1%
265 Vac 104.6 W	400.9 V 100.5 W	96.08%	0.901 / 38.9%

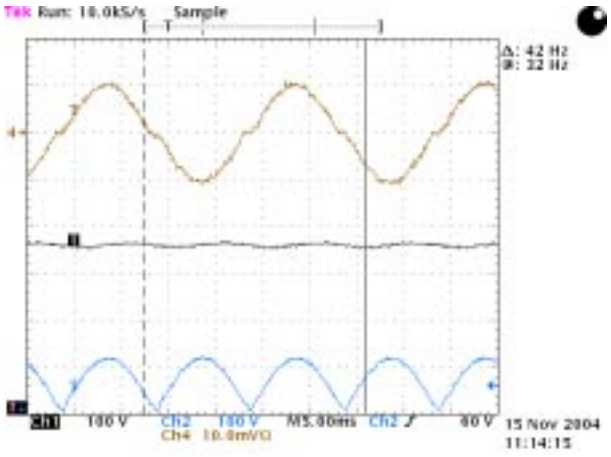

Figure 11. 85 Vac Input Voltage

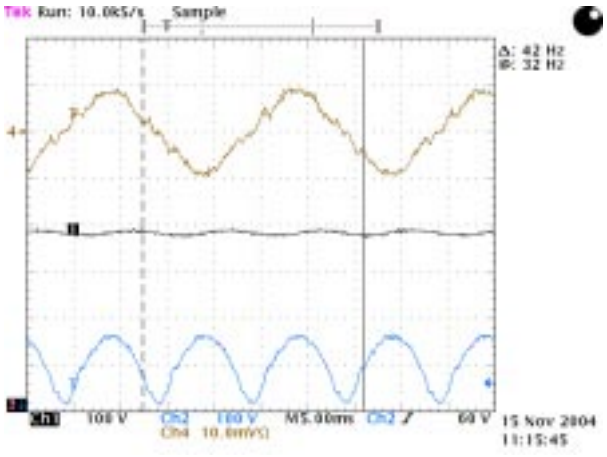

Figure 12. 115 Vac Input Voltage

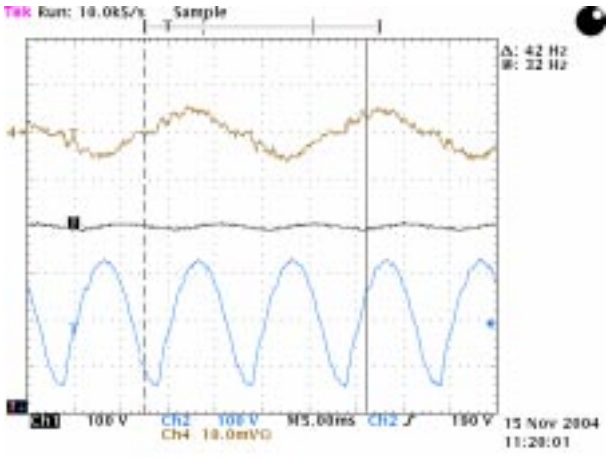

Figure 13. 230 Vac Input Voltage

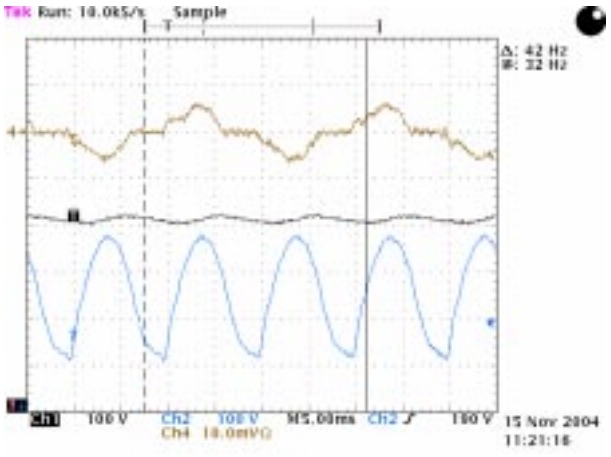

Figure 14. 265 Vac Input Voltage

In order to illustrate the capability of both DCM and CRM operation of the NCP1601, Figures 15 to 17 are taken. The upper trace of the figures is the boost input voltage with 100 V/div. The lower trace is the voltage across the 0.05 Ω current sense resistor with 50 mV/div so that the inductor current and the mode of operation are indirectly shown. Figure 15 shows the traces with 2 ms time base so that the maximum and minimum value of the boost input voltage is observed in this time base but the voltage across the current sense resistor is too noisy to study. Figure 16 shows the moment when the boost input voltage is the maximum. It illustrates that the circuit is in CRM operation in this moment. Figure 17 shows the moment when the boost input voltage is the minimum. It illustrates that the circuit is in DCM operation.

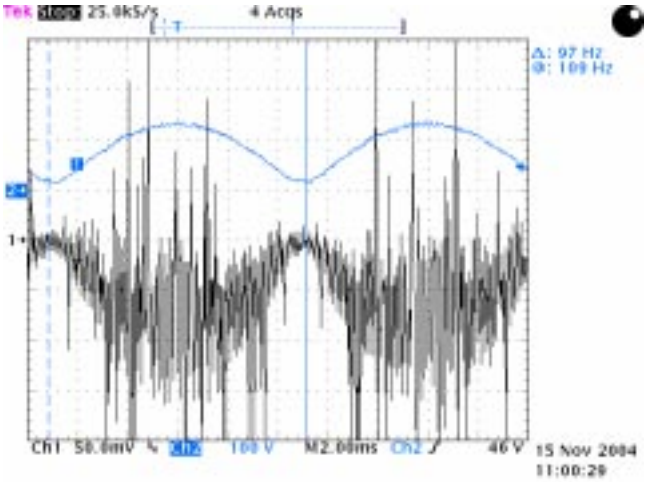

Figure 15. Current Sense Resistor Voltage

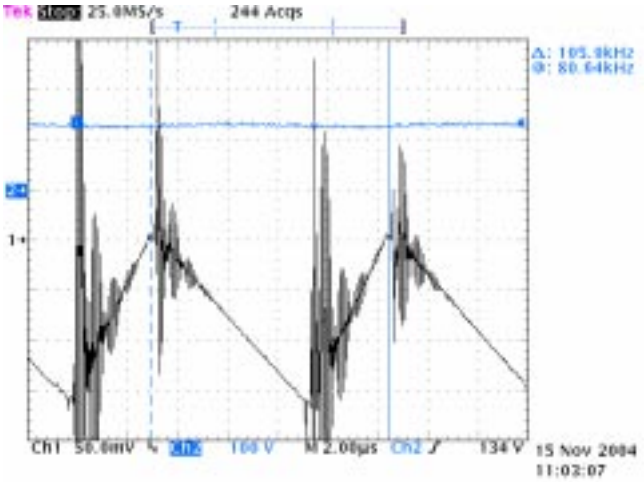

Figure 16. CRM Operation in Near the Peak

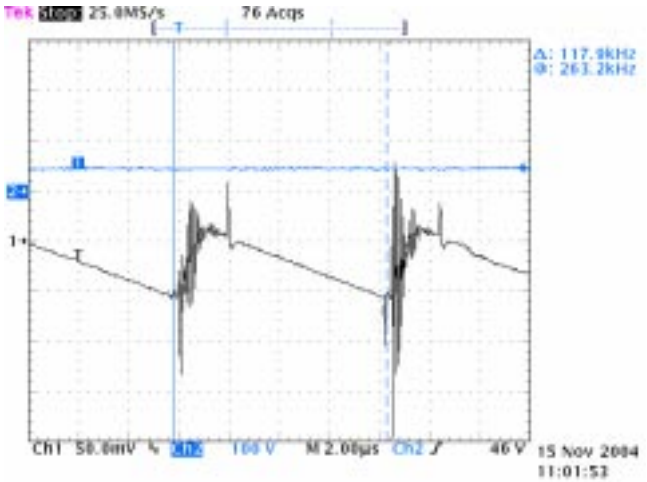

Figure 17. DCM Operation in the Zero Crossing

CONCLUSION

A 100 W example circuit using NCP1601A is presented. The design steps and measurement are covered. It is noted that the NCP1601 can perform a decent power factor correction and efficiency in CRM and DCM so that it is suitable for low power PFC applications. Major equations for the NCP1601 design are listed in appendix for reference.

Appendix I − Bill of Material of the NCP1601 100 W / 390 V Example Circuit

Qty	Part No.	Description	Manufacturer
1	NCP1601A	PFC Controller	ON Semiconductor
4	1N5406	Standard Diode, 4 A 600 V	ON Semiconductor
2	1N4001	Standard Diode,1 A 50 V	ON Semiconductor
1	MUR460	Fast Recovery Diode, 4 A 600 V	ON Semiconductor
1	MZP4745A	Zener Diode, 16 V 5%	ON Semiconductor
1	PCV−2−105−02	Inductor, 1000 μH / 2 A	Coilcraft
1	CTX22−16885	Custom Transformer, L_p = 230 μH / 6 A, 25:1:1	Cooper Coiltronics
1	SPP07N60C3	650 V, 0.6 Ω TO−220AB N−Channel MOSFET	Infineon
2	RE105	Noise Suppression Capacitor	Okaya
2	50MH71M4X7	Aluminum Electrolytic Capacitor, 1 μF 50 V	Rubycon
1	UHD1E471MPD	Aluminum Electrolytic Capacitor, 470 μF 25 V	Nichicon
1	450AXW100M18X40	Aluminum Electrolytic Capacitor, 100 μF 450 V	Rubycon
1	VJ1206A101KXAA	1206 SMD Capacitor, 100 pF	Vishay
1	VJ1206Y154KXXA	1206 SMD Capacitor, 0.15 μF	Vishay
1	VJ1206A681KXAA	1206 SMD Capacitor, 680 pF	Vishay
1	VJ1206A102KXAA	1206 SMD Capacitor, 1000 pF	Vishay
1	WSL2010−R0500−F	SMD Resistor, 0.05 Ω 1 W 1%	Vishay Dale
1		Axial Resistor, 150 kΩ 1/2 W	
1		Axial Resistor, 1.8 MΩ 1/4 W	
1		Axial Resistor, 150 kΩ 1/4 W	
1		Axial Resistor, 1 kΩ 1/4 W	
1		Axial Resistor, 10 Ω 1/4 W	
2	26−60−4030 or 009652038	Male Header	Molex

Appendix II – Summary of Equations in NCP1601 Boost PFC

Description	Critical Mode (CRM)	Discontinuous Mode (DCM)
Boost converter	$\frac{V_{out}}{V_{in}} = \frac{t_1 + t_2}{t_2}$ $\rightarrow \frac{V_{out} - V_{in}}{V_{out}} = \frac{t_1}{t_1 + t_2}$	$\frac{V_{out}}{V_{in}} = \frac{t_1 + t_2}{t_2}$ $\rightarrow \frac{V_{out} - V_{in}}{V_{out}} = \frac{t_1}{t_1 + t_2}$
Input current averaged by filter capacitor	$I_{in} = \frac{I_{pk}}{2}$	$I_{in} = \frac{t_1 + t_2}{T}\frac{I_{pk}}{2}$
Voltage for on time V_{ton}	$V_{ton} = V_{control}$	$V_{ton} = \frac{T}{t_1 + t_2}V_{control}$
MOSFET on−time t_1	$t_1 = \frac{LI_{pk}}{V_{in}}$, or $t_1 = \frac{C_{ramp}V_{control}}{I_{ch}}$ $\rightarrow$ t_1 is constant for unity PFC $\rightarrow$ $V_{control}$ is constant for unity PFC	$t_1 = \frac{LI_{pk}}{V_{in}}$, or $t_1 = \sqrt{\frac{V_{out} - V_{in}}{V_{out}}T\frac{C_{ramp}V_{control}}{I_{ch}}}$ $\rightarrow$ t_1 ($t_1 + t_2$) is constant for unity PFC $\rightarrow$ $V_{control}$ is constant for unity PFC
Switching period	$t_1 + t_2 = \frac{V_{out}}{V_{out} - V_{in}}\frac{C_{ramp}V_{control}}{I_{ch}}$, or $t_1 + t_2 = \frac{V_{out}}{V_{out} - V_{in}}\frac{LI_{pk}}{V_{in}}$	$t_1 + t_2 = \frac{T}{t_1}\frac{C_{ramp}V_{control}}{I_{ch}}$, or $t_1 + t_2 = \sqrt{\frac{V_{out}}{V_{out} - V_{in}}T\frac{C_{ramp}V_{control}}{I_{ch}}}$
Minimum Inductor for CRM	$L > L_{(CRM)} = \frac{V_{out} - V_{in}}{V_{out}}\frac{V_{in}}{I_{pk}}\frac{1}{f}$	Same as CRM
Input impedance	$Z_{in} = \frac{2LI_{ch}}{C_{ramp}V_{control}}$	Same as CRM
Input power	$P_{in} = \frac{V_{ac}^2 C_{ramp}V_{control}}{2LI_{ch}}$	Same as CRM
Output power	$P_{out} = \eta P_{in} = \frac{\eta V_{ac}^2 C_{ramp}V_{control}}{2LI_{ch}}$	Same as CRM
Maximum input power when $V_{control}$ = 1 V	$P_{in\_max} = \frac{V_{ac}^2 C_{ramp}}{2LI_{ch}}$	Same as CRM
Minimum ramp capacitor when $V_{control}$ = 1 V	$C_{ramp} > \frac{P_{in}}{V_{ac}^2} \cdot 2LI_{ch}$	Same as CRM
Control voltage $V_{control}$	$V_{ctrl} = \frac{2LI_{ch}P_{in}}{C_{ramp}V_{ac}^2}$	Same as CRM

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