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www.onsemi.com

Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

FAIRCHILD SEMICONDUCTOR®

October 2009

MM74HCT14
Hex Inverting Schmitt Trigger

Features

- Typical Propagation Delay: 13ns
- Wide Power Supply Range: 4.5V–5.5V
- Low Quiescent Current: 10µA Maximum
- Low Input Current: 1µA Maximum
- Fanout of 10 LS-TTL Loads
- Typical Hysteresis Voltage: 0.6V at V_{CC} = 4.5V
- TTL, LS Pin-out and Input Threshold Compatible

Description

The MM74HCT14 utilizes advanced silicon-gate CMOS technology to achieve the low power dissipation and high noise immunity of standard CMOS, as well as the capability to drive 10 LS-TTL loads.

The 74HCT logic family is functionally and pinout-compatible with the standard 74LS logic family. Inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Ordering Information

Part Number	Operating Temperature Range	Eco Status	Package	Packing Method
MM74HCT14M	-40°C to +85°C	RoHS	14-Lead, Small-Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150in Narrow	Tube
MM74HCT14MX	-40°C to +85°C	RoHS	14-Lead, Small-Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150in Narrow	Tape & Reel
MM74HCT14SJ	-40°C to +85°C	RoHS	14-Lead, Small-Outline Package (SOP), EIAJ Type II, 5.3mm Wide	Tube
MM74HCT14SJX	-40°C to +85°C	RoHS	14-Lead, Small-Outline Package (SOP), EIAJ Type II, 5.3mm Wide	Tape & Reel
MM74HCT14MTC	-40°C to +85°C	RoHS	14-Lead, Thin-Shrink Small-Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide	Tube
MM74HCT14MTCX	-40°C to +85°C	RoHS	14-Lead, Thin-Shrink Small-Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide	Tape & Reel
MM74HCT14SN	-40°C to +85°C	RoHS	14-Lead, Plastic Dual-Inline Package (PDIP), JEDEC MS-001, 0.300in Wide	Tube

For Fairchild's definition of Eco Status, please visit: http://www.fairchildsemi.com/company/green/rohs_green.html.

Connection Diagram

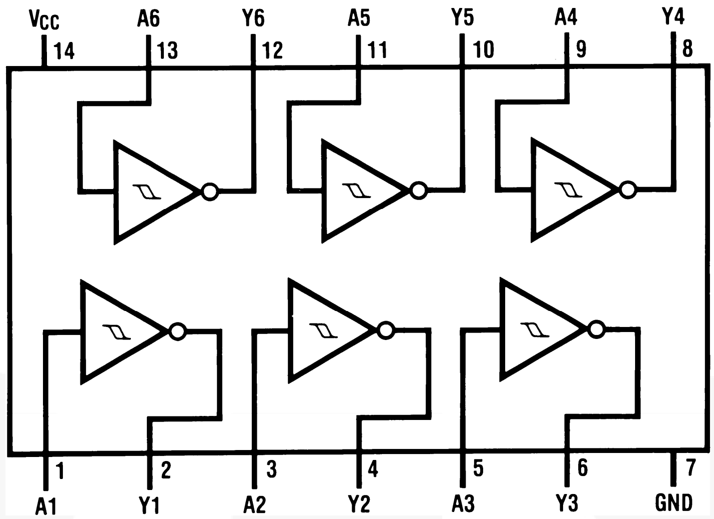


Figure 1. Pin Assignments

Schematic Diagram

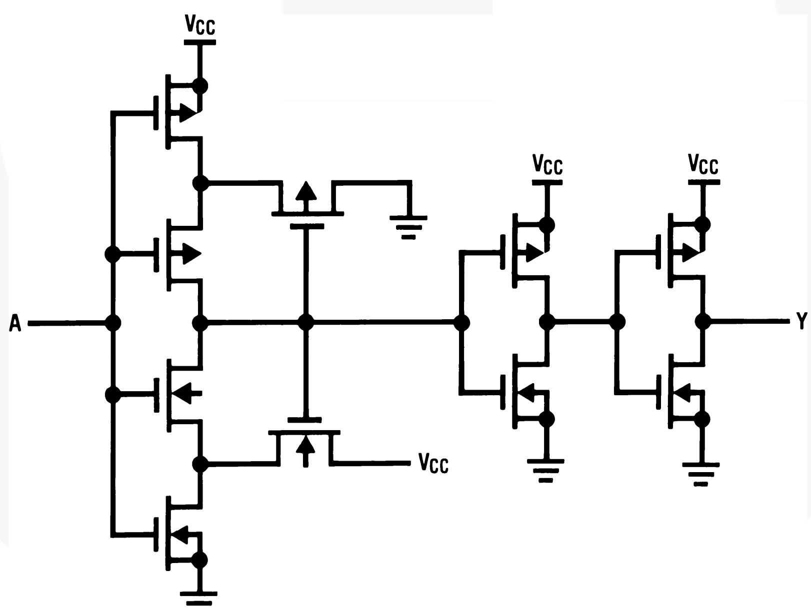


Figure 2. Schematic

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. Unless otherwise specified, all voltages are referenced to ground.

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	–0.5	+7.0	V
V_{IN}	DC Input Voltage	–1.5	V_{CC} +1.5	V
V_{OUT}	DC Output Voltage	–0.5	V_{CC} +0.5	V
I_K, I_{OK}	Clamp Diode Current		±20	mA
I_{OUT}	DC Output Current, Per Pin		±25	mA
I_{CC}	DC V_{CC} or GND Current, Per Pin		±50	mA
T_{STG}	Storage Temperature Range	–65	+150	°C
T_L	Lead Temperature (Soldering 10 Seconds)		+260	°C

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.5	V
V_{IN}, V_{OUT}	DC Input or Output Voltage	0	V_{CC}	V
T_A	Operating Temperature Range	–40	+85	°C

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC}	T_A=+25°C		T_A=-40°C to +85°C	Units
				Typ.	Guaranteed Limits		
V_{T+}	Positive-Going Threshold Voltage	Minimum	4.5	1.5	1.2	1.2	V
			5.5	1.7	1.4	1.4	
		Maximum	4.5	1.5	1.9	1.9	
			5.5	1.7	2.1	2.1	
V_{T-}	Negative-Going Threshold Voltage	Minimum	4.5	0.9	0.5	0.5	V
			5.5	1.0	0.6	0.6	
		Maximum	4.5	0.9	1.2	1.2	
			5.5	1.0	1.4	1.4	
V_H	Hysteresis Voltage	Minimum	4.5	0.6	0.4	0.4	V
			5.5	0.7	0.4	0.4	
		Maximum	4.5	0.6	1.4	1.4	
			5.5	0.7	1.5	1.5	
V_{OH}	Minimum HIGH Level Output Voltage	$V_{IN} = V_{IL}$, $\lvert I_{OUT} \rvert$ = 20µA	4.5	V_{CC}	V_{CC} – 0.1	V_{CC} – 0.1	V
		$V_{IN} = V_{IL}$, $\lvert I_{OUT} \rvert$ = 4.0mA	4.5	4.20	3.98	3.84	
		$V_{IN} = V_{IL}$, $\lvert I_{OUT} \rvert$ = 4.8mA	5.5	5.20	4.98	4.98	
V_{OL}	Maximum LOW Level Voltage	$V_{IN} = V_{IL}$, $\lvert I_{OUT} \rvert$ = 20µA	4.5	0	0.1	0.1	V
		$V_{IN} = V_{IL}$, $\lvert I_{OUT} \rvert$ = 4.0mA	4.5	0.2	0.26	0.33	
		$V_{IN} = V_{IL}$, $\lvert I_{OUT} \rvert$ = 4.8mA	5.5	0.2	0.26	0.33	
I_{IN}	Maximum Input Current	$V_{IN} = V_{CC}$ or GND, V_{IH} or V_{IL}	5.5		±0.1	±1.0	µA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND, I_{OUT} = 0µA	5.5		1.0	10.0	µA
		V_{IN} = 2.4V or 0.5V			2.4	2.4	mA

AC Electrical Characteristics

V_{CC} = 5V, T_A = 25°C, C_L = 15pF, t_r = t_f = 6ns.

Symbol	Parameter	Typ.	Guaranteed Limit	Unit
t_{PHL}, t_{PLH}	Maximum Propagation Delay	10	18	ns

AC Electrical Characteristics

Unless otherwise specified, V_{CC} = 5V±10%, C_L = 50pF, t_r = t_f = 6ns.

Symbol	Parameter	Conditions	T_A=+25°C		T_A=-40°C to +85°C	Units
			Typ.	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay			20	25	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		9	15	19	ns
C_{PD}	Power Dissipation Capacitance(1)	Per Gate		25		pF
C_{IN}	Maximum Input Capacitance		5	10	10	pF

Note:

1. C_{PD} determines the no-load dynamic power consumption, $P_D = C_{PD} V_{CC}2 f+I_{CC} V_{CC}$, and the no-load dynamic current consumption, $I_S = C_{PD} V_{CC} f+I_{CC}$.

Typical Applications

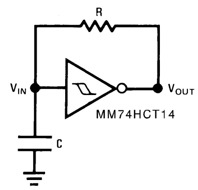


Figure 3. Low Power Oscillator

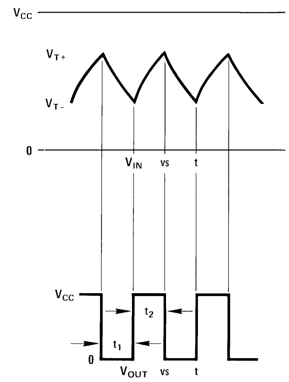
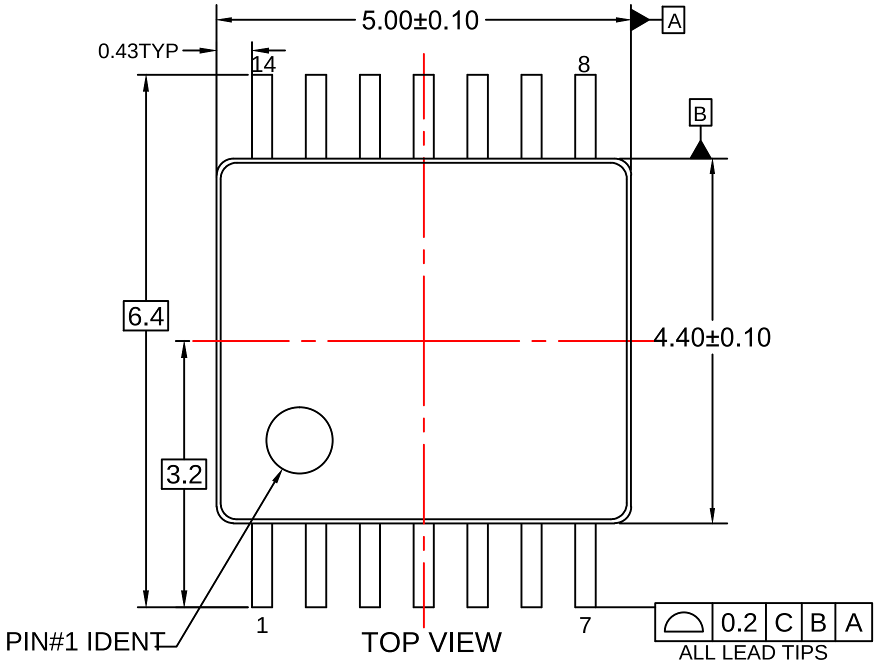


Figure 4. Oscillator Input and Output Waveforms

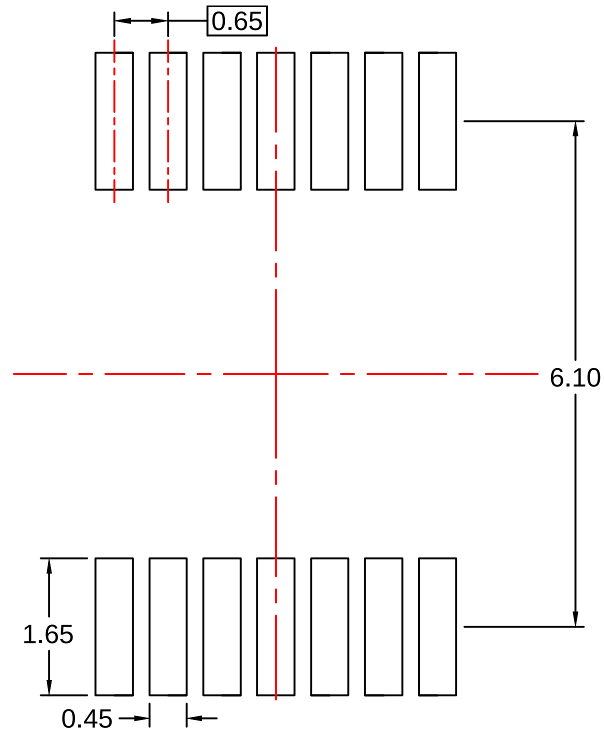
The following equations assume $t_1+t_2 >> t_{pd0}+t_{pd1}$:

$$t_2 \approx RCln\frac{V_{CC} - V_{T-}}{V_{CC} - V_{T+}} \quad (1)$$

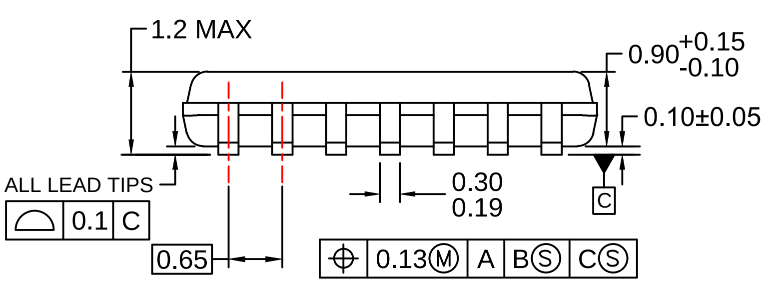
$$f \approx \frac{1}{RCln\frac{V_{T+}\left(V_{CC} - V_{T-}\right)}{V_{T-}\left(V_{CC} - V_{T+}\right)}} \quad (2)$$



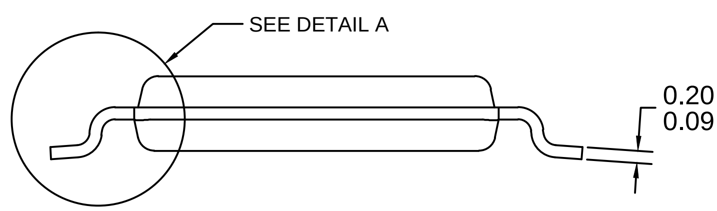
TOP VIEW

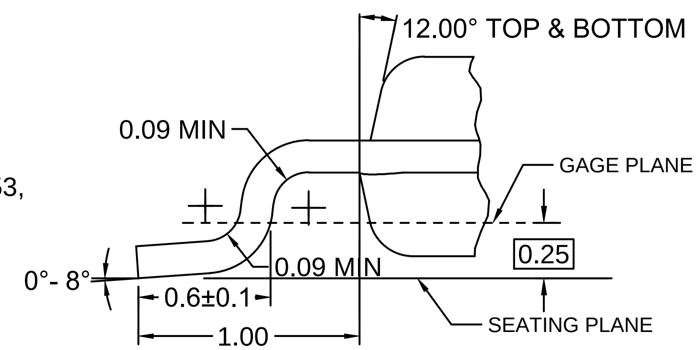


RECOMMENDED LAND PATTERN



FRONT VIEW





DETAIL A

NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6

B. DIMENSIONS ARE IN MILLIMETERS.

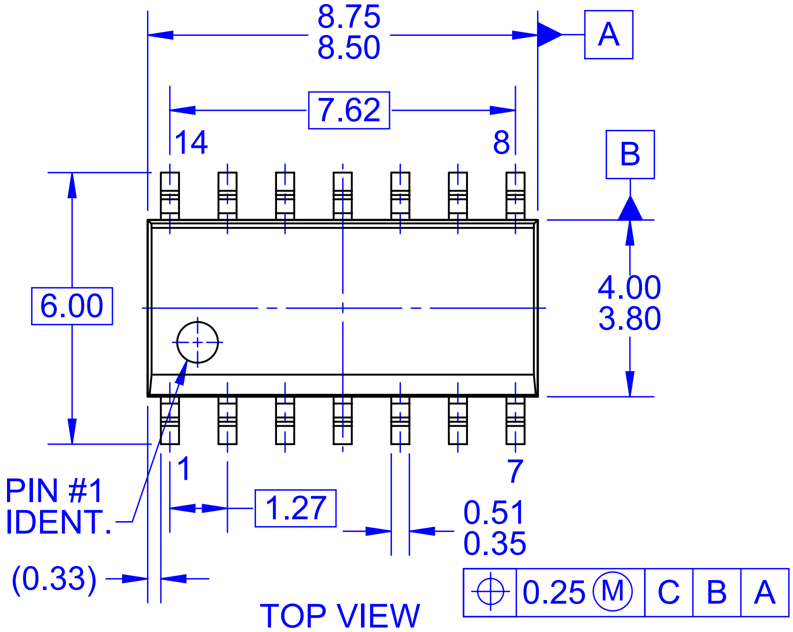
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS

D. DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 2009.

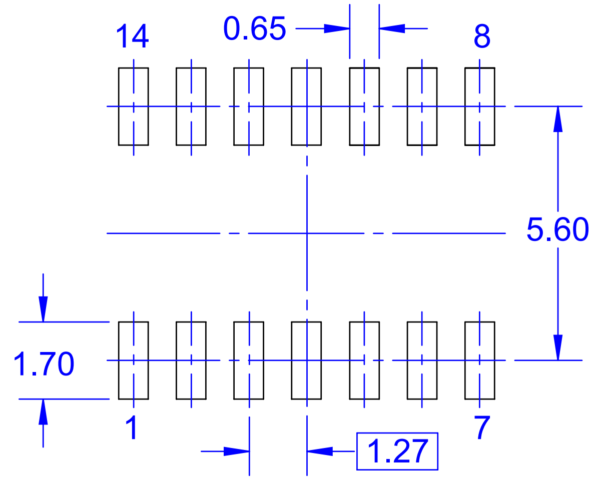
E. LANDPATTERN STANDARD: SOP65P640X110-14M.

F. DRAWING FILE NAME: MKT-MTC14rev7.

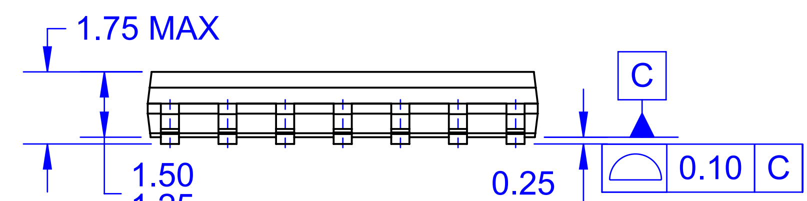
FAIRCHILD



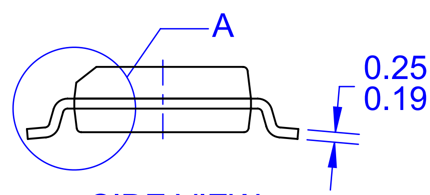
TOP VIEW



LAND PATTERN RECOMMENDATION



FRONT VIEW

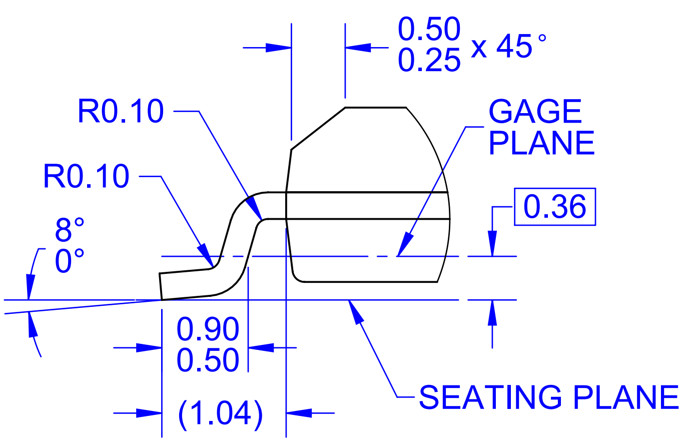


SIDE VIEW

NOTES:

A. CONFORMS TO JEDEC MS-012, VARIATION AB, ISSUE C
B. ALL DIMENSIONS ARE IN MILLIMETERS
C. DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS
D. LAND PATTERN STANDARD: SOIC127P600X145-14M
E. CONFORMS TO ASME Y14.5M, 2009
D. DRAWING FILENAME: MKT-M14Arev14

FAIRCHILD ™



DETAIL A
SCALE 16 : 1

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