

M41T56C64

Serial Real Time Clock with 56 bytes of NVRAM + 64 Kbit (8192 bit x 8) EEPROM

Feature summary

- 5V ±10% supply voltage
- I²C bus compatible
- Operating temperature of -40 to 85°C
- Packaging includes:
 - 18-lead SOIC (with embedded crystal)
- RoHS compliant

Serial RTC features

- Counters for seconds, minutes, hours, day, date, month, years, and century
- Embedded crystal package
- Software clock calibration
- Automatic power-fail detect and switch circuitry
- 56 bytes of general purpose SRAM
- Ultra-low battery supply current of 450n/.
- Automatic leap year compensation
- Special software program กเละ!a output
- Two-wire I²C seriol interface supports 100kHz protocol

Serial EEPKOM features

- 8192 bytes of general ວັນຖະວຣອ EEPROM (ກາວເອ than 1e6 Grase/write cycles)
- ► Two-wire I²C seria! interface supports 400kHz protocol
- Byte ลกน์ page write (up to 32 bytes)
- More than 40 year data retention
- Self-timed programming cycle

Embedded crystal



SOX18(MY) 18-pin (300mii) SC(C Contents M41T56C64

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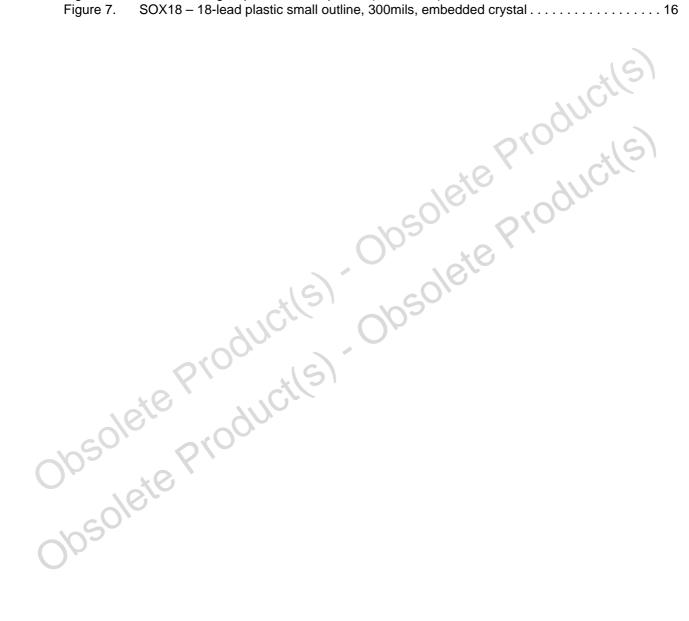
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Summary description 1

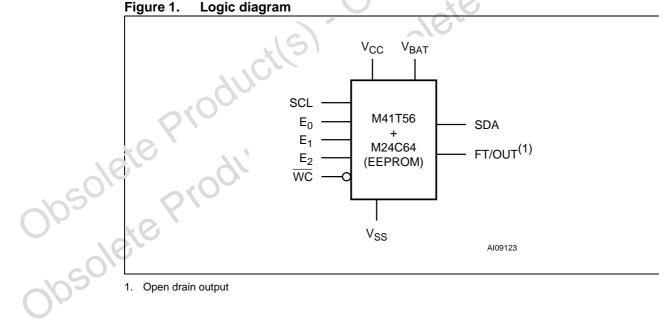
The M41T56C64 is a low power, Serial Real Time Clock with 56 bytes of NVRAM plus a 64Kb EEPROM (see Figure 3). A built-in 32,768Hz oscillator (crystal controlled) and the first 8 bytes of the RAM are used for the clock/calendar function and are configured in binary coded decimal (BCD) format. Addresses and data are transferred serially via a two-line, bidirectional bus. The built-in address register is incremented automatically after each WRITE or READ data byte.

The M41T56C64 clock has a built-in power sense circuit which detects power failures and automatically switches to the battery supply during power failures. The energy needed to sustain the RAM and clock operations can be supplied from a small lithium coin cell.

Typical data retention time for the Serial RTC is in excess of 10 years with a 50rr A'1, 3V lithium cell. The M41T56C64 is supplied in an 18-lead Plastic SOIC package

1.1 **Calibration**

As the crystal is molded together with the silicon in this package, ST can program the appropriate calibration value necessary to achieve ±5 p.o.~ accuracy at 25°C after two SMT reflows (see Figure 4). This calibration value will be written into address 1550h of the EEPROM. This clock accuracy can then be que ranteed to drift no more than ±3 ppm the first year, and ±1 ppm for each following year at e to crystal aging.



Pin settings M41T56C64

Pin settings 2

Pin description 2.1

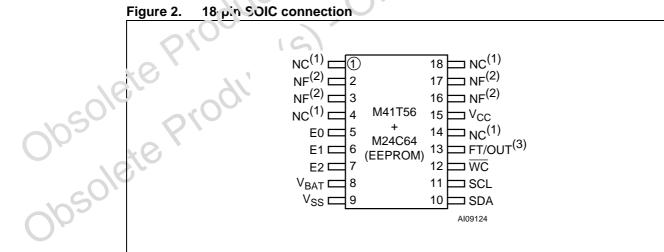
Table 1. Signal names

FT/OUT (1)	Frequency test / output driver (open drain)
SDA	Serial data address input / output
SCL	Serial clock
WC	Write control
E0, E1, E2	Chip enables
V_{BAT}	Battery supply voltage
V _{CC}	Supply voltage
V _{SS}	Ground
NC ⁽²⁾	No connect
NF ⁽³⁾	No function

- 1. Open drain output
- 2. No connect (NC) pins should be tied to VSS.
- No function (NF) pins should be tied to V_S; Pir s ? and 3, and pins 16 and 17 are internally shorted

Pin connections 2.2

18 pin SOIC connection Figure 2.



- 1. No connect (NC) pins should be tied to V_{SS}
- No function (NF) pins should be tied to V_{SS}. Pins 2 and 3, and pins 16 and 17 are internally shorted
- 3. Open drain output

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M41T56C64 Application

3 Application

Figure 3. Block diagram

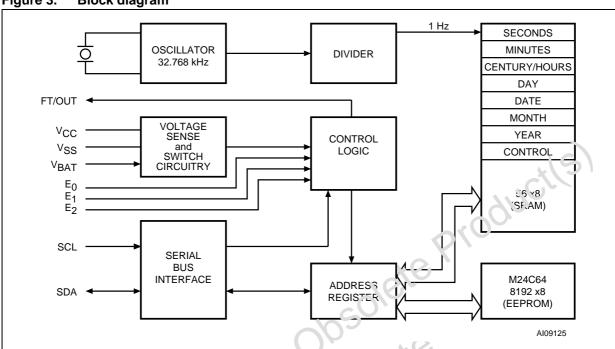
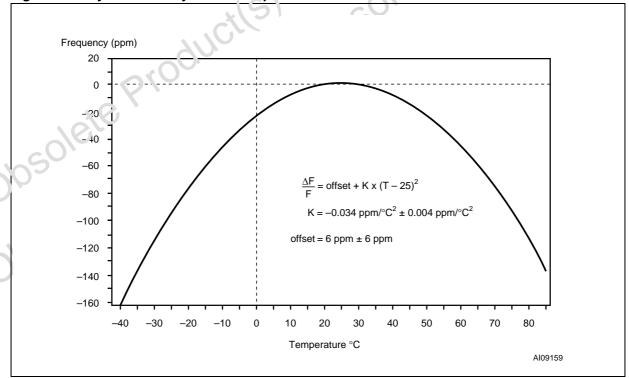


Figure 4. Crystal accuracy across temperature



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Application M41T56C64

Table 2. Device select code

	Device type identifier ⁽¹⁾				Chip enable address ⁽²⁾		R₩	
	b7	b6	b5	b4	b3	b2	b1	b0
M24C64	1	0	1	0	E2	E1	E0	R₩
M41T56	1	1	0	1	0	0	0	RW

^{1.} The most significant bit, b7, is sent first.

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Obsolete Producits) Obsolete Producits)

^{2.} E0, E1, and E2 are compared against the respective external pins on the memory device.

M41T56C64 Operation

Operation 4

4.1 Serial RTC device

The M41T56C64 contains one Serial RTC (M41T56). For detailed information on how to use the devices, see the M41T56 datasheet, which is available from your local STMicroelectronics distributor or from the STMicroelectronics website. http://www.st.com/rtc/.

4.2 **EEPROM** device

alled information in the control of The M41T56C64 contains a 64 Kbit Serial EEPROM (M24C64). For detailed information on



M41T56C64 Maximum rating

5 **Maximum rating**

Stressing the device above the rating listed in the "absolute maximum ratings" table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE program and other relevant quality documents.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
T_A	Ambient operating temperature	-40 to 85	C°C
T _{STG}	Storage temperature (V _{CC} off, oscillator off)	-55 to 125	°C
T _{SLD} ⁽¹⁾	Lead solder temperature for 10 seconds	2.0	°C
V _{IO}	Input or output voltages	-0.3 to 6.5	V
V _{CC}	Supply voltage	-0.3 to 6.5	V
I _O	Output current	20	mA
P _D	Power dissipation	0.25	W

For SOX18 package, Lead-free (Pb-free) Ir.ao "r.'sh. Reflow at peak temperature of 240°C (total thermal budget not to exceed 180°C for between \$0 to 150 seconds). No direct exposure to infrared (IR) reflow, or IR preheat allowed, to avoid damaging the e.m. Jedded 32KHz crystal. Joy -0.3V are no

Negative undershoots below -0.3V are not allowed on any pin while in the battery back-up

6 DC and AC parameters

This section summarizes the operating and measurement conditions, as well as the DC and AC characteristics of the device. The parameters in the following DC and AC characteristic tables are derived from tests performed under the measurement conditions listed in the relevant tables. Designers should check that the operating conditions in their projects match the measurement conditions when using the quoted parameters.

Table 4. Operating and AC measurement conditions⁽¹⁾

Parameter	Value	Unit
Supply voltage (V _{CC})	4.5 to 5.5	V
Ambient operating temperature (T _A)	-40 to 85	,(9)
Load capacitance (C _L)	100	pF
Input rise and fall times	50 (max)	ns
Input pulse voltages	0.2'v _{C3} 'o 0.8V _{CC}	V
Input and output timing ref. voltages	℃.3V _{CC} to 0.7V _{CC}	V

^{1.} Output Hi-Z is defined as the point where data is no longer driver.

Figure 5. AC measurement I/O waveform

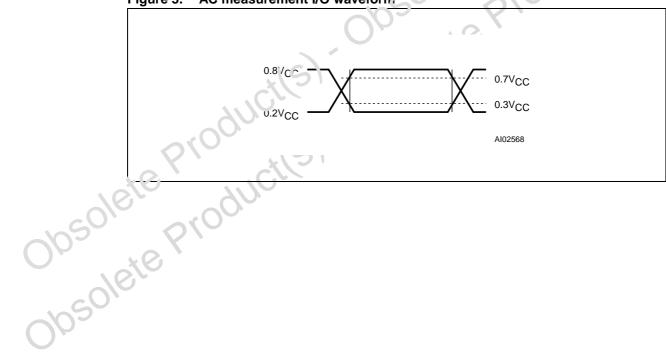


Table 5. Capacitance and input parameters

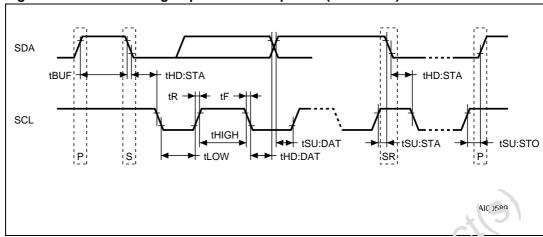
Symbol	Parameter ^{(1) (2)}	Test condition	Min	Max	Unit
C _{IN}	Input capacitance (SCL)			13	pF
	Input capacitance (SDA)			18	pF
	Input Capacitance (Other pins)			6	pF
Z _{WCL}	WC input impedance	V _{IN} < 0.5V	5	20	kΩ
Z _{WCH}	WC input impedance	$V_{IN} < 0.7V_{CC}$	500		kΩ
C _{OUT} ⁽³⁾	Output capacitance (SDA)			18	pF
	Output capacitance (FT/OUT)			10	ρF

- 1. Effective capacitance measured with power supply at 5V; sampled, not 100% tested.
- 2. At 25°C, f = 400kHz..
- 3. Outputs deselected.

Table 6. DC characteristics

Output capacitance (FT/Ol	JT)			10	PF
°C, f = 400kHz uts deselected.	er supply at 5V; sampled, no	ot 100% test	ed.	scile	
-	(1)		7	15	
Parameter		Wiin	тур	Max	Unit
Input leakage current	0V ≤V _{IN'} ≤V _{C'} C		Al	±3	μΑ
Output leakage current	0V ≤V _{(NUT} ≤V _{CC}	210	70	±3	μΑ
Supply current (Serial RTC active)	S vitch requency = 100kHz	K		310	μA
Supply current (Serial EEPROM active)	V_{CC} = 5V, f_c =400kHz (rise/fall time < 30ns)			2.2	mA
Supply current (รเลาเฮิษ)	SCL, SDA = $V_{CC} - 0.3$	/	100		μΑ
Input Icw voltage (SCL, SDA)	0,	-0.3		1.5	V
Ir ρ.τt low voltage (E2, E1, E0)		-0.45		0.3V _{CC}	V
Input low voltage (WC)		-0.45		0.5	V
Input high voltage (SCL, SDA)		3		V _{CC} + 0.8	V
Input high voltage (E2, E1, E1, WC)		0.7V _{CC}		V _{CC} + 1	V
Output low voltage	$I_{OL} = 3mA, V_{CC} = 5V$			0.4	V
Battery supply voltage		2.5	3	3.5	V
Battery supply current	$T_A = 25$ °C, $V_{CC} = 0V$, Oscillator ON, $V_{BAT} = 3$	v	450	550	nA
	tive capacitance measured with power C, f = 400kHz Lets deselected. DC characteristics I Parameter Input leakage current Output leakage current Supply current (Serial RTC active) Supply current (Serial EEPROM active) Supply current (Serial EEPROM active) Input Icw voltage (SCL, SDA) It put I bw voltage (E2, E1, E0) Input high voltage (SCL, SDA) Input high voltage (E2, E1, E1, WC) Output low voltage Battery supply voltage	tive capacitance measured with power supply at 5V; sampled, no °C, f = 400kHz Lets deselected. DC characteristics I Parameter Test Condition(1) Input leakage current	tive capacitance measured with power supply at 5V; sampled, not 100% test °C, f = 400kHz Its deselected. I Parameter Test Condition(1) Min Input leakage current 0V ≤V _{IN} ≤V _{CC} Output leakage current 0V ≤V _{OUT} ≤V _{CC} Supply current (Serial RTC active) Svitch requency = 100kHz Supply current (Serial EEPROM active) V _{CC} = 5V, f _c =400kHz (rise/fall time < 30ns) Supply current (scandby) SCL, SDA = V _{CC} − 0.3V Input Icw. Voltage (SCL, SDA) −0.3 It put Icw voltage (E2, E1, E0) −0.45 Input high voltage (SCL, SDA) 3 Input high voltage (SCL, SDA) 3 Input high voltage (SCL, SDA) 3 Input high voltage (SCL, SDA) 10, E3 mA, V _{CC} = 5V Battery supply voltage 2.5	tive capacitance measured with power supply at 5V; sampled, not 100% tested. C, f = 400kHz Its deselected. DC characteristics I Parameter Test Condition ⁽¹⁾ Min Typ Input leakage current $0V \leq V_{ D } \leq V_{ C }$ Output leakage current $0V \leq V_{ D } \leq V_{ C }$ Supply current (Serial RTC active) $V_{ C } = 5V$, $f_c = 400kHz$ (rise/fall time < 30ns) Supply current (Serial EEPROM active) $V_{ C } = 5V$, $V_{ C } = 5V$	tive capacitance measured with power supply at 5V; sampled, not 100% tested. **C, f = 400kHz **Its deselected.** **DC characteristics* I

- 1. Valid for ambient operating temperature: $T_A = -40$ to 85° C; $V_{CC} = 4.5$ to 5.5V (except where noted).
- 2. STMicroelectronics recommends the RAYOVAC BR1225 or BR1632 (or equivalent) as the battery supply.



AC Bus timing requirements sequence (serial RTC) Figure 6.

Table 7. AC characteristics, (serial RTC, M41T56)

Symbol	Parameter ⁽¹⁾	.Win	Max	Unit
f _{SCL}	SCL clock frequency	0	100	kHz
t _{LOW}	Clock low period	4.7	700	μs
t _{HIGH}	Clock high period	4 0		μs
t _R	SDA and SCL rise time		1	μs
t _F	SDA and SCL fall time		300	ns
t _{HD:STA}	START condition haid time (after this period the first clock pulse is generated)	4		μs
t _{SU:STA}	START condition setup time (only enacht for a repeated start condition)	4.7		μs
t _{SU:D} /;	ງ _ຣ ¹ 2 setup time	250		ns
t _{HD:DAT} (.)	Data hold time	0		μs
l 'SU:STO	STOP condition setup time	4.7		μs
t _{BUF}	Time the bus must be free before a new transmission can start	4.7		μs
(t _{LP}	Low-pass filter input time constant (SDA and SCL) for Serial RTC	0.25	1	μs
1. Valid fo	or ambient operating temperature: T _A = -40 to 85°C; VCC = 4.5	to 5.5V (exce	pt where note	ed).
2. Transn edge o	nitter must internally provide a hold time to bridge the undefined f SCL.	region (300n	s max.) of the	falling

Valid for ambient operating temperature: $T_A = -40$ to $85^{\circ}C$; VCC = 4.5 to 5.5V (except where noted).

Transmitter must internally provide a hold time to bridge the undefined region (300ns max.) of the falling edge of SCL.

Table 8. AC characteristics (Serial EEPROM, M24C64)

Symbol	Alt.	Parameter	Test condition	Min.	Max.	Unit
f _C	f_{SCL}	Clock frequency			400	kHz
t _{CHCL}	t _{HIGH}	Clock pulse width high		600		ns
t _{CLCH}	t_{LOW}	Clock pulse width low		1300		ns
t _{DL1DL2} ⁽¹⁾	t _F	SDA fall time		20	300	ns
t _{DXCX}	t _{SU:DAT}	Data in set up time		100		ns
t _{CLDX}	t _{HD:DAT}	Data in hold time		0		ns
t _{CLQX}	t _{DH}	Data out hold time		200	16	าร
t _{CLQV} (2)	t _{AA}	Clock low to next data valid (access time)		200	900	ns
t _{CHDX} (3)	t _{SU:STA}	Start condition set up time	ArC	000) ,	ns
t _{DLCL}	t _{HD:STA}	Start condition hold time		600		ns
t _{CHDH}	t _{SU:STO}	Stop condition set up time		600	9	ns
t _{DHDL}	t _{BUF}	Time between stop condition and next start condition	OYC	1300		ns
t _W	t _{WR}	Write time			5	ms
t _{NS}		Pulse width ignored (input filter on SCL and SDA for cerial EEPROM)	Single glitch		100	ns

^{1.} Sampled only, not 100% tested.

SILAPT and great of SDA.

PETAL OF SDA.

PETAL CONDITION OF FOLK

PETAL OF STAR (CONDITION OF FOLK

PETAL OF To avoid spurious ST.\h'T and STOP conditions, a minimum delay is placed between SCL=1 and the falling or rising ec ne of SDA.

^{3.} For a reST/R i condition, or following a Write cycle.

7 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

Obsolete Product(s) Obsolete Product(s)
Obsolete Product(s) Obsolete Product(s)

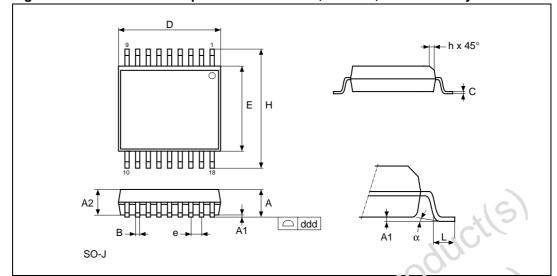


Figure 7. SOX18 – 18-lead plastic small outline, 300mils, embedded crystal

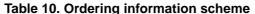
1. Drawing is not to scale.

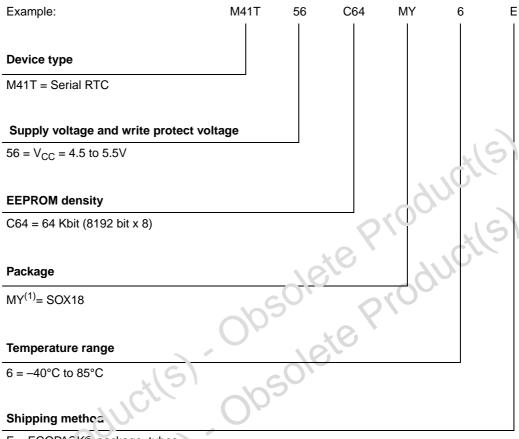
Table 9. SOX18 – 18-lead plastic small outline, 300nils, embedded crystal, package mech.

Comple at		millimetres	c0		inches	
Symbol	Тур	Min	XEM	Тур	Min	Max
А		2.44	2.69	0,10	0.096	0.106
A1		0.15	0.31		0.096	0.012
A2		2.29	2.39		0.090	0.094
В	AU	0.41	0.51		0.016	0.020
С	100	0.20	0.31		0.008	0.012
D	11.61	11.56	11.66	0.457	0.455	0.459
bkb	1,10		0.10			0.004
E	000	7.57	7.67		0.298	0.302
е	1.27	-	_	0.050	_	_
ОН		10.16	10.52		0.400	0.414
10 L		0.51	0.81		0.020	0.032
а		0°	8°		0°	8°
N		18		•	18	

M41T56C64 **Order codes**

Order codes 8





E = ECOPACK® package, tubes

F = EC PACK® package, tape & reel

rhe SOX18 package includes an embedded 32,768Hz crystal.

ge, tult
Jn® package, tap
The SOX18 package includes a
For other options, or for more
ST Sales Office nearest you. For other options, or for more information on any aspect of this device, please contact the

Revision history M41T56C64

9 Revision history

Table 11. Revision history

	Date	Version	Description
	14-Sep-2004	1	First Edition
	25-Mar-2005	2	Clarify pin connections, maximum rating
	4-Sep-2006	3	Datasheet status updated to full datasheet; changed title on page 1; small text changes to Section 1: Summary description; reformatted figure in the Feature summary, reformatted Figure 1, Figure 2, Table 2 and Table 9; ecopack compliant; updated disclaimer
	22-Sep-2006	4	Added information on EEPROM density <i>Table 10: Ordering information scheme</i>
Obsolete Product(s) Obsolete Product(s) Obsolete Product(s) Obsolete Product(s)			

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