

# MT29F256G08CKEDBJ5-12

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## Data Sheets (1)

### Data Sheet

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### Orderable Part Information

Status	Production	Alternative Part	N/A
FBGA Code	NW554	SPD Data	N/A
MBQual Data	N/A	Shipping Media	N/A
PLP	No	Start Date	N/A

### Specs

Density	256Gb	Status	Production
RoHS	Yes	Width	x8
Voltage	3.3V	Package	TBGA
Pin Count	132-ball	MT/s	166 MT/s
I/O	Common	Product Name	

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## Sim Models & Software

## FAQs

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Date	What was added
04/2014	64Gb 128Gb 256Gb 512Gb Async Sync NAND
01/2014	IBIS: 64Gb 128Gb 256Gb 512Gb Async Sync NAND

### FAQs

- » [Do you support small block devices?](#)
- » [How much ECC do I need to support your devices?](#)
- » [I am using the correct amount of error correction code \(ECC\) for the NAND device, but I'm still seeing bit/byte errors in data I read back from the NAND device.](#)
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### Sim Models & Software

Title & Description	Secure	ID	Updated
HSpipe: 64Gb 128Gb 256Gb 512Gb Async Sync NAND: Rev2.1		L84C	01/2014
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[+](#) [My design was based on a specification stating the JTAG was relative to VDD \(1.8V\), but now we've discovered that JTAG is actually relative to VDDQ \(1.5V\). It's a fairly significant board spin to change this; what do I risk by leaving the design as-is? I assume that the specification is still for VDDQ + 0.3V = 1.8V, but with CMOS parts there's no way I can guarantee that it won't swing past that on transitions.](#)
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