REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Correct case outline X as non-standard case outline. Change Radiation Hardness Assurance (RHA) level to R. Change V_{OLV}, t_{PHL1}, t_{PLH1}, t_{PLZ1}, t_{PHZ1}, t_{PLZ2}, and t_{PHZ2} maximum limits in table I to adapt the RHA level R. Make change to footnote 3/ in table I. Editorial changes throughout. - TVN	03-10-17	Thomas M. Hess
B	Add device type 02. Correct DC input voltage range (V_{IN}) and lead temperature in section 1.3. Correct input voltage range (V_{IN}) in note 5 of figure 6, switching waveforms and test circuit. Update the boilerplate to the requirements of MIL-PRF-38535. Editorial changes throughout. - TVN	06-06-01	Thomas M. Hess
C	Change Radiation Hardness Assurance (RHA) level to F. - TVN	07-02-09	Thomas M. Hess
D	Update radiation features in section 1.5 and add SEP test table IB. Update the boilerplate paragraphs to the current requirements of MIL-PRF-38535. - MAA	12-02-16	Thomas M. Hess
E	Add die for device type 02 and die appendix A. Update vendor information. Delete class M requirements throughout. Update boilerplate paragraphs to the current requirements of MIL-PRF-38535. - MAA	14-05-28	Thomas M. Hess
F	To correct absolute maximum rating DC input/output clamp current (I_{IK},I_{OK}) in section 1.3. – MAA	16-08-10	Thomas M. Hess
G	To correct vendor pin number for supplying die of device type 02. – MAA	16-11-23	Muhammad Akbar
H	Add case outline Y to section 1.2.4 for device type 02. Update boilerplate paragraphs to the current requirements of MIL-PRF-38535. - MAA	18-03-22	Thomas M. Hess

REV																				
SHEET																				
REV	H	H	H	H	H	H	H	H	H	H	H	H	H							
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27							

REV STATUS OF SHEETS																
REV	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14		

PMIC N/A

PREPARED BY
Thanh V. Nguyen

CHECKED BY
Thanh V. Nguyen

APPROVED BY
Thomas M. Hess

DRAWING APPROVAL DATE
03-06-05

REVISION LEVEL
H

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
http://www.dla.mil/landandmaritime

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

MICROCIRCUIT, DIGITAL, RADIATION HARDENED, LOW VOLTAGE CMOS, 16-BIT BUS TRANSCEIVER WITH BUS HOLD AND THREE-STATE OUTPUTS, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	5962-02508

SHEET 1 OF 27

DSCC FORM 2233
APR 97

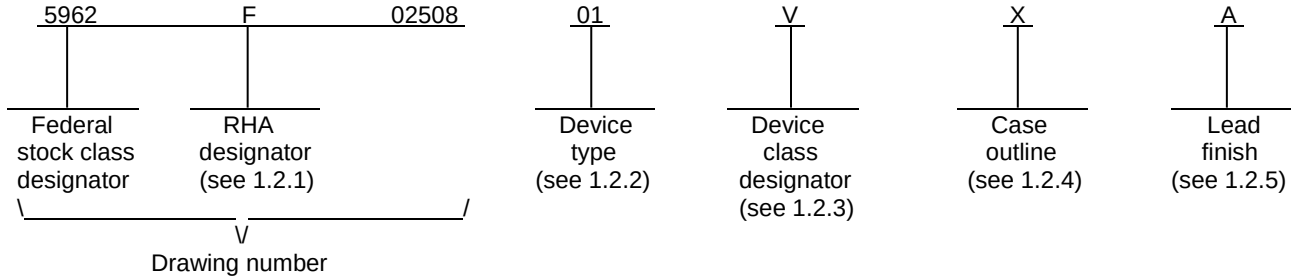
5962-E271-18

DISTRIBUTION STATEMENT A. Approved for public release. Distribution is unlimited

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability device class Q and space application device class V. A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54VCXH162245	16-bit bus transceiver with bus hold, series output resistors on A side, and three-state outputs
02	54VCXH162245	16-bit bus transceiver with bus hold, series output resistors on A side, and three-state outputs

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	48	Flat pack 1/
Y	See figure 1	48	Flat pack 2/

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

1/ Package case outline X flat pack with isolated lid.
2/ Package case outline Y flat pack with grounded lid.

1.3 Absolute maximum ratings. 1/ 2/ 3/

Supply voltage range (V_{CC}) ..... -0.5 V dc to +4.6 V dc
DC input voltage range (V_{IN}) ..... -0.5 V dc to +4.6 V dc
DC output voltage range (V_{OUT}) ..... -0.5 V dc to V_{CC} + 0.5 V dc
DC input/output clamp current (I_{IK}, I_{OK}) ..... - 50 mA
DC output current (per pin) (I_{OUT}) ..... ±50 mA
DC V_{CC} or GND current (per output pin) (I_{CC}, I_{GND}) ..... ±100 mA
Maximum power dissipation (P_D) ..... 400 mW
Storage temperature range (T_{STG}) ..... -65°C to +150°C
Lead temperature (soldering, 10 seconds) ..... +260°C
Thermal resistance, junction-to-case (θ_{JC}) ..... 22°C/W
Junction temperature (T_J) ..... +150°C 4/

1.4 Recommended operating conditions. 2/ 3/

Supply voltage range (V_{CC}):

Device type 01 ..... +2.3 V dc to +3.6 V dc
Device type 02 ..... +1.8 V dc to +3.6 V dc
Input voltage range (V_{IN}) ..... -0.3 V dc to +3.6 V dc
Output voltage range (V_{OUT}) ..... +0.0 V dc to V_{CC}
Maximum high level output current (I_{OH}):
A side:
V_{CC} = 1.8 V (device type 02) ..... -4 mA
V_{CC} = 2.3 V to 2.7 V ..... -8 mA
V_{CC} = 3.0 V to 3.6 V ..... -12 mA
B side:
V_{CC} = 1.8 V (device type 02) ..... -6 mA
V_{CC} = 2.3 V to 2.7 V ..... -18 mA
V_{CC} = 3.0 V to 3.6 V ..... -24 mA
Maximum low level output current (I_{OL}):
A side:
V_{CC} = 1.8 V (device type 02) ..... +4 mA
V_{CC} = 2.3 V to 2.7 V ..... +8 mA
V_{CC} = 3.0 V to 3.6 V ..... +12 mA
B side:
V_{CC} = 1.8 V (device type 02) ..... +6 mA
V_{CC} = 2.3 V to 2.7 V ..... +18 mA
V_{CC} = 3.0 V to 3.6 V ..... +24 mA
Input rise or fall time rate ($\Delta t/\Delta V$):
V_{CC} = 3.0 V ..... 0 to 10 ns/V
Case operating temperature range (T_C) ..... -55°C to +125°C

1.5 Radiation features.

Maximum total dose available (dose rate = 50 – 300 Rad(Si)/s):
For device types 01 and 02 ..... 300K Rad(Si)
Single event effects (SEE) for device types 01 and 02:
No Single Event Latch-up (SEL) occurs at effective LET (see 4.4.4.2) ..... ≤ 72 MeV-cm^2/mg 5/
No Single Event Upset (SEU) occurs at effective LET (see 4.4.4.2) ..... ≤ 72 MeV-cm^2/mg 5/

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Unless otherwise noted, all voltages are referenced to GND.
3/ The limits for the parameters specified herein shall apply over the full specified V_{CC} range and case temperature range of -55°C to +125°C.
4/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.
5/ Limits are guaranteed by design or process, but not production tested unless specified by the customer through the purchase order or contract.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://quicksearch.dla.mil/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

ASTM INTERNATIONAL (ASTM)

ASTM F1192 - Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of semiconductor Devices.

(Copies of these documents are available online at https://www.astm.org or from ASTM International, 100 Barr Harbor Drive, P.O. Box C700, West Conshohocken, PA, 19428-2959).

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.1.1 Microcircuit die. For the requirements for microcircuit die, see appendix A to this document.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 and figure 1 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table. The truth table shall be as specified on figure 3.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 4.

3.2.5 Ground bounce waveforms and test circuit. The ground bounce waveforms and test circuit shall be as specified on figure 5.

3.2.6 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 6.

3.2.7 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post irradiation parameter limits are as specified in table IA and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

TABLE IA. Electrical performance characteristics.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ 3/ $-55°C \le T_C \le +125°C$ $+1.8\ V \le V_{CC} \le +3.6\ V$ unless otherwise specified		Device type and device class	V_{CC}	Group A subgroups	Limits 4/		Unit
							Min	Max	
Negative input clamp voltage 3022	V_{IC-}	For input under test, $I_{IN} = -1.0$ mA		All Q, V	Open	1	-0.4	-1.5	V
High level output voltage 3006	V_{OH}	$V_{IN} = V_{IH}$ minimum or V_{IL} maximum $I_{OH} = -100\ \mu A$		All All	2.7 V	1, 2, 3	2.5		V
					3.6 V	1, 2, 3	3.4		
		A side $V_{IN} = V_{IH}$ minimum or V_{IL} maximum	$I_{OH} = -6$ mA	All All	2.3 V	1	1.8		
					2.7 V	1	2.2		
			$I_{OH} = -8$ mA		2.3 V	1, 2, 3	1.7		
					3.0 V	1	2.4		
			$I_{OH} = -12$ mA		3.0 V	1, 2, 3	2.2		
			$I_{OH} = -4$ mA	02 All	1.8 V	1	1.4		
		B side $V_{IN} = V_{IH}$ minimum or V_{IL} maximum	$I_{OH} = -12$ mA	All All	2.3 V	1	1.8		
					2.7 V	1	2.2		
			$I_{OH} = -18$ mA		2.3 V	1, 2, 3	1.7		
					3.0 V	1	2.4		
			$I_{OH} = -24$ mA		3.0 V	1, 2, 3	2.2		
			$I_{OH} = -6$ mA	02 All	1.8 V	1	1.4		
Low level output voltage 3007	V_{OL}	$V_{IN} = V_{IH}$ minimum or V_{IL} maximum $I_{OL} = 100\ \mu A$		All All	2.7 V	1, 2, 3		0.20	V
					3.6 V	1, 2, 3		0.20	
		A side $V_{IN} = V_{IH}$ minimum or V_{IL} maximum	$I_{OL} = 6$ mA	All All	2.3 V	1		0.40	
					2.7 V	1		0.40	
			$I_{OL} = 8$ mA		2.3 V	1, 2, 3		0.60	
					3.0 V	1		0.55	
			$I_{OL} = 12$ mA		3.0 V	1, 2, 3		0.80	
			$I_{OL} = 4$ mA	02 All	1.8 V	1		0.3	
		B side $V_{IN} = V_{IH}$ minimum or V_{IL} maximum	$I_{OL} = 12$ mA	All All	2.3 V	1		0.40	
					2.7 V	1		0.40	
			$I_{OL} = 18$ mA		2.3 V	1, 2, 3		0.60	
					3.0 V	1		0.40	
			$I_{OL} = 24$ mA		3.0 V	1, 2, 3		0.55	
			$I_{OL} = 6$ mA	02 All	1.8 V	1		0.3	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ 3/ $-55°C \le T_C \le +125°C$ $+1.8\ V \le V_{CC} \le +3.6\ V$ unless otherwise specified	Device type and device class	V_{CC}	Group A subgroups	Limits 4/		Unit
						Min	Max	
High level input voltage	V_{IH} 5/		All	2.3 V	1, 2, 3	1.6		V
			All	2.7 V	1, 2, 3	2.0		
				3.0 V	1, 2, 3	2.0		
				3.6 V	1, 2, 3	2.0		
			02	1.8 V	1, 2, 3	1.2		
			All					
Low level input voltage	V_{IL} 5/		All	2.3 V	1, 2, 3		0.7	V
			All	2.7 V	1, 2, 3		0.8	
				3.0 V	1, 2, 3		0.8	
				3.6 V	1, 2, 3		0.8	
			02	1.8 V	1, 2, 3		0.4	
			All					
Input leakage current high 3010	I_{IH}	For input under test, $V_{IN} = 3.6\ V$ For all other inputs, $V_{IN} = V_{CC}$ or GND	All All	3.6 V	1, 2, 3		5	µA
Input leakage current low 3009	I_{IL}	For input under test, $V_{IN} = 0.0\ V$ For all other inputs, $V_{IN} = V_{CC}$ or GND	All All	3.6 V	1, 2, 3		-5	µA
Quiescent supply current, output high 3005	I_{CCH}	$V_{IN} = V_{CC}$ or GND	All All	3.6 V	1		20	µA
					2, 3		100	
Quiescent supply current, output low 3005	I_{CCL}	$V_{IN} = V_{CC}$ or GND	All All	3.6 V	1		20	µA
					2, 3		100	
Quiescent supply current, output three-state 3005	I_{CCZ}	$V_{IN} = V_{CC}$ or GND	All All	3.6 V	1		20	µA
					2, 3		100	
Quiescent supply current delta, TTL input levels 3005	ΔI_{CC} 6/	For input under test, $V_{IH} = V_{CC} - 0.6\ V$ For all other inputs, $V_{IN} = V_{CC}$ or GND	All All	3.6 V	1, 2, 3		750	µA
Input hold current	$I_{I(HOLD)}$	$V_{IN} = 0.8\ V$	All All	3.0 V	1, 2, 3	75		µA
		$V_{IN} = 2.0\ V$		3.0 V	1, 2, 3	-75		
Power off leakage current	I_{OFF}	V_{IN} or $V_{OUT} = 0.0\ V$ to $3.6\ V$	All All	0.0 V	1, 2, 3		10	µA

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ 3/ $-55°C \le T_C \le +125°C$ $+1.8\ V \le V_{CC} \le +3.6\ V$ unless otherwise specified	Device type and device class	V_{CC}	Group A subgroups	Limits 4/		Unit
						Min	Max	
Three-state output leakage current high 3021	I_{OZH}	$V_{IN} = V_{IH}$ minimum or V_{IL} maximum $V_{OUT} = 3.6\ V$	All All	3.6 V	1, 2, 3		+10	µA
Three-state output leakage current low 3020	I_{OZL}	$V_{IN} = V_{IH}$ minimum or V_{IL} maximum $V_{OUT} = 0.0\ V$	All All	3.6 V	1, 2, 3		-10	µA
Input capacitance 3012	C_{IN}	See 4.4.1c $T_C = +25°C$	All All	GND	4		10	pF
Output capacitance 3012	C_{OUT}	See 4.4.1c $T_C = +25°C$	All All	3.3 V	4		12	pF
Power dissipation capacitance	C_{PD} 7/	See 4.4.1c $T_C = +25°C$, f = 1 MHz	All All	3.3 V	4		80	pF
Low level ground bounce noise	V_{OLP} 8/	$V_{IH} = 3.3\ V$, $V_{IL} = 0.0\ V$ $T_A = +25°C$ See figure 5 See 4.4.1d	All All	3.3 V	4		1250	mV
	V_{OLV} 8/				4		-600	
High level V_{CC} bounce noise	V_{OHP} 8/		All All	3.3 V	4		1350	mV
	V_{OHV} 8/				4		-1250	
Functional tests 3014	9/	$V_{IN} = V_{IH}$ minimum or V_{IL} maximum Verify output V_{OUT} See 4.4.1b	All All	2.3 V	7, 8	L	H	
				2.7 V	7, 8	L	H	
				3.6 V	7, 8	L	H	
			02 All	1.8 V	7, 8	L	H	
Propagation delay time, mAn to mBn 3003	t_{PHL1}, t_{PLH1} 10/	$C_L = 30\ pF$ minimum $R_L = 500\Omega$ See figure 6	All All	2.3 V	9, 10, 11	1.0	4.0	ns
				3.6 V	9, 10, 11	0.8	3.6	
			02 All	1.8 V	9, 10, 11	1.0	7.0	
Propagation delay time, mBn to mAn 3003	t_{PHL2}, t_{PLH2} 10/		All All	2.3 V	9, 10, 11	1.0	4.9	ns
				3.6 V	9, 10, 11	0.8	4.0	
			02 All	1.8 V	9, 10, 11	1.0	8.7	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ 3/ $-55°C \le T_C \le +125°C$ $+1.8\ V \le V_{CC} \le +3.6\ V$ unless otherwise specified	Device type and device class	V_{CC}	Group A subgroups	Limits 4/		Unit
						Min	Max	
Propagation delay time, output enable, $m\overline{G}$ to mBn 3003	t_{PZL1}, t_{PZH1} 10/	C_L = 30 pF minimum R_L = 500Ω See figure 6	All All	2.3 V	9, 10, 11	1.0	5.8	ns
				3.6 V	9, 10, 11	0.8	4.3	
			02 All	1.8 V	9, 10, 11	1.0	9.0	
Propagation delay time, output enable, $m\overline{G}$ to mAn 3003	t_{PZL2}, t_{PZH2} 10/		All All	2.3 V	9, 10, 11	1.0	6.8	ns
				3.6 V	9, 10, 11	0.8	4.8	
			02 All	1.8 V	9, 10, 11	1.0	10.5	
Propagation delay time, output disable, $m\overline{G}$ to mBn 3003	t_{PLZ1}, t_{PHZ1} 10/		All All	2.3 V	9, 10, 11	1.0	4.8	ns
				3.6 V	9, 10, 11	0.8	5.6	
			02 All	1.8 V	9, 10, 11	1.0	6.8	
Propagation delay time, output disable, $m\overline{G}$ to mAn 3003	t_{PLZ2}, t_{PHZ2} 10/		All All	2.3 V	9, 10, 11	1.0	5.7	ns
				3.6 V	9, 10, 11	0.8	7.0	
			02 All	1.8 V	9, 10, 11	1.0	8.0	

1/ For tests not listed in the referenced MIL-STD-883, [e.g. V_{IH}, V_{IL}], utilize the general test procedure under the conditions listed herein.

2/ Each input/output, as applicable, shall be tested at the specified temperature, for the specified limits, to the tests in table IA herein. Output terminals not designated shall be high level logic, low level logic, or open, except as follows:
   a. For V_{IC-} test, the V_{CC} terminal shall be open. T_C = +25°C.
   b. For all I_{CC} and ΔI_{CC} tests, the output terminal shall be open. When performing these tests, the current meter shall be placed in the circuit such that all current flows through the meter.

3/ RHA parts for device types 01 and 02 meet all levels M, D, P, L, R, and F of irradiation. However, these parts are only tested at the "F" level. Pre and post irradiation values are identical unless otherwise specified in table IA. When performing post irradiation electrical measurements for any RHA level, T_A = 25°C.

4/ For negative and positive voltage and current values, the sign designates the potential difference in reference to GND and the direction of current flow, respectively; and the absolute value of the magnitude, not the sign, is relative to the minimum and maximum limits, as applicable, listed herein. All devices shall meet or exceed the limits specified in table IA, as applicable, at $1.8\ V \le V_{CC} \le 3.6\ V$.

5/ The V_{IH} and V_{IL} tests are not required if applied as forcing functions for V_{OH} and V_{OL} tests.

6/ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than at 0.0 V or V_{CC}. This test may be performed either one input at a time (preferred method) or with all input pins simultaneously at $V_{IN} = V_{CC} - 0.6\ V$ (alternate method). Classes Q and V shall use the preferred method. When the test is performed using the alternate test method, the maximum limit is equal to the number of inputs at a high TTL input level times ΔI_{CC} maximum limit, and the preferred method and limits are guaranteed.

7/ Power dissipation capacitance (C_{PD}) determines both the power consumption (P_D) and dynamic current consumption (I_S). Where:

$$P_D = (C_{PD} + C_L)(V_{CC} \times V_{CC})f + (I_{CC} \times V_{CC}) + (n \times d \times \Delta I_{CC} \times V_{CC})$$

$$I_S = (C_{PD} + C_L)\, V_{CC} f + I_{CC} + n \times d \times \Delta I_{CC}$$

For both P_D and I_S, n is number of device inputs at TTL levels; d is duty cycle of the input signal; f is the frequency of the input signal; and C_L is the external output load capacitance.

TABLE IA. Electrical performance characteristics - Continued.

8/ This test is for qualification only. Ground and V_{CC} bounce tests are performed on a non-switching (quiescent) output and are used to measure the magnitude of induced noise caused by other simultaneously switching outputs. The test is performed on a low noise bench test fixture. For the device under test, all outputs shall be loaded with 500Ω load resistance and a minimum of 50 pF of load capacitance (see figure 5). Only chip capacitors and resistors shall be used. The output load components shall be located as close as possible to the device outputs. It is suggested, that whenever possible, this distance be kept to less than 0.25 inches. Decoupling capacitors shall be placed in parallel from V_{CC} to ground. The values of these decoupling capacitors shall be determined by the device manufacturer. The low and high level ground and V_{CC} bounce noise is measured at the quiet output using a 1 GHz minimum bandwidth oscilloscope with a 50Ω impedance.

The device inputs shall be conditioned such that all outputs are at a low nominal V_{OH} level. The device inputs shall then be conditioned such that they switch simultaneously and the output under test remains at V_{OH} as all other outputs possible are switched from V_{OH} to V_{OL}. V_{OHV} and V_{OHP} are then measured from the nominal V_{OH} level to the largest negative and positive peaks, respectively (see figure 5). This is then repeated with the same outputs not under test switching from V_{OL} to V_{OH}.

The device inputs shall be conditioned such that all outputs are at a low nominal V_{OL} level. The device inputs shall then be conditioned such that they switch simultaneously and the output under test remains at V_{OL} as all other outputs possible are switched from V_{OL} to V_{OH}. V_{OLP} and V_{OLV} are then measured from the nominal V_{OL} level to the largest positive and negative peaks, respectively (see figure 5). This is then repeated with the same outputs not under test switching from V_{OH} to V_{OL}.

9/ Tests shall be performed in sequence, attributes data only. Functional tests shall include the truth table and other logic patterns used for fault detection. The test vectors used to verify the truth table shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth table in figure 3 herein. Functional tests shall be performed in sequence as approved by the qualifying activity on qualified devices. Allowable tolerances in accordance with MIL-STD-883 for the input voltage levels may be incorporated. For outputs, L ≤ V_{IL} maximum, H ≥ V_{IH} minimum.

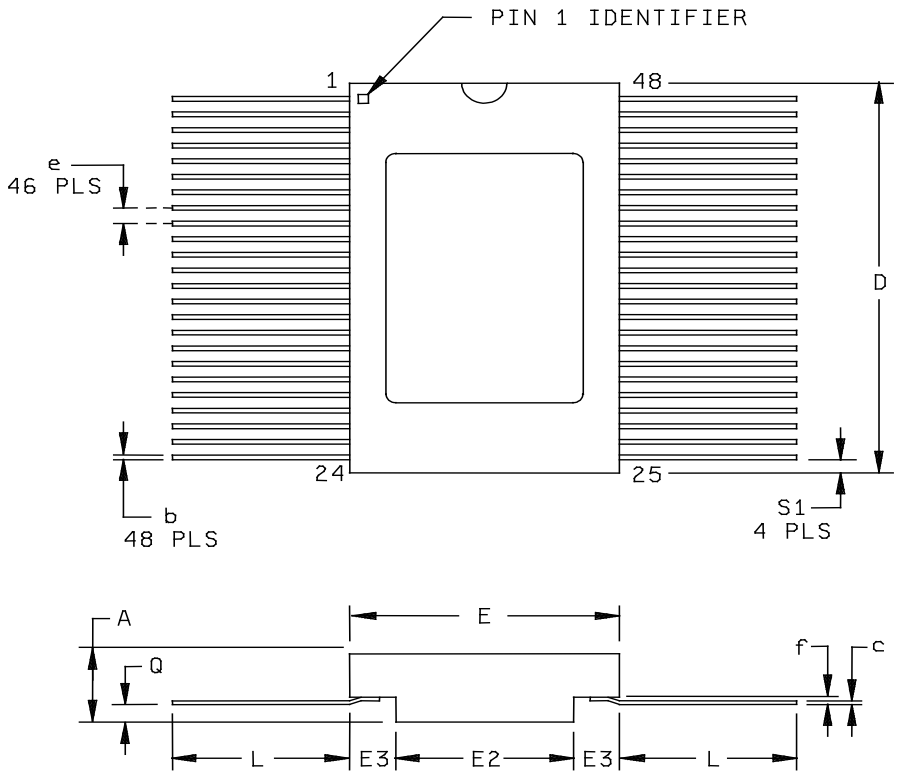
10/ AC limits at V_{CC} = 2.7 V are equal to the limits at V_{CC} = 2.3 V and guaranteed by testing at V_{CC} = 2.3 V. AC limits at V_{CC}=3.0V are equal to the limits at V_{CC} = 3.6 V and guaranteed by testing at V_{CC} = 3.6 V. Minimum ac limits for V_{CC}=2.7V are 1.0 ns and guaranteed by guardbanding the V_{CC} = 2.3 V minimum limits to 1.0 ns. Minimum ac limits for V_{CC} = 3.0 V are 0.8 ns and guaranteed by guardbanding the V_{CC} = 3.6 V minimum limits to 0.8 ns. For propagation delay tests, all paths must be tested.

TABLE IB. SEP test limits. 1/ 2/

Device types	V_{CC} = 1.8 V 3/		Bias V_{CC} = 3.6 V For Latch-up test no latch-up(SEL) at effective LET 3/ 4/
	Effective LET no upsets(SEU)	Maximum device cross section (μm^2)	
01, 02	LET ≤ 72 MeV/(mg/cm^2)	5/	L:ET ≤ 72 MeV/(mg/cm^2)

1/ For SEP test conditions, see 4.4.4.2 herein.
2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end-of-line testing. Test plan must be approved by TRB and qualifying activity.
3/ Worst case temperature is T_A = +125°C ± 10°C for SEL and T_A = +25°C ± 10°C for SEU
4/ Tested to LET ≥ 72 MeV/(mg/cm^2), and no latch-up (SEL) at effective LET ≤ 72 MeV/(mg/cm^2).
5/ Tested to LET ≥ 72 MeV/(mg/cm^2), and no single event upsets (SEU) at effective LET ≤ 72 MeV/(mg/cm^2).

Case outline X and Y



Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	.086	.107	2.18	2.72
b	.008	.012	0.20	0.30
c	.005	.007	0.12	0.18
D	.613	.627	15.57	15.92
E	.375	.385	9.52	9.78
E2	.245	.255	6.22	6.48
E3	.060	.070	1.52	1.78
e	.025 BSC		0.635 BSC	
f	.008 BSC		0.20 BSC	
L	.270	.370	6.85	9.40
Q	.026	.036	0.66	0.92
S1	.010	.024	0.25	0.61
N	48		48	

Note: Package case outline X flat pack with isolated lid. Package case outline Y flat pack with grounded lid.

FIGURE 1. Case outline X and Y.

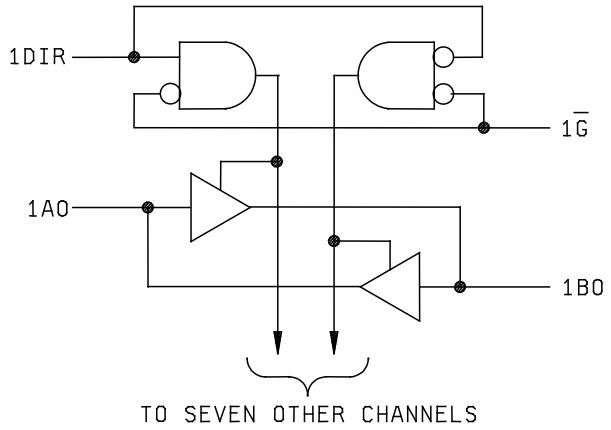
Device type	All		
Case outline	X and Y		
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	1DIR	25	$2\overline{G}$
2	1B0	26	2A7
3	1B1	27	2A6
4	GND	28	GND
5	1B2	29	2A5
6	1B3	30	2A4
7	V_{CC}	31	V_{CC}
8	1B4	32	2A3
9	1B5	33	2A2
10	GND	34	GND
11	1B6	35	2A1
12	1B7	36	2A0
13	2B0	37	1A7
14	2B1	38	1A6
15	GND	39	GND
16	2B2	40	1A5
17	2B3	41	1A4
18	V_{CC}	42	V_{CC}
19	2B4	43	1A3
20	2B5	44	1A2
21	GND	45	GND
22	2B6	46	1A1
23	2B7	47	1A0
24	2DIR	48	$1\overline{G}$

FIGURE 2. Terminal connections.

Inputs		Function		Output
$m\overline{G}$	mDIR	A bus	B bus	
L	L	Output	Input	A = B
L	H	Input	Output	B = A
H	X	Z	Z	Z

H = High voltage level
L = Low voltage level
X = Immaterial
Z = High impedance

FIGURE 3. Truth table.



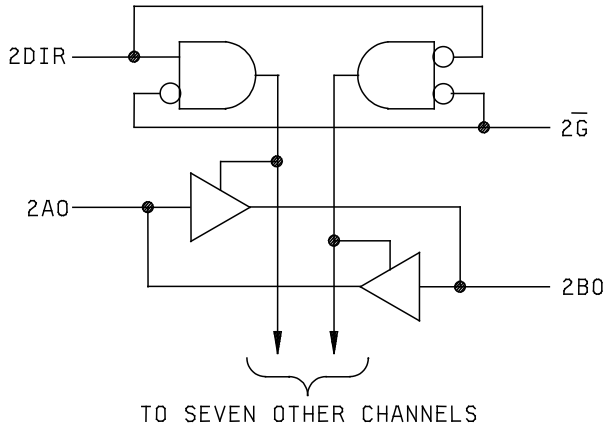
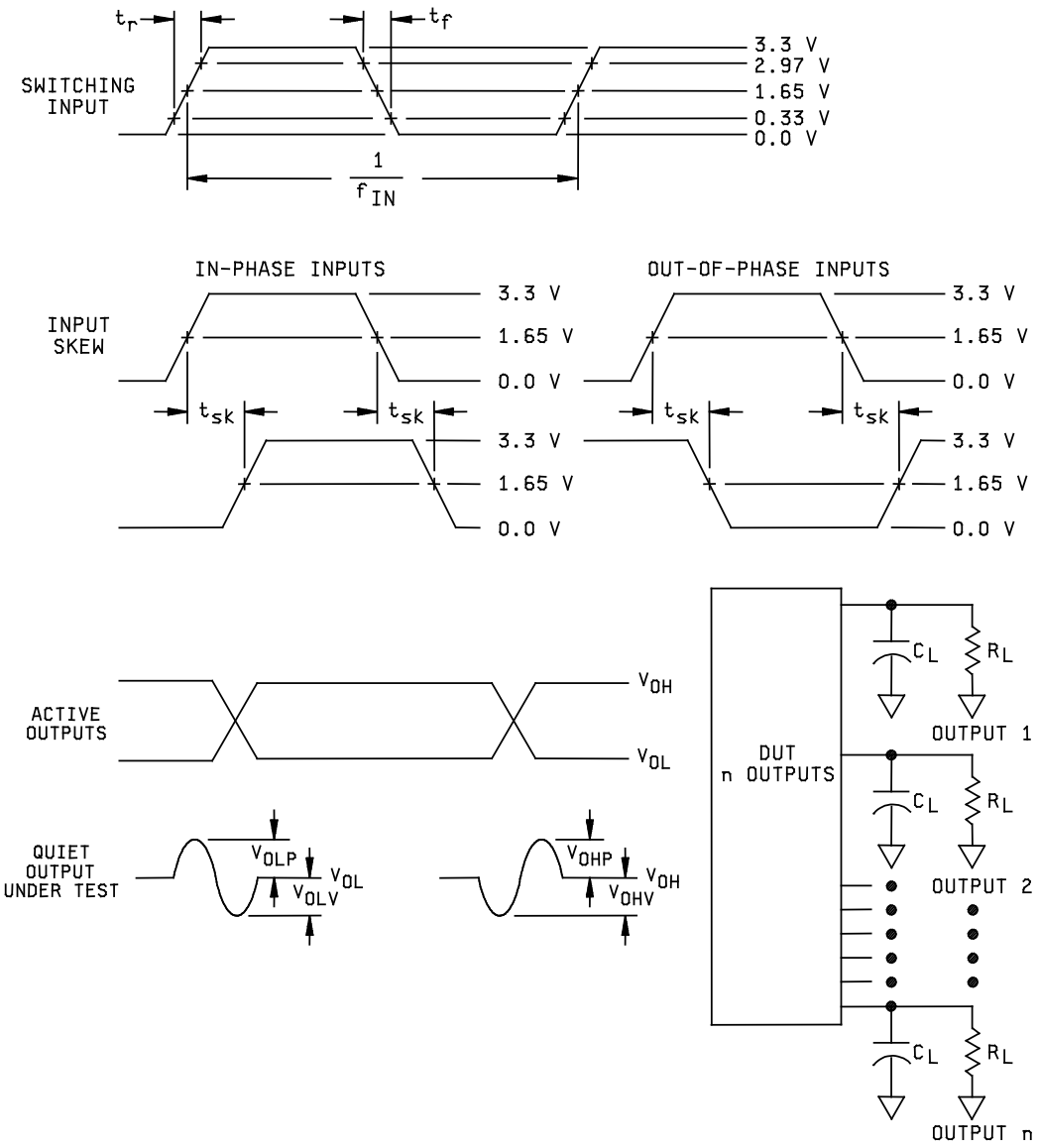


FIGURE 4. Logic diagram.



NOTES:

1. C_L includes a 47 pF chip capacitor (-0 percent, +20 percent) and at least 3 pF of equivalent capacitance from the test jig and probe.
2. R_L = 500Ω ±1 percent, chip resistor in series with a 50Ω termination. For monitored outputs, the 50Ω termination shall be the 50Ω characteristic impedance of the coaxial connector to the oscilloscope.
3. Input signal to the device under test:
   a. V_{IN} = 0.0 V to 3.3 V; duty cycle = 50 percent; $f_{IN} \geq 1$ MHz.
   b. t_r, t_f = 3.0 ns ±0.1 ns. For input signal generators incapable of maintaining these values of t_r and t_f, the 3.0 ns limit may be increased up to 10 ns, as needed, maintaining the ±1.0 ns tolerance and guaranteeing the results at 3.0 ns ±1.0 ns; skew between any two switching input signals (t_{sk}): ≤ 250 ps.

FIGURE 5. Ground bounce waveforms and test circuit.

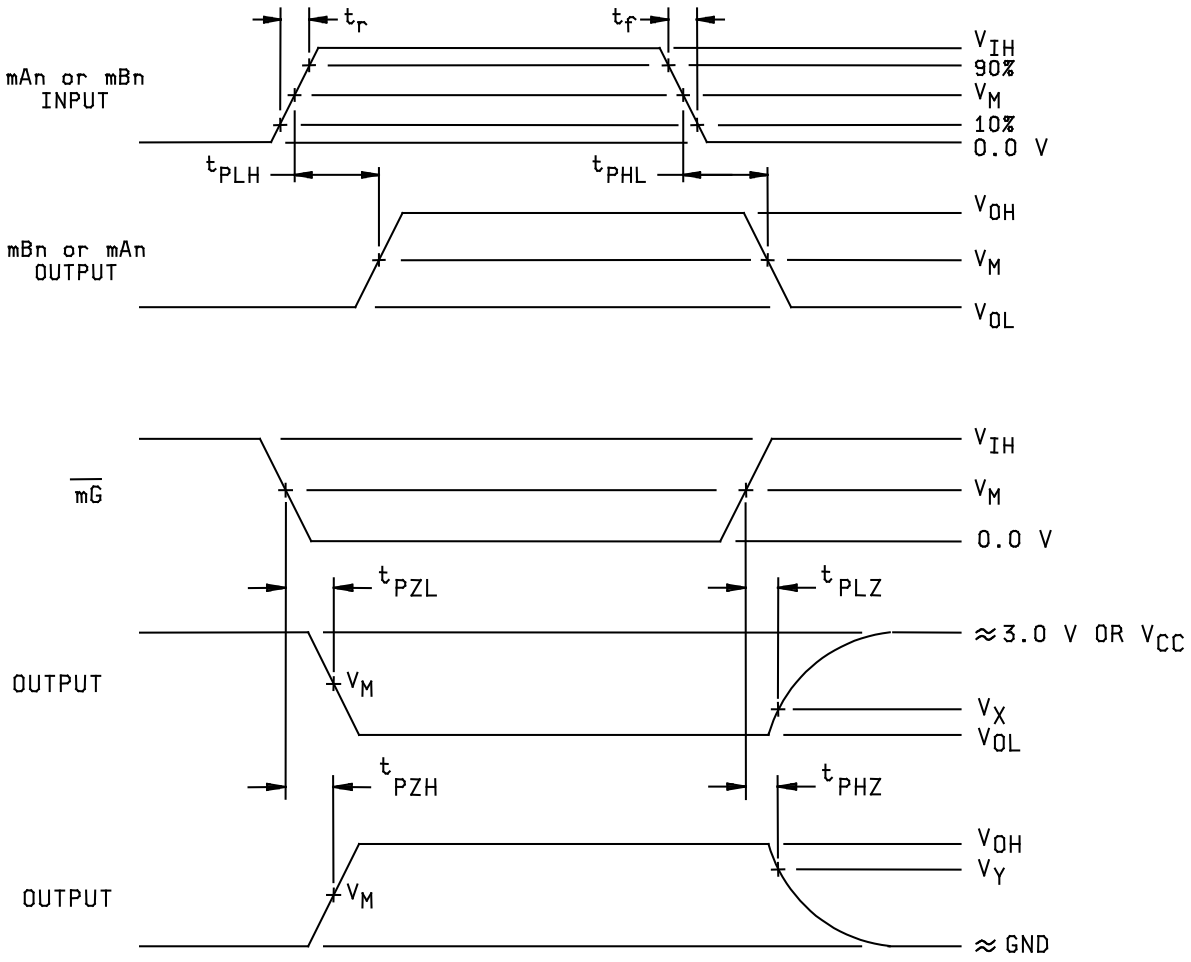
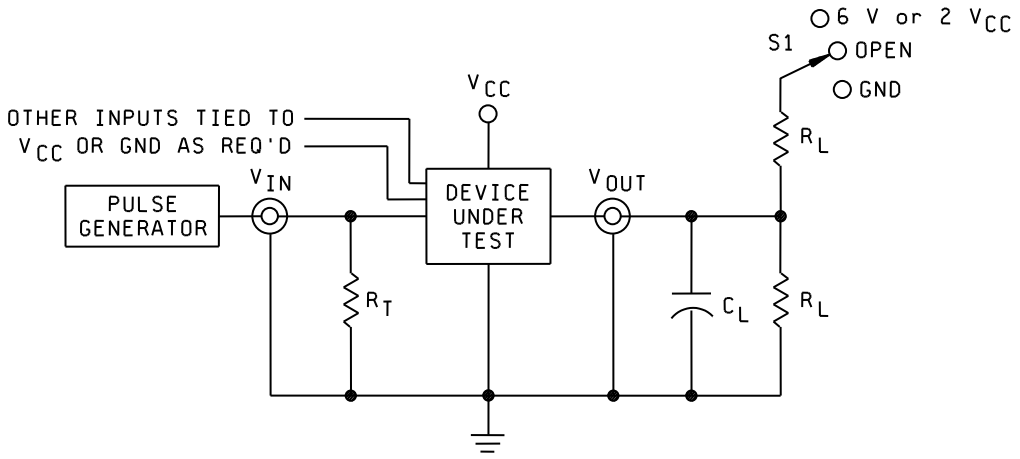


FIGURE 6. Switching waveforms and test circuit.



Symbol	V_{CC}	
	1.8 V and 2.3 V to 2.7 V	3.0 V to 3.6 V
V_{IH}	V_{CC}	2.7 V
V_M	$V_{CC}/2$	1.5 V
V_X	V_{OL} + 0.15 V	V_{OL} + 0.3 V
V_Y	V_{OH} - 0.15 V	V_{OH} - 0.3 V

NOTES:
1. When measuring t_{PLH} and t_{PHL}: S1 = open.
   When measuring t_{PLZ} and t_{PZL}: S1 = $2V_{CC}$ for V_{CC} = 1.8 V and V_{CC} = 2.3 V to 2.7 V; S1 = 6.0 V for V_{CC} = 3.0 V to 3.6 V.
   When measuring t_{PHZ} and t_{PZH}: S1 = GND.
2. The t_{PZL} and t_{PZH} reference waveform is for the output under test with internal conditions such that the output is low at V_{OL} except when disabled by the output enable control. The t_{PZH} and t_{PHZ} reference waveform is for the output under test with internal conditions such that the output is high at V_{OH} except when disabled by the output enable control.
3. C_L = 30 pF minimum or equivalent (includes test jig and probe capacitance).
4. R_T = 50Ω or equivalent, R_L = 500Ω or equivalent.
5. Input signal from pulse generator: V_{IN} = 0.0 V to V_{IH}; PRR ≤ 1 MHz; Z_O = 50Ω; t_r ≤ 2.0 ns; t_f ≤ 2.0 ns; t_r and t_f shall be measured from 10% of V_{IH} to 90% of V_{IH} and from 90% of V_{IH} to 10% of V_{IH}, respectively; duty cycle = 50 percent.
6. Timing parameters shall be tested at a minimum input frequency of 1 MHz.
7. The outputs are measured one at a time with one transition per measurement.

FIGURE 6. Switching waveforms and test circuit - Continued.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection

a. Tests shall be as specified in table II herein.

b. The test vectors used to verify the truth table shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth table in figure 3, herein. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

c. C_{IN}, C_{OUT}, and C_{PD} shall be measured only for initial qualification and after process or design changes which may affect capacitance. C_{IN} and C_{OUT} shall be measured between the designated terminal and GND at a frequency of 1 MHz. This test may be performed at 10 MHz and guaranteed, if not tested, at 1 MHz. The DC bias for the pin under test (V_{BIAS}) = 2.5 V or 3.0 V. For C_{IN}, C_{OUT}, and C_{PD}, test all applicable pins on five devices with zero failures.

For C_{IN} and C_{OUT}, a device manufacturer may qualify devices by functional groups. A specific functional group shall be composed of functional types, that by design, will yield the same capacitance values when tested in accordance with table IA, herein. The device manufacturer shall set a function group limit for the C_{IN} and C_{OUT} tests. The device manufacturer may then test one device functional group, to the limits and conditions specified herein. All other device functions in that particular functional group shall be guaranteed, if not tested, to the limits and test conditions specified in table IA, herein. The device manufacturers shall submit to DLA Land and Maritime-VA the device functions listed in each functional group and the test results for each device tested.

d. Ground and V_{CC} bounce tests are required for all device classes. These tests shall be performed only for initial qualification, after process or design changes which may affect the performance of the device, and any changes to the test fixture. V_{OLP}, V_{OLV}, V_{OHP}, and V_{OHV} shall be measured for the worst case outputs of the device. All other outputs shall be guaranteed, if not tested, to the limits established for the worst case outputs. The worst case outputs tested are to be determined by the manufacturer. Test 5 devices assembled in the worst case package type supplied to this document. All other package types shall be guaranteed, if not tested, to the limits established for the worst case package. The 5 devices to be tested shall be the worst case device type supplied to this drawing. All other device types shall be guaranteed, if not tested, to the limits established for the worst case device type. The package type and device type to be tested shall be determined by the manufacturer. The device manufacturer will submit to DLA Land and Maritime-VA data that shall include all measured peak values for each device tested and detailed oscilloscope plots for each V_{OLP}, V_{OLV}, V_{OHP}, and V_{OHV} from one sample part per function. The plot shall contain the waveforms of both a switching output and the output under test.

Each device manufacturer shall test product on the fixtures they currently use. When a new fixture is used, the device manufacturer shall inform DLA Land and Maritime-VA of this change and test the 5 devices on both the new and old test fixtures. The device manufacturer shall then submit to DLA Land and Maritime-VA data from testing on both fixtures, that shall include all measured peak values for each device tested and detailed oscilloscope plots for each V_{OLP}, V_{OLV}, V_{OHP}, and V_{OHV} from one sample part per function. The plot shall contain the waveforms of both a switching output and the output under test.

For V_{OLP}, V_{OLV}, V_{OHP}, and V_{OHV}, a device manufacturer may qualify devices by functional groups. A specific functional group shall be composed of function types, that by design, will yield the same test values when tested in accordance with table IA, herein. The device manufacturer shall set a functional group limit for the V_{OLP}, V_{OLV}, V_{OHP}, and V_{OHV} tests. The device manufacturer may then test one device function from a functional group, to the limits and conditions specified herein. All other device functions in that particular functional group shall be guaranteed, if not tested, to the limits and conditions specified in table IA, herein. The device manufacturers shall submit to DLA Land and Maritime-VA the device functions listed in each functional group and test results, along with the oscilloscope plots, for each device tested.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class Q	Device class V
Interim electrical parameters (see 4.2)	---	1
Final electrical parameters (see 4.2)	1/ 1, 2, 3, 7, 8, 9, 10, 11	2/ 3/ 1, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3	3/ 1, 2, 3, 7, 8, 9, 10 , 11
Group D end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3, 7, 9
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1, 7, and deltas.
3/ Delta limits, as specified in table III, shall be required where specified, and the delta limits shall be completed with reference to the zero hour electrical parameters.

TABLE III. Burn-in and operating life test, delta parameters (+25°C).

Parameter 1/	Symbol	Delta limits
Quiescent supply current	I_{CCH}, I_{CCL}, I_{CCZ}	±1 µA
Quiescent supply current delta	ΔI_{CC}	±0.2 mA
Input current low level	I_{IL}	±100 nA
Input current high level	I_{IH}	±100 nA
Output voltage low level (I_{OL} = 12 mA or 24 mA, V_{CC} = 3.0 V)	V_{OL}	±0.08 V
Output voltage high level (I_{OH} = -12 mA or -24 mA, V_{CC} = 3.0 V)	V_{OH}	±0.20 V

1/ These parameters shall be recorded before and after the required burn-in and life tests to determined delta limits.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table IA at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

c. RHA tests for device classes M, Q, and V for levels M, D, P, L, R, and F shall be performed through each level to determine at what levels the devices meet the RHA requirements. These RHA tests shall be performed for initial qualification and after design or process changes which may affect the RHA performance of the device.

d. Prior to irradiation, each selected sample shall be assembled in its qualified package. It shall pass the specified group A electrical parameters in table IA for subgroups specified in table II herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883, method 1019, condition A, and as specified herein. Prior to and during total dose irradiation characterization and testing, the devices for characterization shall be biased so that 50 percent are at inputs high and 50 percent are at inputs low, and the devices for testing shall be biased to the worst case condition established during characterization. Devices shall be biased as follows:

a. Inputs tested high, V_{CC} = 3.6 V dc ±5%, $V_{IN} = V_{CC}$, R_{IN} = 1 kΩ ±20%, and all outputs are open.
b. Inputs tested low, V_{CC} = 3.6 V dc ±5%, V_{IN} = 0.0 V, R_{IN} = 1 kΩ ±20%, and all outputs are open.

4.4.4.1.1 Accelerated anneal test. Accelerated anneal test shall be performed on classes M, Q, and V devices requiring an RHA level greater than 5K rad (Si). The post-anneal end-point electrical parameter limits shall be as specified in table IA herein and shall be the pre-irradiation end-point electrical parameter limit at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be performed on class V devices. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. Test four devices with zero failures. ASTM F1192 may be used as a guideline when performing SEP testing. The test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. 0° ≤ angle ≤ 60°). No shadowing of the ion beam due to fixturing or package related effects is allowed.
b. The fluence shall be ≥ 100 errors or ≥ 10^7 ions/cm^2.
c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.
d. The particle range shall be ≥ 20 microns in silicon.
e. The upset test temperature shall be +25°C. The latch-up test temperature shall be at the maximum rated operating temperature ±10°C.
f. Bias conditions shall be V_{CC} = 1.8 V dc for the upset measurements, and V_{CC} = 3.6 V dc for the latch-up measurements.
g. For SEP test limits, see table IB herein.

4.5 Methods of inspection. Methods of inspection shall be specified as follows:

4.5.1 Voltage and current. Unless otherwise specified, all voltages given are referenced to the microcircuit GND terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

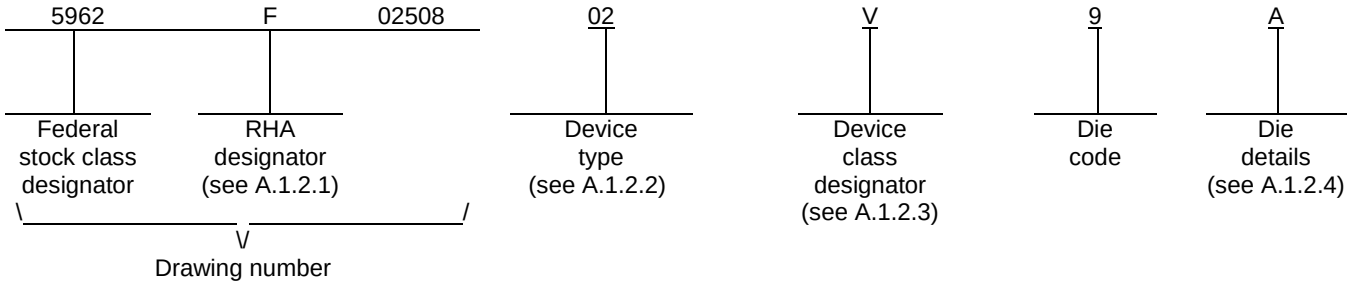
6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

APPENDIX A
APPENDIX A FORMS A PART OF SMD 5962-02508

A.1 SCOPE

A.1.1 Scope. This appendix establishes minimum requirements for microcircuit die to be supplied under the Qualified Manufacturers List (QML) Program. QML microcircuit die meeting the requirements of MIL-PRF-38535 and the manufacturers approved QM plan for use in monolithic microcircuits, multi-chip modules (MCMs), hybrids, electronic modules, or devices using chip and wire designs in accordance with MIL-PRF-38534 are specified herein. Two product assurance classes consisting of military high reliability (device class Q) and space application (device Class V) are reflected in the Part or Identification Number (PIN). When available a choice of Radiation Hardiness Assurance (RHA) levels is reflected in the PIN.

A.1.2 PIN. The PIN is as shown in the following example:



A.1.2.1 RHA designator. Device classes Q and V RHA identified die shall meet the MIL-PRF-38535 specified RHA levels. A dash (-) indicates a non-RHA die.

A.1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54VCXH162245	16-bit bus transceiver with bus hold, series output resistors on A side, and three-state outputs
02	54VCXH162245	16-bit bus transceiver with bus hold, series output resistors on A side, and three-state outputs

A.1.2.3 Device class designator.

Device class	Device requirements documentation
Q or V	Certification and qualification to the die requirements of MIL-PRF-38535.

A.1.2.4 Die Details. The die details designation shall be a unique letter which designates the die's physical dimensions, bonding pad location(s) and related electrical function(s), interface materials, and other assembly related information, for each product and variant supplied to this appendix.

A.1.2.4.1 Die physical dimensions.

Die type	Figure number
02	A-1

A.1.2.4.2 Die bonding pad locations and electrical functions.

Die type	Figure number
02	A-1

A.1.2.4.3 Interface materials.

Die type	Figure number
02	A-1

A.1.2.4.4 Assembly related information.

Die type	Figure number
02	A-1

A.1.3 Absolute maximum ratings. See paragraph 1.3 herein for details.

A.1.4 Recommended operating conditions. See paragraph 1.4 herein for details.

A.2 APPLICABLE DOCUMENTS.

A.2.1 Government specifications, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://quicksearch.dla.mil/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

A.2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

A.3 REQUIREMENTS

A.3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not effect the form, fit or function as described herein.

A.3.2 Design, construction and physical dimensions. The design, construction and physical dimensions shall be as specified in MIL-PRF-38535 and the manufacturer's QM plan, for device classes Q and V and herein.

A.3.2.1 Die physical dimensions. The die physical dimensions shall be as specified in A.1.2.4.1 and on figure A-1.

A.3.2.2 Die bonding pad locations and electrical functions. The die bonding pad locations and electrical functions shall be as specified in A.1.2.4.2 and on figure A-1.

A.3.2.3 Interface materials. The interface materials for the die shall be as specified in A.1.2.4.3 and on figure A-1.

A.3.2.4 Assembly related information. The assembly related information shall be as specified in A.1.2.4.4 and figure A-1.

A.3.2.5 Truth table. The truth table shall be as defined in paragraph 3.2.3 herein.

A.3.2.6 Radiation exposure circuit. The radiation exposure circuit shall be as defined in paragraph 3.2.6 herein.

A.3.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table IA of the body of this document.

A.3.4 Electrical test requirements. The wafer probe test requirements shall include functional and parametric testing sufficient to make the packaged die capable of meeting the electrical performance requirements in table IA.

A.3.5 Marking. As a minimum, each unique lot of die, loaded in single or multiple stack of carriers, for shipment to a customer, shall be identified with the wafer lot number, the certification mark, the manufacturer's identification and the PIN listed in A.1.2 herein. The certification mark shall be a "QML" or "Q" as required by MIL-PRF-38535.

A.3.6 Certification of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see A.6.4 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this appendix shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and the requirements herein.

A.3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuit die delivered to this drawing.

A.4 VERIFICATION

A.4.1 Sampling and inspection. For device classes Q and V, die sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modifications in the QM plan shall not effect the form, fit or function as described herein.

A.4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and as defined in the manufacturer's QM plan. As a minimum it shall consist of:

a) Wafer lot acceptance for Class V product using the criteria defined in MIL-STD-883, method 5007.

b) 100% wafer probe (see paragraph A.3.4 herein).

c) 100% internal visual inspection to the applicable class Q or V criteria defined in MIL-STD-883 method 2010 or the alternate procedures allowed in MIL-STD-883, method 5004.

A.4.3 Conformance inspection.

A.4.3.1 Group E inspection. Group E inspection is required only for parts intended to be identified as radiation assured (see A.3.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End point electrical testing of packaged die shall be as specified in table II herein. Group E tests and conditions are as specified in paragraphs 4.4.4 herein.

A.5 DIE CARRIER

A.5.1 Die carrier requirements. The requirements for the die carrier shall be accordance with the manufacturer's QM plan or as specified in the purchase order by the acquiring activity. The die carrier shall provide adequate physical, mechanical and electrostatic protection.

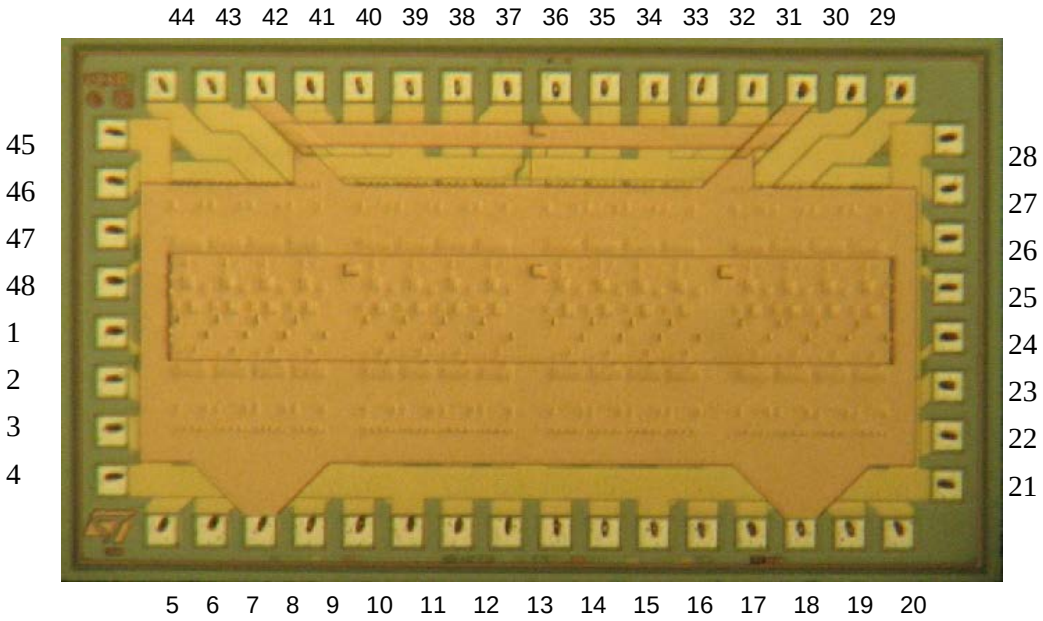
A.6 NOTES

A.6.1 Intended use. Microcircuit die conforming to this drawing are intended for use in microcircuits built in accordance with MIL-PRF-38535 or MIL-PRF-38534 for government microcircuit applications (original equipment), design applications and logistics purposes.

A.6.2 Comments. Comments on this appendix should be directed to DLA Land and Maritime-VA, Columbus, Ohio, 43218-3990 or telephone (614)-692-0547.

A.6.3 Abbreviations, symbols and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

A.6.4 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed within QML-38535 have submitted a certificate of compliance (see A.3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.



Note: Pad numbers reflect terminal numbers when placed in Case Outline X and Y see figure 1.

FIGURE A-1. Die bonding pad locations and electrical functions.

Die physical dimensions.

Die size:	2450 μm x 1440 μm	
Die thickness:	280 μm	

Interface materials.

Top to bottom metallization:	Si Al Cu	
Backside metallization:	None (lapped Si)	

Glassivation.

Type:	Nitride	6000Å
	Pvapox	5000Å

Substrate:	Silicon

Assembly related information.

Substrate potential:	Floating or tied to ground
Special assembly instructions:	Bond pad # 42 first.

FIGURE A-1. Die bonding pad locations and electrical functions - Continued.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 18-03-22

Approved sources of supply for SMD 5962-02508 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962R0250801QXA	3/	RHRXH162245K02Q
5962R0250801QXC	3/	RHRXH162245K01Q
5962R0250801VXA	3/	RHRXH162245K02V
5962R0250801VXC	3/	RHRXH162245K01V
5962R0250802QXA	3/	RHRXH162245K04Q
5962R0250802QXC	3/	RHRXH162245K03Q
5962R0250802VXA	3/	RHRXH162245K04V
5962R0250802VXC	F8859	RHRXH162245K03V
5962F0250801QXA	3/	RHFXH162245K02Q
5962F0250801QXC	3/	RHFXH162245K01Q
5962F0250801VXA	3/	RHFXH162245K02V
5962F0250801VXC	3/	RHFXH162245K01V
5962F0250802QXA	3/	RHFXH162245K04Q
5962F0250802QXC	3/	RHFXH162245K03Q
5962F0250802VXA	3/	RHFXH162245K04V
5962F0250802VXC	F8859	RHFXH162245K03V
5962F0250802VYC	F8859	RHFXH162245K05V
5962F0250802V9A	F8859	RHFXH162245D2V

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed, contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available from an approved source and supply.

Vendor CAGE number	Vendor name and address
F8859	STMicroelectronics 3 rue de Suisse CS 60816 35208 RENNES cedex2-FRANCE

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.