STA321MP

Scalable digital microphone processor

Datasheet - production data

TQFP64
10 mm x 10 mm

Features

- 8 digital processing channels each 24-bits
  - 6 channels of PDM input
  - 2 additional virtual channels
- >100 dB SNR and dynamic range
- Digital gain/attenuation 58 dB to -100 dB in 0.5 dB steps
- Soft volume update
- Individual channel and master level control
- Up to 10 independent 32-bit user-programmable biquads (EQ) per channel
- Bass/treble tone control
- Pre- and post-EQ full 8-channel input mix on all 8 channels
- Dual independent limiters/compressors
- Dynamic range compression or anti-clipping modes
- Individual channel and master soft/hard mute
- 3 I²S data outputs
- I²S data output channel mapping function
- Independent channel volume and DSP bypass
- Channel mapping of any input to any processing channel

Applications

- Tablets
- Gaming
- Audio conference sets
- Legacy microphone-equipped devices

Description

The STA321MP is a PDM, high-performance, multichannel processor with ultra-low quiescent current. It is designed for general-purpose digital microphone applications. The device is fully digital and is comprised of three main sections. The first section is the PDM input interface which can accept up to six serial digital inputs. The second section is a high-quality audio processor allowing flexible channel mixing/muxing and provides up to 10 biquads for general sound equalization and voice enhancement with independent volume control. The last block is the I²S output interface which streams out the processed digital audio. The output interface can also be programmed for flexible channel mapping. The device offers some of the most commonly required audio enhancements such as programmable voice tuning and equalization, limiter/compressor for improved voice quality, multiband selection for customizable microphone usage, and configurable wind-noise rejection. The embedded digital processor allows the microphone processing to be offloaded from the main CPU or SoC to the device.

Table 1. Device summary

Order code	Package	Packaging
STA321MPLTR	TQFP64	Tape and reel

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Contents

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1 Block diagram

Figure 1. Block diagram

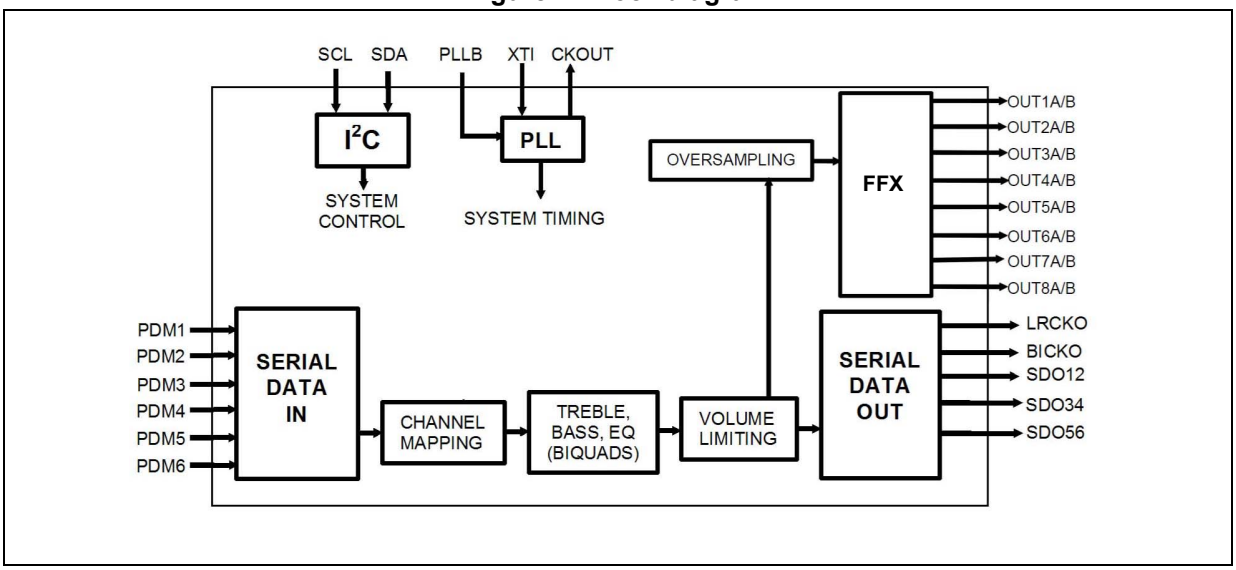
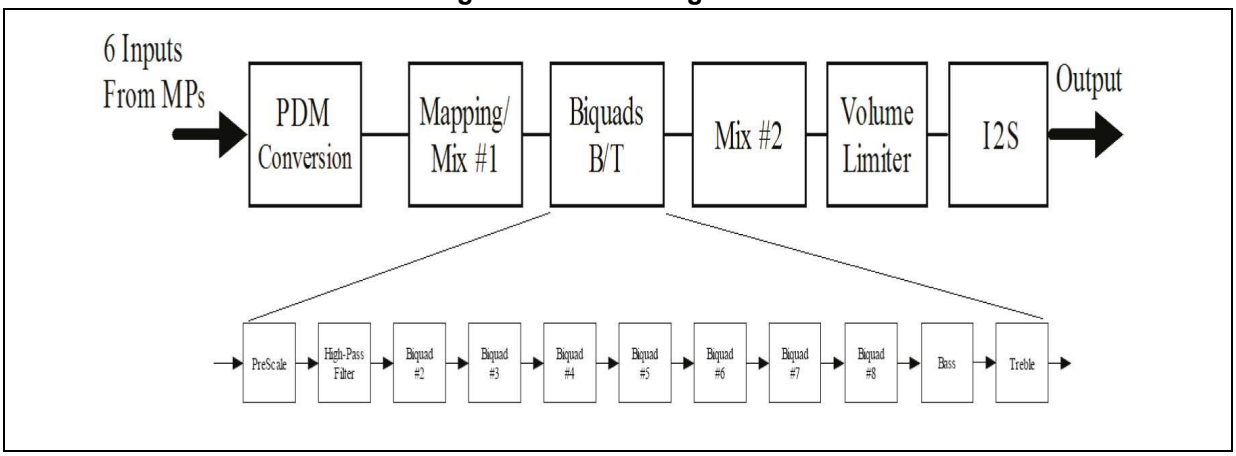


Figure 2. Channel signal flow



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2 Pin connections

Figure 3. Pin connections (top view)

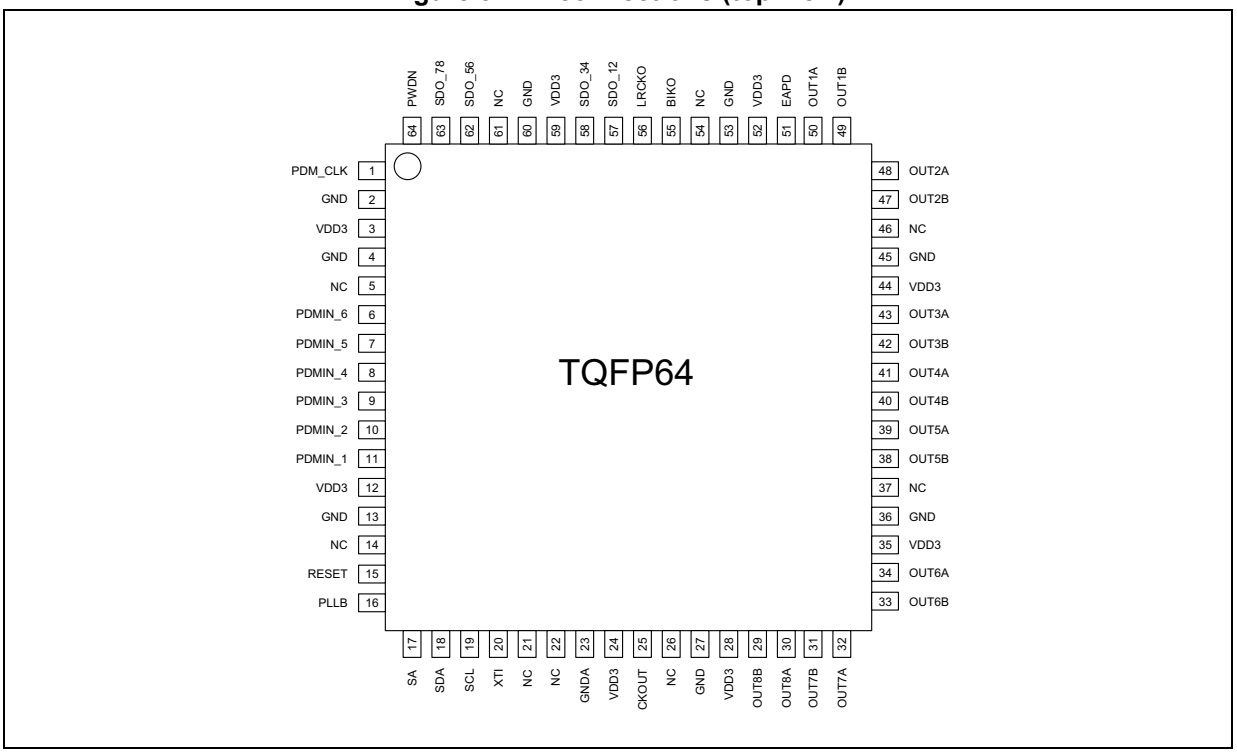

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Table 2. Pin description

Pin number	Type	Name	Description
1	5-V tolerant TTL input buffer	PDM_CLK	PDM I/F CLK
6		PDMIN_6	PDM input channel 6
7		PDMIN_5	PDM input channel 5
8		PDMIN_4	PDM input channel 4
9		PDMIN_3	PDM input channel 3
10		PDMIN_2	PDM input channel 2
11		PDMIN_1	PDM input channel 1
15	5-V tolerant TTL Schmitt trigger input buffer	RESET	Global reset
16	CMOS input buffer with pull-down	PLLB	Bypass phase-locked loop
17		SA	Connect to GND
18	Bidirectional buffer: 5-V tolerant TTL Schmitt trigger input; 3.3-V capable 2 mA slew-rate controlled output	SDA	Serial data (I^2C)
19	5-V tolerant TTL Schmitt trigger input buffer	SCL	Serial clock (I^2C)
20		XTI	Crystal oscillator input (clock input)
23	Analog ground	GNDA	PLL ground
25	3.3-V capable TTL tristate 4 mA output buffer	CKOUT	Clock output
29	3.3-V capable TTL 2 mA output buffer	OUT8B	PWM channel 8 output B
30		OUT8A	PWM channel 8 output A
31		OUT7B	PWM channel 7 output B
32		OUT7A	PWM channel 7 output A
33		OUT6B	PWM channel 6 output B
34		OUT6A	PWM channel 6 output A
38		OUT5B	PWM channel 5 output B
39		OUT5A	PWM channel 5 output A
40		OUT4B	PWM channel 4 output B
41		OUT4A	PWM channel 4 output A
42		OUT3B	PWM channel 3 output B
43		OUT3A	PWM channel 3 output A
47		OUT2B	PWM channel 2 output B
48		OUT2A	PWM channel 2 output A
49		OUT1B	PWM channel 1 output B
50		OUT1A	PWM channel 1 output A
51	3.3-V capable TTL 4 mA output buffer	EAPD	Ext. amp power-down
55	3.3-V capable TTL 2 mA output buffer	BICKO	Output serial clock

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Table 2. Pin description (continued)

Pin number	Type	Name	Description
56	3.3-V capable TTL 2 mA output buffer	LRCKO	Output left/right clock
57		SDO_12	Output serial data channels 1 and 2
58		SDO_34	Output serial data channels 3 and 4
62		SDO_56	Output serial data channels 5 and 6
63		SDO_78	Output serial data channels 7 and 8
64	5-V tolerant TTL Schmitt trigger input buffer	PWDN	Device power-down
3, 12, 24, 28, 35, 44, 52, 59	3.3-V digital supply voltage	VDD3	3.3-V supply
2, 4, 13, 27, 36, 45, 53, 60	Digital ground	GND	Ground
14, 21, 22, 26, 37, 46, 54, 61, 63		NC	Not connected

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3 Electrical characteristics

3.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	3.3-V I/O power supply	-0.5	—	4	V
V_{DDA}	3.3-V logic power supply	-0.5		4	
V_i	Voltage on input pins	-0.5		VDD + 0.5	
V_o	Voltage on output pins	-0.5		VDD + 0.3	
T_{stg}	Storage temperature	-40		150	°C
T_{amb}	Ambient operating temperature	-40		90	

3.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Min	Typ	Max	Unit
$R_{thj\text{-}case}$	Thermal resistance, junction-case (thermal pad)	—	—	1.5	°C/W

3.3 Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	I/O power supply	3.0	—	3.6	V
V_{DDA}	Logic power supply	3.0		3.6	
T_j	Operating junction temperature	-40		125	°C

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3.4 Electrical specifications

The following specifications are valid for V_{DD} = 3.3 V ± 0.3 V, V_{DDA} = 3.3 V ± 0.3 V and Tamb = 0 to 70 °C, unless otherwise stated

Table 6. General interface electrical specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{il}	Low-level input no pull-up	V_i = 0 V			1 (1)	
I_{ih}	High-level input no pull-down	$V_i = V_{DD}$			2	µA
I_{OZ}	Tristate output leakage without pull-up/down	$V_i = V_{DD}$		—	2	
V_{esd}	Electrostatic protection (human body model)	Leakage < 1µA	2000			V

1. The leakage currents are generally very small, < 1 nA. The values given here are maximum after an electrostatic stress on the pin.

Table 7. DC electrical characteristics: 3.3-V buffers

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Low-level input voltage				0.8	
V_{IH}	High-level input voltage		2.0			
V_{ILhyst}	Low-level threshold	Input falling	0.8		1.35	
V_{IHhyst}	High-level threshold	Input rising	1.3		2.0	
V_{hyst}	Schmitt trigger hysteresis		0.3	—	0.8	V
V_{ol}	Low-level output	I_{ol} = 100 µA			0.2	
V_{oh}	High-level output	I_{oh} = -100 µA	VDD-0.2			
		I_{oh} = -2 mA	2.4			

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4 Pin description

PDM interface clock (PDM_CLK)

The clock to the PDM interface is provided on this pin and is used by the device to sample the digital microphone data. This clock must be used to clock both the interface and the microphones. The clock frequency must not exceed the upper limit of the microphone's specific clock frequency (please refer to the datasheet of the specific microphone used).

PDM input channels (PDMIN_1/6)

Audio information enters the device through the PDM input channels. These input pins receive the digital output signal from the microphones.

RESET

Driving this pin low turns off the outputs and returns all settings to their defaults.

I^2C bus

The SDA and SCL pins operate per the Phillips I^2C specification. See *Section 5: I^2C bus operation*.

Phase-locked loop (PLL)

The phase-locked loop section provides the system timing signals and CKOUT.

Clock output (CKOUT)

System synchronization and master clocks are provided by CKOUT. This clock can be conveniently divided and then used to clock both the PDM interface and the microphones. Please refer to *Figure 6.*

PWM outputs (OUT1 through OUT8)

The PWM outputs provide the input signal for the power devices.

Serial data out (SDO_12, SDO_34, SDO_56, SDO_78)

These are the outputs for audio information. Six different formats are available including I^2S, left- or right-justified, LSB or MSB first, with word widths of 16, 18, 20 and 24 bits.

Device power-down (PWDN)

Pulling PWDN low begins the power-down sequence which puts the STA321MP into a low-power state. EAPD (pin 51) goes low approximately 30 ms later.

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5 I²C bus operation

The STA321MP supports the I²C protocol via the input ports SCL and SDA_IN (master to slave) and the output port SDA_OUT (slave to master).

This protocol defines any device that sends data to the bus as a transmitter and any device that reads data as a receiver.

The device that controls the data transfer is known as the master and the other is called the slave. The master always starts the transfer and provides the serial clock for synchronization. The STA321MP is a slave device in all of its communications.

5.1 Communication protocol

5.1.1 Data transition or change

Data changes on the SDA line must only occur when the SCL clock is low. SDA transition while the clock is high is used to identify a START or STOP condition.

5.1.2 Start condition

START is identified by a high to low transition of the data bus SDA signal while the clock signal SCL is stable in the high state. A START condition must precede any command for data transfer.

5.1.3 Stop condition

STOP is identified by a low to high transition of the data bus SDA signal while the clock signal SCL is stable in the high state. A STOP condition terminates communication between STA321MP and the bus master.

5.1.4 Data input

During data input, the STA321MP samples the SDA signal on the rising edge of the SCL clock.

For correct device operation, the SDA signal must be stable during the rising edge of the clock and the data can change only when the SCL line is low.

5.2 Device addressing

To start communication between the master and the Omega FFX core, the master must initiate with a start condition. Following this, the master sends 8 bits to the SDA line (MSB first) corresponding to the device select address and read or write mode.

The 7 most significant bits are the device address identifiers, corresponding to the I²C bus definition. In the STA321MP the I²C interface has two device addresses depending on the SA port configuration, 0x40 or 0100000x when SA = 0, and 0x42 or 0100001x when SA = 1.

The 8th bit (LSB) identifies a read or write operation RW, this bit is set to 1 in read mode and 0 for write mode. After a START condition the STA321MP identifies on the bus the device

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address and if a match is found, it acknowledges the identification on the SDA bus during the 9th-bit time. The byte following the device identification byte is the internal space address.

5.3 Write operation

Following the START condition, the master sends a device select code with the RW bit set to 0. The STA321MP acknowledges this and then waits for the byte of the internal address.

After receiving the internal byte address the STA321MP again responds with an acknowledgment.

5.3.1 Byte write

In byte write mode, the master sends one data byte, which is acknowledged by the FFX core. The master then terminates the transfer by generating a STOP condition.

5.3.2 Multi-byte write

The multi-byte write modes can start from any internal address. The master generating a STOP condition terminates the transfer.

Figure 4. Write mode sequence

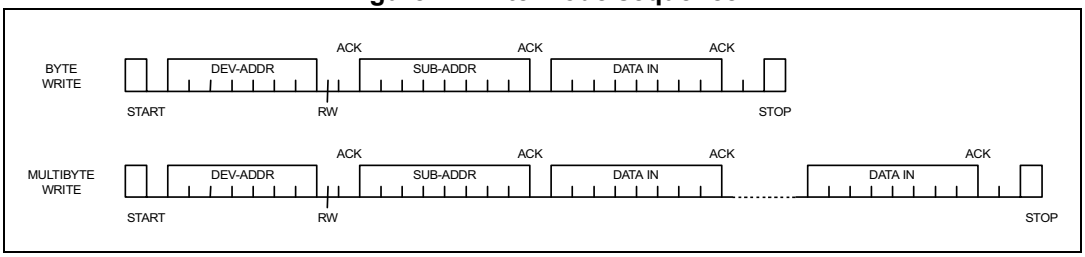
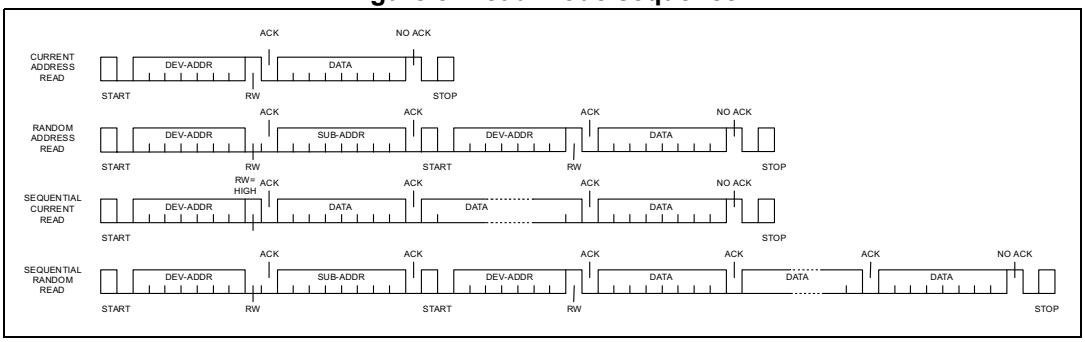


Figure 5. Read mode sequence



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6 Application reference schematic

Figure 6. Reference schematic for STA321MP-based application

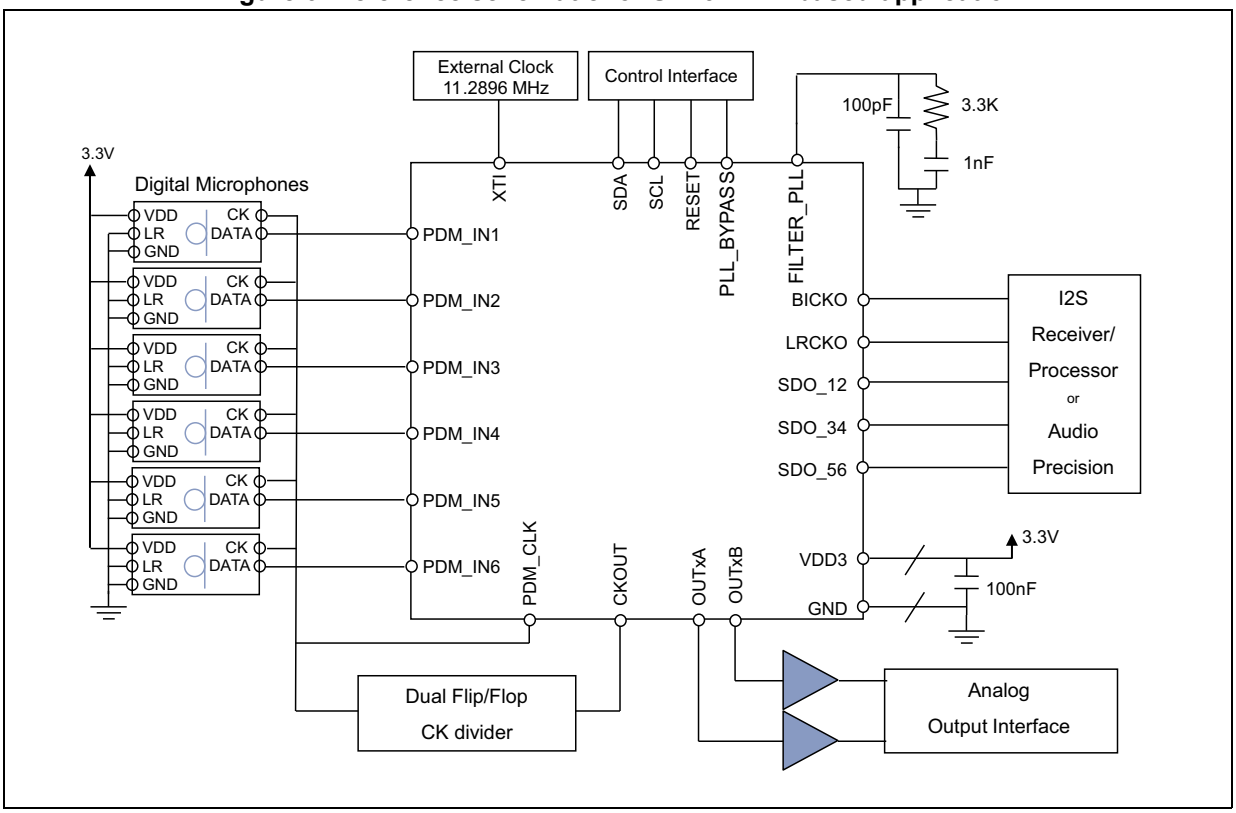
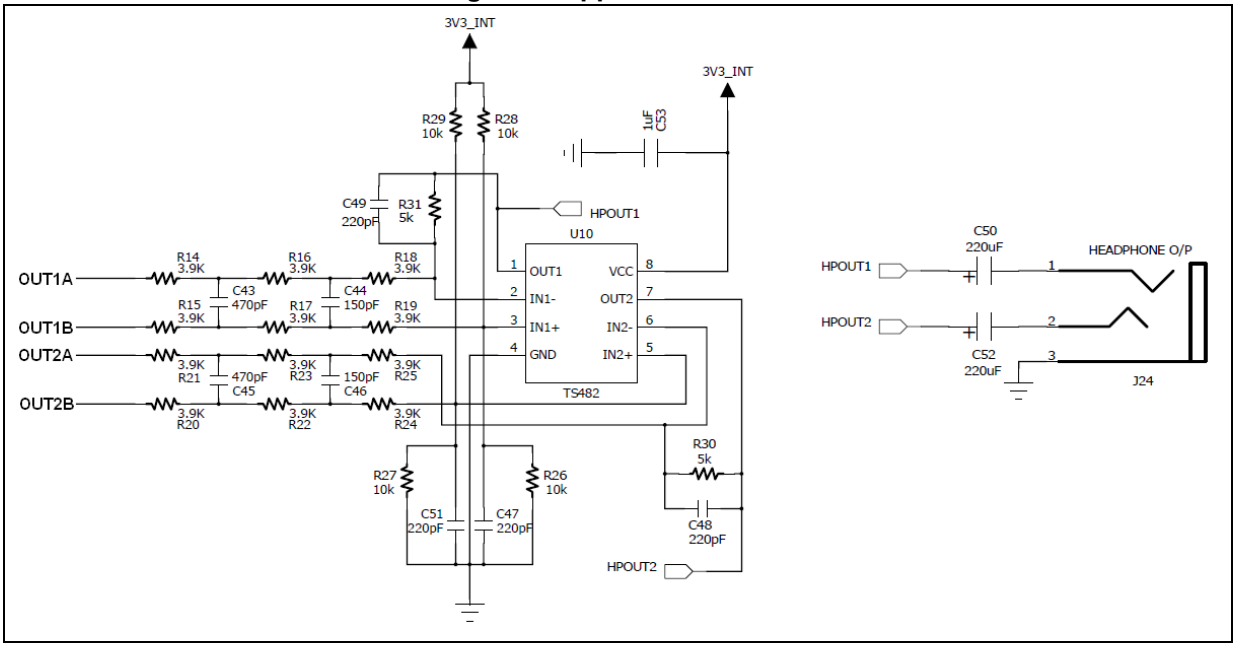


Figure 7. Application circuit



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7 Registers

7.1 Register summary

Table 8. Register summary

Addr	Name	D7	D6	D5	D4	D3	D2	D1	D0
Configuration									
0x00	CONFA	COS1	COS0	DSPB	IR1	IR0	MCS2	MCS1	MCS0
0x01	ConfB				SAIFB	SAI3	SAI2	SAI1	SAI0
0x02	ConfC				SAOFB	SAO3	SAO2	SAO1	SAO0
0x03	ConfD	MPC	CSZ4	CSZ3	CSZ2	CSZ1	CSZ0	OM1	OM0
0x04	ConfE	C8BO	C7BO	C6BO	C5BO	C4BO	C3BO	C2BO	C1BO
0x05	ConfF	PWMS2	PWMS1	PWMS0	BQL	PSL	DEMP	DRC	HPB
0x06	ConfG	MPCV	DCCV	HPE	AM2E	AME	COD	SID	PWMD
0x07	ConfH	ECLE	LDTE	BCLE	IDE	ZDE	SVE	ZCE	NSBW
0x08	ConfI	EAPD							PSCE
Volume control									
0x09	MMUTE								MMUTE
0x0A	Mvol	MV7	MV6	MV5	MV4	MV3	MV2	MV1	MV0
0x0B	C1Vol	C1V7	C1V6	C1V5	C1V4	C1V3	C1V2	C1V1	C1V0
0x0C	C2Vol	C2V7	C2V6	C2V5	C2V4	C2V3	C2V2	C2V1	C2V0
0x0D	C3Vol	C3V7	C3V6	C3V5	C3V4	C3V3	C3V2	C3V1	C3V0
0x0E	C4Vol	C4V7	C4V6	C4V5	C4V4	C4V3	C4V2	C4V1	C4V0
0x0F	C5Vol	C5V7	C5V6	C5V5	C5V4	C5V3	C5V2	C5V1	C5V0
0x10	C6Vol	C6V7	C6V6	C6V5	C6V4	C6V3	C6V2	C6V1	C6V0
0x11	C7Vol	C7V7	C7V6	C7V5	C7V4	C7V3	C7V2	C7V1	C7V0
0x12	C8Vol	C8V7	C8V6	C8V5	C8V4	C8V3	C8V2	C8V1	C8V0
0x13	C1VTMB	C1M	C1VBP		C1VT4	C1VT3	C1VT2	C1VT1	C1VT0
0x14	C2VTMB	C2M	C2VBP		C2VT4	C2VT3	C2VT2	C2VT1	C2VT0
0x15	C3VTMB	C3M	C3VBP		C3VT4	C3VT3	C3VT2	C3VT1	C3VT0
0x16	C4VTMB	C4M	C4VBP		C4VT4	C4VT3	C4VT2	C4VT1	C4VT0
0x17	C5VTMB	C5M	C5VBP		C5VT4	C5VT3	C5VT2	C5VT1	C5VT0
0x18	C6VTMB	C6M	C6VBP		C6VT4	C6VT3	C6VT2	C6VT1	C6VT0
0x19	C7VTMB	C7M	C7VBP		C7VT4	C7VT3	C7VT2	C7VT1	C7VT0
0x1A	C8VTMB	C8M	C8VBP		C8VT4	C8VT3	C8VT2	C8VT1	C8VT0

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Table 8. Register summary (continued)

Addr	Name	D7	D6	D5	D4	D3	D2	D1	D0
Input mapping									
0x1B	C12im		C2IM2	C2IM1	C2IM0		C1IM2	C1IM1	C1IM0
0x1C	C34im		C4IM2	C4IM1	C4IM0		C3IM2	C3IM1	C3IM0
0x1D	C56im		C6IM2	C6IM1	C6IM0		C5IM2	C5IM1	C5IM0
0x1E	C78im		C8IM2	C8IM1	C8IM0		C7IM2	C7IM1	C7IM0
Processing loop									
0x28	BQlp	C8BLP	C7BLP	C6BLP	C5BLP	C4BLP	C3BLP	C2BLP	C1BLP
0x29	MXlp	C8MXLP	C7MXLP	C6MXLP	C5MXLP	C4MXLP	C3MXLP	C2MXLP	C1MXLP
Processing bypass									
0x2A	EQbp	C8EQBP	C7EQBP	C6EQBP	C5EQBP	C4EQBP	C3EQBP	C2EQBP	C1EQBP
0x2B	ToneBP	C8TCB	C7TCB	C6TCB	C5TCB	C4TCB	C3TCB	C2TCB	C1TCB
Tone control									
0x2C	Tone	TTC3	TTC2	TTC1	TTC0	BTC3	BTC2	BTC1	BTC0
PWM output timing									
0x33	C12ot		C2OT2	C2OT1	C2OT0		C1OT2	C1OT1	C1OT0
0x34	C34ot		C4OT2	C4OT1	C4OT0		C3OT2	C3OT1	C3OT0
0x35	C56ot		C6OT2	C6OT1	C6OT0		C5OT2	C5OT1	C5OT0
0x36	C78ot		C8OT2	C8OT1	C8OT0		C7OT2	C7OT1	C7OT0
I^2S output channel mapping									
0x37	C12om		C2OM2	C2OM1	C2OM0		C1OM2	C1OM1	C1OM0
0x38	C34om		C4OM2	C4OM1	C4OM0		C3OM2	C3OM1	C3OM0
0x39	C56om		C6OM2	C6OM1	C6OM0		C5OM2	C5OM1	C5OM0
0x3A	C78om		C8OM2	C8OM1	C8OM0		C7OM2	C7OM1	C7OM0
User-defined coefficient RAM									
0x3B	Cfaddr1							CFA9	CFA8
0x3C	Cfaddr2	CFA7	CFA6	CFA5	CFA4	CFA3	CFA2	CFA1	CFA0
0x3D	B1cf1	C1B23	C1B22	C1B21	C1B20	C1B19	C1B18	C1B17	C1B16
0x3E	B1cf2	C1B15	C1B14	C1B13	C1B12	C1B11	C1B10	C1B9	C1B8
0x3F	B1cf3	C1B7	C1B6	C1B5	C1B4	C1B3	C1B2	C1B1	C1B0
0x40	B2cf1	C2B23	C2B22	C2B21	C2B20	C2B19	C2B18	C2B17	C2B16
0x41	B2cf2	C2B15	C2B14	C2B13	C2B12	C2B11	C2B10	C2B9	C2B8
0x42	B2cf3	C2B7	C2B6	C2B5	C2B4	C2B3	C2B2	C2B1	C2B0
0x43	A1cf1	C3B23	C3B22	C3B21	C3B20	C3B19	C3B18	C3B17	C3B16

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Table 8. Register summary (continued)

Addr	Name	D7	D6	D5	D4	D3	D2	D1	D0
0x44	A1cf2	C3B15	C3B14	C3B13	C3B12	C3B11	C3B10	C3B9	C3B8
0x45	A1cf3	C3B7	C3B6	C3B5	C3B4	C3B3	C3B2	C3B1	C3B0
0x46	A2cf1	C4B23	C4B22	C4B21	C4B20	C4B19	C4B18	C4B17	C4B16
0x47	A2cf2	C4B15	C4B14	C4B13	C4B12	C4B11	C4B10	C4B9	C4B8
0x48	A2cf3	C4B7	C4B6	C4B5	C4B4	C4B3	C4B2	C4B1	C4B0
0x49	B0cf1	C5B23	C5B22	C5B21	C5B20	C5B19	C5B18	C5B17	C5B16
0x4A	B0cf2	C5B15	C5B14	C5B13	C5B12	C5B11	C5B10	C5B9	C5B8
0x4B	B0cf3	C5B7	C5B6	C5B5	C5B4	C5B3	C5B2	C5B1	C5B0
0x4C	Cfud							WA	W1
0x4D	MPCC1	MPCC15	MPCC14	MPCC13	MPCC12	MPCC11	MPCC10	MPCC9	MPCC8
0x4E	MPCC2	MPCC7	MPCC6	MPCC5	MPCC4	MPCC3	MPCC2	MPCC1	MPCC0
0x4F	DCC1	DCC15	DCC14	DCC13	DCC12	DCC11	DCC10	DCC9	DCC8
0x50	DCC2	DCC7	DCC6	DCC5	DCC4	DCC3	DCC2	DCC1	DCC0
0x51	PSC1	RCV11	RCV10	RCV9	RCV8	RCV7	RCV6	RCV5	RCV4
0x52	PSC2	RCV3	RCV2	RCV1	RCV0	CNV11	CNV10	CNV9	CNV8
0x53	PSC3	CNV7	CNV6	CNV5	CNV4	CNV3	CNV2	CNV1	CNV0

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7.2 Register description

7.2.1 Configuration register A (0x00)

D7	D6	D5	D4	D3	D2	D1	D0
COS1	COS0	DSPB	IR1	IR0	MCS2	MCS1	MCS0
1	0	0	0	0	0	1	1

Bit	RW	RST	Name	Description
0	RW	1	MCS0	Master clock select: selects the ratio between the input sampling frequency (PDM I/FCLK) and the input clock(XTI).
1	RW	1	MCS1	
2	RW	0	MCS2	

The STA321MP supports a sampling rate of 2.8224 MHz. Therefore the internal clock is:

- 90.3168 MHz for the respective sampling frequency

The external clock frequency provided to the XTI pin must be a multiple of the input sampling frequency (fs). The relationship between the input clock and the input sampling rate is determined by both the MCSn and the IRn (input rate) register bits. The MCSn bits determine the PLL factor generating the internal clock and the IRn bits determine the oversampling ratio used internally.

Input sampling rate *fs* (kHz)	IR	MCS[2:0]				
		1XX	011	010	001	000
PDM I/F 2822.4	11	2 * fs	4 * fs	6 * fs	8 * fs	10 * fs

Interpolation ratio select

Bit	RW	RST	Name	Description
3	RW	0	IR0	Interpolation ratio select: selects the internal interpolation ratio based on the input sampling frequency
4	RW	0	IR1	

The STA321MP has variable interpolation (oversampling) settings such that internal processing and FFX output rates remain consistent. The first processing block interpolates by either 4 times, 2 times, or 1 time (pass-through).

The oversampling ratio of this interpolation is determined by the IR bits.

IR[1,0]	Input sampling rate *Fs* (kHz)	1st stage interpolation ratio
11	2822.4	PDM CLK to 176.4 kHz conversion

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Bit	RW	RST	Name	Description
0	RW	0	DSPB	DSP bypass bit: 0: normal operation 1: bypass of biquad and bass/treble functions

Setting the DSPB bit bypasses the biquad function of the FFX core.

COS[1,0]	CKOUT frequency
00	PLL output
01	PLL output/4
10	PLL output/8
11	PLL output/16

Application example:

- External clock: XTI = 11.2896 MHz
- COS[1,0] = 10: CKOUT = 90.3168 MHz/8 = 11.2896 MHz
- External Dual Flip Flop PDM I/F = CKOUT/4 = 2.8224 MHz, also provided to the microphones
- MCS[2:0] = 011: XTI/Fs = 4

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7.2.2 Configuration register C (0x02) - serial output formats

D7	D6	D5	D4	D3	D2	D1	D0
			SAOFB	SAO3	SAO2	SAIO	SAO0
			0	0	0	0	0

Bit	RW	RST	Name	Description
0	RW	0	SAO0	Serial audio output interface format: determines the interface format of the output serial digital audio interface.
1	RW	0	SAO1	
2	RW	0	SAO2	
3	RW	0	SAO3	

The STA321MP features a serial audio output interface that consists of 8 channels.

The serial audio output acts as a master with an output sampling frequency of 176.4 kHz. The output serial format can be selected independently from the input format and is done via the SAO and SAOFB bits.

Bit	RW	RST	Name	Description
4	RW	0	SAOFB	Determines MSB or LSB first for all SAO formats: 0: MSB first 1: LSB first

BICKI = BICKO	SAO[3:0]	Interface data format
32 * fs	0111	I^2S data
	1111	Left/right-justified 16-bit data
48 * fs	1110	I^2S data
	0001	Left-justified data
	1010	Right-justified 24-bit data
	1011	Right-justified 20-bit data
	1100	Right-justified 18-bit data
	1101	Right-justified 16-bit data
64 * fs	0000	I^2S data
	0001	Left-justified data
	0010	Right-justified 24-bit data
	0011	Right-justified 20-bit data
	0100	Right-justified 18-bit data
	0101	Right-justified 16-bit data

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7.2.3 Configuration register E (0x04)

D7	D6	D5	D4	D3	D2	D1	D0
C8BO	C7BO	C6BO	C5BO	C4BO	C3BO	C2BO	C1BO
0	0	0	0	0	0	0	0

Bit	RW	RST	Name	Description
0	RW	0	C1BO	Channels 1, 2, 3, 4, 5, 6, 7, and 8 binary output mode enable bits. A setting of 0 indicates ordinary FFX tristate output. A setting of 1 indicates binary output mode.
1	RW	0	C2BO	
2	RW	0	C3BO	
3	RW	0	C4BO	
4	RW	0	C5BO	
5	RW	0	C6BO	
6	RW	0	C7BO	
7	RW	0	C8BO	

Each individual channel output can be set to output a binary PWM stream. In this mode, output A of a channel is considered the positive output and output B is considered the negative output.

7.2.4 Configuration register F (0x05)

D7	D6	D5	D4	D3	D2	D1	D0
PWMS2	PWMS1	PWMS0	BQL	PSL	DEMP	DRC	HPB
0	0	0	0	0	0	0	0

Bit	RW	RST	Name	Description
0	RW	0	HPB	High-pass filter bypass bit: a setting of 1 bypasses the internal AC coupling digital high-pass filter

The STA321MP features an internal digital high-pass filter for the purpose of AC coupling. The purpose of this filter is to prevent DC signals from passing through an FFX amplifier. DC signals can cause speaker damage.

If HPB = 1, then the filter that the high-pass filter utilizes is made available as user-programmable biquad#1.

Bit	RW	RST	Name	Description
1	RW	0	DRC	Dynamic range compression/anti-clipping 0: limiters act in anti-clipping mode 1: limiters act in dynamic range compression mode

Both limiters can be used in one of two ways, anti-clipping or dynamic range compression. When used in anti-clipping mode, the limiter threshold values are constant and dependent on the limiter settings.

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In dynamic range compression mode the limiter threshold values vary with the volume settings, allowing a nighttime listening mode that provides a reduction in the dynamic range regardless of the volume level.

Bit	RW	RST	Name	Description
2	RW	0	DEMP	De-emphasis: 0: no de-emphasis 1: de-emphasis

By setting this bit to one, de-emphasis is implemented on all channels. When de-emphasis is used, it takes the place of biquad #7 in each channel and any coefficients using biquad #1 are ignored. The DSPB (DSP bypass) bit must be set to 0 for de-emphasis to function.

Bit	RW	RST	Name	Description
3	RW	0	PSL	Post-scale link: 0: each channel uses individual post-scale values 1: each channel uses channel 1 post-scale values

Post-scale functionality can be used for power-supply error correction. For multi-channel applications running off the same power-supply, the post-scale values can be linked to the value of channel 1 for ease of use and in order to update the values faster.

Bit	RW	RST	Name	Description
4	RW	0	BQL	Biquad link: 0: each channel uses coefficient values 1: each channel uses channel 1 coefficient values

For ease of use, all channels can use the biquad coefficients loaded into the channel 1 Coefficient RAM space by setting the BQL bit to 1. Therefore, any EQ updates only have to be performed once.

Bit	RW	RST	Name	Description
7:5	RW	00	PWMS[2:0]	PWM speed selection

PWMS[1:0]	PWM output speed
000	Normal speed (384 kHz) (all channels)
001	Half-speed (192 kHz) (all channels)
010	Double-speed (768 kHz) (all channels)
011	Normal speed (channels 1-6), double-speed (channels 7-8)
100	Odd speed (341.3 kHz) (all channels)

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7.2.5 Configuration register G (0x06)

D7	D6	D5	D4	D3	D2	D1	D0
MPCV	DCCV	HPE	AM2E	AME	COD	SID	PWMD
0	0	0	0	0	0	0	0

Bit	RW	RST	Name	Description
0	RW	0	PWMD	PWM output disable: 0: PWM output normal 1: no PWM output
1	RW	0	SID	Serial interface (I^2S out) disable: 0: I^2S output normal 1: no I^2S output
2	RW	0	COD	Clock output disable: 0: clock output normal 1: no clock output

Bit	RW	RST	Name	Description
3	RW	0	AME	AM mode enable: 0: normal FFX operation 1: AM reduction mode FFX operation

The STA321MP features an FFX processing mode that minimizes the amount of noise generated in the frequency range of AM radio. This mode is intended for use when FFX is operating in a device with an active AM tuner. The SNR of the FFX processing is reduced to ~83 dB in this mode, which is still greater than the SNR of the AM radio.

Bit	RW	RST	Name	Description
4	RW	0	AM2E	AM2 mode enable: 0: normal FFX operation 1: AM2 reduction mode FFX operation

The STA321MP features two FFX processing modes that minimize the amount of noise generated in the frequency range of the AM radio. This second mode is intended for use when FFX operates in a device with an active AM tuner. This mode eliminates the noise-shaper.

Bit	RW	RST	Name	Description
5	RW	0	HPE	FFX headphone enable: 0: channels 7 and 8 normal FFX operation 1: channels 7 and 8 headphone operation

Channels 7 and 8 can be configured to be processed and output in such a manner that headphones can be driven using an appropriate output device. This signal is a differential 3-wire drive called the FFX headphone.

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Bit	RW	RST	Name	Description
6	RW	0	DCCV	Distortion compensation variable enable: 0: uses preset DC coefficient 1: uses DCC coefficient

Bit	RW	RST	Name	Description
7	RW	0	MPCV	Max power correction variable: 0: use standard MPC coefficient 1: use MPCC bits for MPC coefficient

7.2.6 Configuration register H (0x07)

D7	D6	D5	D4	D3	D2	D1	D0
ECLE	LDTE	BCLE	IDE	ZDE	SVE	ZCE	NSBW
0	1	1	1	1	1	1	0

Bit	RW	RST	Name	Description
0	RW	0	NSBW	Noise-shaper bandwidth selection: 1: 3rd order NS 0: 4th order NS

Bit	RW	RST	Name	Description
1	RW	1	ZCE	Zero-crossing volume enable: 1: volume adjustments only occur at digital zero-crossings. 0: volume adjustments occur immediately

The ZCE bit enables zero-crossing volume adjustments. When volume is adjusted on digital zero-crossings, no clicks are audible.

Bit	RW	RST	Name	Description
2	RW	1	SVE	Soft volume enable: 1: volume adjustments use soft volume 0: volume adjustments occur immediately

Bit	RW	RST	Name	Description
3	RW	1	ZDE	Zero-detect mute enable: setting of 1 enables the automatic zero-detect mute

Setting the ZDE bit enables the zero-detect automatic mute. The zero-detect circuit looks at the input data of each processing channel after the channel-mapping block. If any channel receives 2048 consecutive zero value samples (regardless of fs), then that individual channel is muted if this function is enabled.

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Bit	RW	RST	Name	Description
4	RW	1	IDE	Invalid input detect mute enable: 1: enables the automatic invalid input detect mute

Setting the IDE bit enables this function, which looks at the input I^2S data and automatically mutes if the signals are perceived as invalid.

Bit	RW	RST	Name	Description
5	RW	1	BCLE	Binary output mode clock loss detection enable

The BCLE bit detects loss of input MCLK in binary mode and outputs 50 % duty cycle.

Bit	RW	RST	Name	Description
6	RW	1	LDTE	LRCLK double trigger protection enable

The LDTE bit actively prevents double triggering of LRCLK.

Bit	RW	RST	Name	Description
7	RW	1	ECLE	Auto EAPD on clock loss

The ECLE bit controls the device power down signal (EAPD) on clock loss detection. This function is enabled by default. It is strongly recommended to avoid spurious noise during the on-off sequence. The STA321MP has the ECLE bit set to 0.

7.2.7 Configuration register I (0x08)

D7	D6	D5	D4	D3	D2	D1	D0
EAPD							PSCE
0							0

This feature utilizes an ADC on SDI78 that provides power supply ripple information for correction. Registers PSC1, PSC2, and PSC3 are utilized in this mode.

Bit	RW	RST	Name	Description
0	RW	0	PSCE	Power supply ripple correction enable: 0: normal operation 1: PSCorrect operation

Bit	RW	RST	Name	Description
7	RW	0	EAPD	External amplifier power down: 0: external power stage power-down active 1: normal operation

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7.2.8 Master mute register (0x09)

D7	D6	D5	D4	D3	D2	D1	D0
							MMUTE
							0

7.2.9 Master volume register (0x0A)

D7	D6	D5	D4	D3	D2	D1	D0
MV7	MV6	MV5	MV4	MV3	MV2	MV1	MV0
1	1	1	1	1	1	1	1

Note: The value of the volume derived from MVOL is dependent on the AMV AutoMode volume settings.

7.2.10 Channel 1 volume (0x0B)

D7	D6	D5	D4	D3	D2	D1	D0
C1V7	C1V6	C1V5	C1V4	C1V3	C1V2	C1V1	C1V0
0	1	1	0	0	0	0	0

7.2.11 Channel 2 volume (0x0C)

D7	D6	D5	D4	D3	D2	D1	D0
C2V7	C2V6	C2V5	C2V4	C2V3	C2V2	C2V1	C2V0
0	1	1	0	0	0	0	0

7.2.12 Channel 3 volume (0x0D)

D7	D6	D5	D4	D3	D2	D1	D0
C3V7	C3V6	C3V5	C3V4	C3V3	C3V2	C3V1	C3V0
0	1	1	0	0	0	0	0

7.2.13 Channel 4 volume (0x0E)

D7	D6	D5	D4	D3	D2	D1	D0
C4V7	C4V6	C4V5	C4V4	C4V3	C4V2	C4V1	C4V0
0	1	1	0	0	0	0	0

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7.2.14 Channel 5 volume (0x0F)

D7	D6	D5	D4	D3	D2	D1	D0
C5V7	C5V6	C5V5	C5V4	C5V3	C5V2	C5V1	C5V0
0	1	1	0	0	0	0	0

7.2.15 Channel 6 volume (0x10)

D7	D6	D5	D4	D3	D2	D1	D0
C6V7	C6V6	C6V5	C6V4	C6V3	C6V2	C6V1	C6V0
0	1	1	0	0	0	0	0

7.2.16 Channel 7 volume (0x11)

D7	D6	D5	D4	D3	D2	D1	D0
C7V7	C7V6	C7V5	C7V4	C7V3	C7V2	C7V1	C7V0
0	1	1	0	0	0	0	0

7.2.17 Channel 8 volume (0x12)

D7	D6	D5	D4	D3	D2	D1	D0
C8V7	C8V6	C8V5	C8V4	C8V3	C8V2	C8V1	C8V0
0	1	1	0	0	0	0	0

7.2.18 Channel 1 volume trim, mute, bypass (0x13)

D7	D6	D5	D4	D3	D2	D1	D0
C1M	C1VBP		C1VT4	C1VT3	C1VT2	C1VT1	C1VT0
0	0	0	1	0	0	0	0

7.2.19 Channel 2 volume trim, mute, bypass (0x14)

D7	D6	D5	D4	D3	D2	D1	D0
C2M	C2VBP		C2VT4	C2VT3	C2VT2	C2VT1	C2VT0
0	0	0	1	0	0	0	0

7.2.20 Channel 3 volume trim, mute, bypass (0x15)

D7	D6	D5	D4	D3	D2	D1	D0
C3M	C3VBP		C3VT4	C3VT3	C3VT2	C3VT1	C3VT0
0	0	0	1	0	0	0	0

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7.2.21 Channel 4 volume trim, mute, bypass (0x16)

D7	D6	D5	D4	D3	D2	D1	D0
C4M	C4VBP		C4VT4	C4VT3	C4VT2	C4VT1	C4VT0
0	0	0	1	0	0	0	0

7.2.22 Channel 5 volume trim, mute, bypass (0x17)

D7	D6	D5	D4	D3	D2	D1	D0
C5M	C5VBP		C5VT4	C5VT3	C5VT2	C5VT1	C5VT0
0	0	0	1	0	0	0	0

7.2.23 Channel 6 volume trim, mute, bypass (0x18)

D7	D6	D5	D4	D3	D2	D1	D0
C6M	C6VBP		C6VT4	C6VT3	C6VT2	C6VT1	C6VT0
0	0	0	1	0	0	0	0

7.2.24 Channel 7 volume trim, mute, bypass (0x19)

D7	D6	D5	D4	D3	D2	D1	D0
C7M	C7VBP		C7VT4	C7VT3	C7VT2	C7VT1	C7VT0
0	0	0	1	0	0	0	0

7.2.25 Channel 8 volume trim, mute, bypass (0x1A)

D7	D6	D5	D4	D3	D2	D1	D0
C8M	C8VBP		C8VT4	C8VT3	C8VT2	C8VT1	C8VT0
0	0	0	1	0	0	0	0

The volume structure of the STA321MP consists of individual volume registers for each channel and a master volume register that provides an offset to each channel's volume setting. There is also an additional offset for each channel called the channel volume trim. The individual channel volumes are adjustable in 0.5 dB steps from 48 dB to -78 dB. As an example, if C5V = 0xXX or +XXX dB and MV = 0xXX or -XX dB, then the total gain for channel 5 = XX dB. The channel volume trim is adjustable independently on each channel from -10 dB to 10 dB in 1 dB steps. The master mute when set to 1 mutes all channels at once, whereas the individual channel mutes (CnM) mutes only that channel. Both the master mute and the channel mutes provide a "soft mute" with the volume ramping down to mute in 8192 samples from the maximum volume setting at the internal processing rate (~192 kHz). A "hard mute" can be obtained by commanding a value of 0xFF (255) to any channel volume register or the master volume register. When volume offsets are provided via the master volume register, any channel whose total volume is less than -91 dB is muted. All changes in volume take place at zero-crossings when ZCE = 1 (configuration register H) on a per-channel basis as this creates the smoothest possible volume

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transitions. When ZCE = 0, volume updates occur immediately. Each channel also contains an individual channel volume bypass. If a particular channel has volume bypassed via the CnVBP = 1 register, then only the channel volume setting for that particular channel affects the volume setting, the master volume setting does affect that channel. Each channel also contains a channel mute. If CnM = 1 a soft mute is performed on that channel.

MV[7:0]	Volume offset from channel value
0x00	0 dB
0x01	-0.5 dB
0x02	-1 dB
…	…
0x4C	-38 dB
…	…
0xFE	-127 dB
0xFF	Hardware channel mute

CnV[7:0]	Volume
0x00	48 dB
0x01	47.5 dB
0x02	47 dB
…	…
0x5F	0.5 dB
0x60	0 dB
0x61	-0.5 dB
…	…
0xFE	-79.5 dB
0xFF	Hardware channel mute

CnVT[4:0]	Volume
0x00 to 0x06	10 dB
0x07	9 dB
…	…
0x0F	1 dB
0x10	0 dB
0x11	-1 dB
…	…
0x19	-9 dB
0x1A to 0x1F	-10 dB

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7.2.26 Channel input mapping channels 1 and 2 (0x1B)

D7	D6	D5	D4	D3	D2	D1	D0
	C2IM2	C2IM1	C2IM0		C1IM2	C1IM1	C1IM0
	0	0	1		0	0	0

7.2.27 Channel input mapping channels 3 and 4 (0x1C)

D7	D6	D5	D4	D3	D2	D1	D0
	C4IM2	C4IM1	C4IM0		C3IM2	C3IM1	C3IM0
	0	1	1		0	1	0

7.2.28 Channel input mapping channels 5 and 6 (0x1D)

D7	D6	D5	D4	D3	D2	D1	D0
	C6IM2	C6IM1	C6IM0		C5IM2	C5IM1	C5IM0
	1	0	1		1	0	0

7.2.29 Channel input mapping channels 7 and 8 (0x1E)

D7	D6	D5	D4	D3	D2	D1	D0
	C8IM2	C8M1	C8IM0		C7IM2	C7IM1	C7IM0
	1	1	1		1	1	0

Each channel received via I^2S can be mapped to any internal processing channel via the channel input mapping registers. This allows for flexibility in processing, simplifies output stage designs, and enables the ability to perform crossovers. The default settings of these registers map each I^2S input channel to its corresponding processing channel.

CnIM[2:0]	Serial input from
000	Channel 1
001	Channel 2
010	Channel 3
011	Channel 4
100	Channel 5
101	Channel 6
110	Channel 7
111	Channel 8

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7.2.30 Biquad internal channel loop-through (0x28)

D7	D6	D5	D4	D3	D2	D1	D0
C8BLP	C7BLP	C6BLP	C5BLP	C4BLP	C3BLP	C2BLP	C1BLP
0	0	0	0	0	0	0	0

Each internal processing channel can receive two possible inputs at the input to the biquad block. The input can come either from the output of that channel's MIX#1 engine or from the output of the bass/treble (biquad #10) of the previous channel. In this scenario, channel 1 receives channel 8. This enables the use of more than 10 biquads on any given channel at the loss of the number of separate internal processing channels.

Bit	RW	RST	Name	Description
7:0	RW	0	CnBLP	For n = 1 to 8: 0: input from channel n MIX#1 engine output - normal operation. 1: input from channel (n - 1) biquad #10 output - loop operation.

7.2.31 Mix internal channel loop-through (0x29)

D7	D6	D5	D4	D3	D2	D1	D0
C8MXLP	C7MXLP	C6MXLP	C5MXLP	C4MXLP	C3MXLP	C2MXLP	C1MXLP
0	0	0	0	0	0	0	0

Each internal processing channel can receive two possible sets of inputs at the inputs to the Mix#1 block. The inputs can come from the outputs of the interpolation block as normally occurs (CnMXLP = 0) or they can come from the outputs of the Mix#2 block. This enables the use of additional filtering after the second mix block at the expense of losing this processing capability on the channel.

Bit	RW	RST	Name	Description
7:0	RW	0	CnMXLP	For n = 1 to 8: 0: inputs to channel n MIX#1 engine from interpolation outputs - normal operation. 1: inputs to channel n MIX#1 engine from MIX#2 engine outputs - loop operation.

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7.2.32 EQ bypass (0x2A)

D7	D6	D5	D4	D3	D2	D1	D0
C8EQBP	C7EQBP	C6EQBP	C5EQBP	C4EQCBP	C3EQBP	C2EQBP	C1EQBP
0	0	0	0	0	0	0	0

EQ control can be bypassed on a per-channel basis. If EQ control is bypassed on a given channel the prescale and all 10 filters (high-pass, biquads, de-emphasis, bass management cross-over, bass, treble in any combination) are bypassed for that channel.

Bit	RW	RST	Name	Description
7:0	RW	0	CnEQBP	For n = 1 to 8: 0: perform EQ on channel n - normal operation 1: bypass EQ on channel n

7.2.33 Tone control bypass (0x2B)

D7	D6	D5	D4	D3	D2	D1	D0
C8TCB	C7TCB	C6TCB	C5TCB	C4TCB	C3TCB	C2TCB	C1TCB
0	0	0	0	0	0	0	0

Tone control (bass/treble) can be bypassed on a per-channel basis. If tone control is bypassed on a given channel the two filters that tone control utilizes are made available as user programmable biquads #9 and #10.

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7.2.34 Tone control (0x2C)

D7	D6	D5	D4	D3	D2	D1	D0
TTC3	TTC2	TTC1	TTC0	BTC3	BTC2	BTC1	BTC0
0	1	1	1	0	1	1	1

This is the tone control boost/cut as a function of the BTC and TTC bits.

BTC[3:0]/TTC[3:0)	Boost/cut
0000	-12 dB
0001	-12 dB
…	…
0111	-4 dB
0110	-2 dB
0111	0 dB
1000	2 dB
1001	4 dB
…	…
1101	12 dB
1110	12 dB
1111	12dB

7.2.35 Channel 1 and 2 output timing (0x33)

D7	D6	D5	D4	D3	D2	D1	D0
	C2OT2	C2OT1	C2OT0		C1OT2	C1OT1	C1OT0
	1	0	0		0	0	0

7.2.36 Channel 3 and 4 output timing (0x34)

D7	D6	D5	D4	D3	D2	D1	D0
	C4OT2	C4OT1	C4OT0		C3OT2	C3OT1	C3OT0
	1	1	0		0	1	0

7.2.37 Channel 5 and 6 output timing (0x35)

D7	D6	D5	D4	D3	D2	D1	D0
	C6OT2	C6OT1	C6OT0		C5OT2	C5OT1	C5OT0
	1	0	1		0	0	1

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7.2.38 Channel 7 and 8 output timing (0x36)

D7	D6	D5	D4	D3	D2	D1	D0
	C8OT2	C8OT1	C8OT0		C7OT2	C7OT1	C7OT0
	1	1	1		0	1	1

The centering of the individual channel PWM output periods can be adjusted by the output timing registers. PWM slot settings can be chosen to ensure that pulse transitions do not occur at the same time on different channels using the same power device. There are 8 possible settings, the appropriate setting varies based on the application and connections to the FFX power devices.

CnOT[2:0]	PWM slot
000	1
001	2
010	3
011	4
100	5
101	6
110	7
111	8

7.2.39 Channel I^2S output mapping channels 1 and 2 (0x37)

D7	D6	D5	D4	D3	D2	D1	D0
	C2OM2	C2OM1	C2OM0		C1OM2	C1OM1	C1OM0
	0	0	1		0	0	0

7.2.40 Channel I^2S output mapping channels 3 and 4 (0x38)

D7	D6	D5	D4	D3	D2	D1	D0
	C4OM2	C4OM1	C4OM0		C3OM2	C3OM1	C3OM0
	0	1	1		0	1	0

7.2.41 Channel I^2S output mapping channels 5 and 6 (0x39)

D7	D6	D5	D4	D3	D2	D1	D0
	C6OM2	C6OM1	C6OM0		C5OM2	C5OM1	C5OM0
	1	0	1		1	0	0

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7.2.42 Channel I²S output mapping channels 7 and 8 (0x3A)

D7	D6	D5	D4	D3	D2	D1	D0
	C8OM2	C8M1	C8OM0		C7OM2	C7OM1	C7OM0
	1	1	1		1	1	0

Each I²S output channel can receive data from any channel output of the volume block. Which channel a particular I²S output receives is dependent upon that channel's CnOM register bits.

CnOM[2:0]	Serial output from
000	Channel 1
001	Channel 2
010	Channel 3
011	Channel 4
100	Channel 5
101	Channel 6
110	Channel 7
111	Channel 8

7.2.43 Coefficient address register 1 (0x3B)

D7	D6	D5	D4	D3	D2	D1	D0
						CFA9	CFA8
						0	0

7.2.44 Coefficient address register 2 (0x3C)

D7	D6	D5	D4	D3	D2	D1	D0
CFA7	CFA6	CFA5	CFA4	CFA3	CFA2	CFA1	CFA0
0	0	0	0	0	0	0	0

7.2.45 Coefficient b1 data register, bits 23:16 (0x3D)

D7	D6	D5	D4	D3	D2	D1	D0
C1B23	C1B22	C1B21	C1B20	C1B19	C1B18	C1B17	C1B16
0	0	0	0	0	0	0	0

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7.2.46 Coefficient b1 data register, bits 15:8 (0x3E)

D7	D6	D5	D4	D3	D2	D1	D0
C1B15	C1B14	C1B13	C1B12	C1B11	C1B10	C1B9	C1B8
0	0	0	0	0	0	0	0

7.2.47 Coefficient b1 data register, bits 7:0 (0x3F)

D7	D6	D5	D4	D3	D2	D1	D0
C1B7	C1B6	C1B5	C1B4	C1B3	C1B2	C1B1	C1B0
0	0	0	0	0	0	0	0

7.2.48 Coefficient b2 data register, bits 23:16 (0x40)

D7	D6	D5	D4	D3	D2	D1	D0
C2B23	C2B22	C2B21	C2B20	C2B19	C2B18	C2B17	C2B16
0	0	0	0	0	0	0	0

7.2.49 Coefficient b2 data register, bits 15:8 (0x41)

D7	D6	D5	D4	D3	D2	D1	D0
C2B15	C2B14	C2B13	C2B12	C2B11	C2B10	C2B9	C2B8
0	0	0	0	0	0	0	0

7.2.50 Coefficient b2 data register, bits 7:0 (0x42)

D7	D6	D5	D4	D3	D2	D1	D0
C2B7	C2B6	C2B5	C2B4	C2B3	C2B2	C2B1	C2B0
0	0	0	0	0	0	0	0

7.2.51 Coefficient a1 data register, bits 23:16 (0x43)

D7	D6	D5	D4	D3	D2	D1	D0
C1B23	C1B22	C1B21	C1B20	C1B19	C1B18	C1B17	C1B16
0	0	0	0	0	0	0	0

7.2.52 Coefficient a1 data register, bits 15:8 (0x44)

D7	D6	D5	D4	D3	D2	D1	D0
C3B15	C3B14	C3B13	C3B12	C3B11	C3B10	C3B9	C3B8
0	0	0	0	0	0	0	0

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7.2.53 Coefficient a1 data register, bits 7:0 (0x45)

D7	D6	D5	D4	D3	D2	D1	D0
C3B7	C3B6	C3B5	C3B4	C3B3	C3B2	C3B1	C3B0
0	0	0	0	0	0	0	0

7.2.54 Coefficient a2 data register, bits 23:16 (0x46)

D7	D6	D5	D4	D3	D2	D1	D0
C4B23	C4B22	C4B21	C4B20	C4B19	C4B18	C4B17	C4B16
0	0	0	0	0	0	0	0

7.2.55 Coefficient a2 data register, bits 15:8 (0x47)

D7	D6	D5	D4	D3	D2	D1	D0
C4B15	C4B14	C4B13	C4B12	C4B11	C4B10	C4B9	C4B8
0	0	0	0	0	0	0	0

7.2.56 Coefficient a2 data register, bits 7:0 (0x48)

D7	D6	D5	D4	D3	D2	D1	D0
C4B7	C4B6	C4B5	C4B4	C4B3	C4B2	C4B1	C4B0
0	0	0	0	0	0	0	0

7.2.57 Coefficient b0 data register, bits 23:16 (0x49)

D7	D6	D5	D4	D3	D2	D1	D0
C5B23	C5B22	C5B21	C5B20	C5B19	C5B18	C5B17	C5B16
0	0	0	0	0	0	0	0

7.2.58 Coefficient b0 data register, bits 15:8 (0x4A)

D7	D6	D5	D4	D3	D2	D1	D0
C5B15	C5B14	C5B13	C5B12	C5B11	C5B10	C5B9	C5B8
0	0	0	0	0	0	0	0

7.2.59 Coefficient b0 data register, bits 7:0 (0x4B)

D7	D6	D5	D4	D3	D2	D1	D0
C5B7	C5B6	C5B5	C5B4	C5B3	C5B2	C5B1	C5B0
0	0	0	0	0	0	0	0

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7.2.60 Coefficient write control register (0x4C)

D7	D6	D5	D4	D3	D2	D1	D0
						WA	W1
						0	0

Coefficients for EQ and Bass Management are handled internally in the STA321MP via RAM. Access to this RAM is available to the user via an I^2C register interface.

A collection of I^2C registers are dedicated to this function. One register contains a coefficient base address, five sets of three registers store the values of the 24-bit coefficients to be written or that were read, and one register contains bits used to control the write of the coefficient(s) to RAM. *Section 7.3*, *Section 7.4*, *Section 7.5*, and *Section 7.6* give the instructions for reading and writing coefficients.

7.3 Reading a coefficient from RAM

1. Write the top 2 bits of the address to I^2C register 0x3B
2. Write the bottom 8 bits of the address to I^2C register 0x3C
3. Read the top 8 bits of the coefficient from I^2C address 0x3D
4. Read the middle 8 bits of the coefficient from I^2C address 0x3E
5. Read the bottom 8 bits of the coefficient from I^2C address 0x3F

7.4 Reading a set of coefficients from RAM

1. Write the top 2 bits of the address to I^2C register 0x3B
2. Write the bottom 8 bits of the address to I^2C register 0x3C
3. Read the top 8 bits of the coefficient from I^2C address 0x3D
4. Read the middle 8 bits of the coefficient from I^2C address 0x3E
5. Read the bottom 8 bits of the coefficient from I^2C address 0x3F
6. Read the top 8 bits of coefficient b2 from I^2C address 0x40
7. Read the middle 8 bits of coefficient b2 from I^2C address 0x41
8. Read the bottom 8 bits of coefficient b2 from I^2C address 0x42
9. Read the top 8 bits of coefficient a1 from I^2C address 0x43
10. Read the middle 8 bits of coefficient a1 from I^2C address 0x44
11. Read the bottom 8 bits of coefficient a1 from I^2C address 0x45
12. Read the top 8 bits of coefficient a2 from I^2C address 0x46
13. Read the middle 8 bits of coefficient a2 from I^2C address 0x47
14. Read the bottom 8 bits of coefficient a2 from I^2C address 0x48
15. Read the top 8 bits of coefficient b0 from I^2C address 0x49
16. Read the middle 8 bits of coefficient b0 from I^2C address 0x4A
17. Read the bottom 8 bits of coefficient b0 from I^2C address 0x4B

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7.5 Writing a single coefficient to RAM

1. Write the top 2 bits of the address to I^2C register 0x3B
2. Write the bottom 8 bits of the address to I^2C register 0x3C
3. Write the top 8 bits of the coefficient in I^2C address 0x3D
4. Write the middle 8 bits of the coefficient in I^2C address 0x3E
5. Write the bottom 8 bits of the coefficient in I^2C address 0x3F
6. Write 1 to the W1 bit in I^2C address 0x4C

7.6 Writing a set of coefficients to RAM

1. Write the top 2 bits of the starting address to I^2C register 0x3B
2. Write the bottom 8 bits of the starting address to I^2C register 0x3C
3. Write the top 8 bits of coefficient b1 in I^2C address 0x3D
4. Write the middle 8 bits of coefficient b1 in I^2C address 0x3E
5. Write the bottom 8 bits of coefficient b1 in I^2C address 0x3F
6. Write the top 8 bits of coefficient b2 in I^2C address 0x40
7. Write the middle 8 bits of coefficient b2 in I^2C address 0x41
8. Write the bottom 8 bits of coefficient b2 in I^2C address 0x42
9. Write the top 8 bits of coefficient a1 in I^2C address 0x43
10. Write the middle 8 bits of coefficient a1 in I^2C address 0x44
11. Write the bottom 8 bits of coefficient a1 in I^2C address 0x45
12. Write the top 8 bits of coefficient a2 in I^2C address 0x46
13. Write the middle 8 bits of coefficient a2 in I^2C address 0x47
14. Write the bottom 8 bits of coefficient a2 in I^2C address 0x48
15. Write the top 8 bits of coefficient b0 in I^2C address 0x49
16. Write the middle 8 bits of coefficient b0 in I^2C address 0x4A
17. Write the bottom 8 bits of coefficient b0 in I^2C address 0x4B
18. Write 1 to the WA bit in I^2C address 0x4C

The mechanism for writing a set of coefficients to the RAM provides a method of updating the five coefficients corresponding to a given biquad (filter) simultaneously to avoiding possible unpleasant acoustic side-effects.

When using this technique, the 10-bit address specifies the address of the biquad b1 coefficient (for example, decimals 0, 5, 10, 15, …, 100, … 395), and the STA321MP generates the RAM addresses as offsets from this base value to write the complete set of coefficient data.

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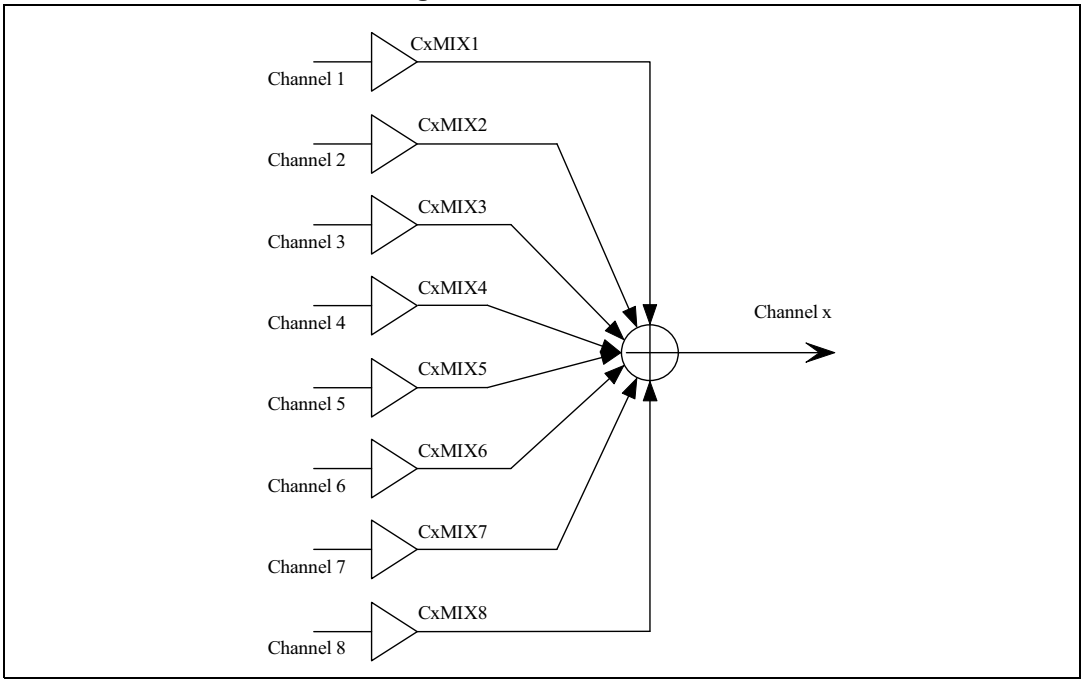
8 Equalization and mixing

Figure 8. Channel mixer



8.1 Post-scale

The STA321MP provides one additional multiplication after the last interpolation stage and before the distortion compensation on each channel. This is a 24-bit signed fractional multiplication.

The scale factor for this multiplication is loaded into the RAM using the same I^2C registers as the biquad coefficients and the bass-management.

This post-scale factor can be used in conjunction with an ADC-equipped microcontroller to perform power-supply error correction. All channels can use channel 1 by setting the post-scale link bit.

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Table 9. RAM block for biquads, mixing, and bass management

Index (decimal)	Index (hex)		Coefficient	Default
0	0x00	Channel 1 - Biquad 1	C1H10 (b1/2)	0x000000
1	0x01		C1H11 (b2)	0x000000
2	0x02		C1H12 (a1/2)	0x000000
3	0x03		C1H13 (a2)	0x000000
4	0x04		C1H14 (b0/2)	0x400000
5	0x05	Channel 1 - Biquad 2	C1H20	0x000000
…	…	…	…	…
49	0x31	Channel 1 - Biquad 10	C1HA4	0x400000
50	0x32	Channel 2 - Biquad 1	C2H10	0x000000
51	0x33		C2H11	0x000000
…	…	…	…	…
99	0x63	Channel 2 - Biquad 10	C2HA4	0x4000000
100	0x64	Channel 3 - Biquad 1	C3H10	0x000000
…	…	…	…	…
399	0x18F	Channel 8 - Biquad 10	C8HA4	0x400000
400	0x190	Channel 1 - Pre-Scale	C1PreS	0x7FFFFF
401	0x191	Channel 2 - Pre-Scale	C2PreS	0x7FFFFF
402	0x192	Channel 3 - Pre-Scale	C3PreS	0x7FFFFF
…	…	…	…	…
407	0x197	Channel 8 - Pre-Scale	C8PreS	0x7FFFFF
408	0x198	Channel 1 - Post-Scale	C1PstS	0x7FFFFF
409	0x199	Channel 2 - Post-Scale	C2PstS	0x7FFFFF
…	…	…	…	…
415	0x19F	Channel 8 - Post-Scale	C8PstS	0x7FFFFF
416	0x1A0	Channel 1 - Mix#1 1	C1MX11	0x7FFFFF
417	0x1A1	Channel 1 - Mix#1 2	C1MX12	0x000000
…	…	…	…	…
423	0x1A7	Channel 1 - Mix#1 8	C1MX18	0x000000
424	0x1A8	Channel 2 - Mix#1 1	C2MX11	0x000000
425	0x1A9	Channel 2 - Mix#1 2	C2MX12	0x7FFFFF
…	…	…	…	…
463	0x1CF	Channel 8 - Mix#1 8	C8MX18	0x7FFFFF
464	0x1D0	Channel 1 - Mix#2 1	C1MX21	0x7FFFFF
465	0x1D1	Channel 1 - Mix#2 2	C1MX22	0x000000

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Table 9. RAM block for biquads, mixing, and bass management (continued)

Index (decimal)	Index (hex)		Coefficient	Default
…	…	…	…	…
471	0x1D7	Channel 1 - Mix#2 8	C1MX28	0x000000
472	0x1D8	Channel 2 - Mix#2 1	C2MX21	0x000000
473	0x1D9	Channel 2 - Mix#2 2	C2MX22	0x7FFFFF
…	…	…	…	…
527	0x20F	Channel 8 - Mix#2 8	C8MX28	0x7FFFFF

8.2 Variable max power correction

8.2.1 MPCC1-2 (0x4D, 0x4E)

The MPCC bits determine the 16 MSBs of the MPC compensation coefficient. This coefficient is used in place of the default coefficient when MPCV = 1.

D7	D6	D5	D4	D3	D2	D1	D0
MPCC15	MPCC14	MPCC13	MPCC12	MPCC11	MPCC10	MPCC9	MPCC8
0	0	1	0	1	1	0	1

D7	D6	D5	D4	D3	D2	D1	D0
MPCC7	MPCC6	MPCC5	MPCC4	MPCC3	MPCC2	MPCC1	MPCC0
1	1	0	0	0	0	0	0

8.3 Variable distortion compensation

8.3.1 DCC1-2 (0x4F, 0x50)

The DCC bits determine the 16 MSBs of the distortion compensation coefficient. This coefficient is used in place of the default coefficient when DCCV = 1.

D7	D6	D5	D4	D3	D2	D1	D0
DCC15	DCC14	DCC13	DCC12	DCC11	DCC10	DCC9	DCC8
1	1	1	1	0	0	1	1

D7	D6	D5	D4	D3	D2	D1	D0
DCC7	DCC6	DCC5	DCC4	DCC3	DCC2	DCC1	DCC0
0	0	1	1	0	0	1	1

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8.4 Reserved registers

- Address: (0x01)
- Address: (0x03)
- Address: (0x51, 0x52)
- Address: (0x53)

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9 Package information

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9.1 TQFP64 (10 mm x 10 mm x 1.4 mm) package information

Figure 9. TQFP64 (10 mm x 10 mm x 1.4 mm) package outline

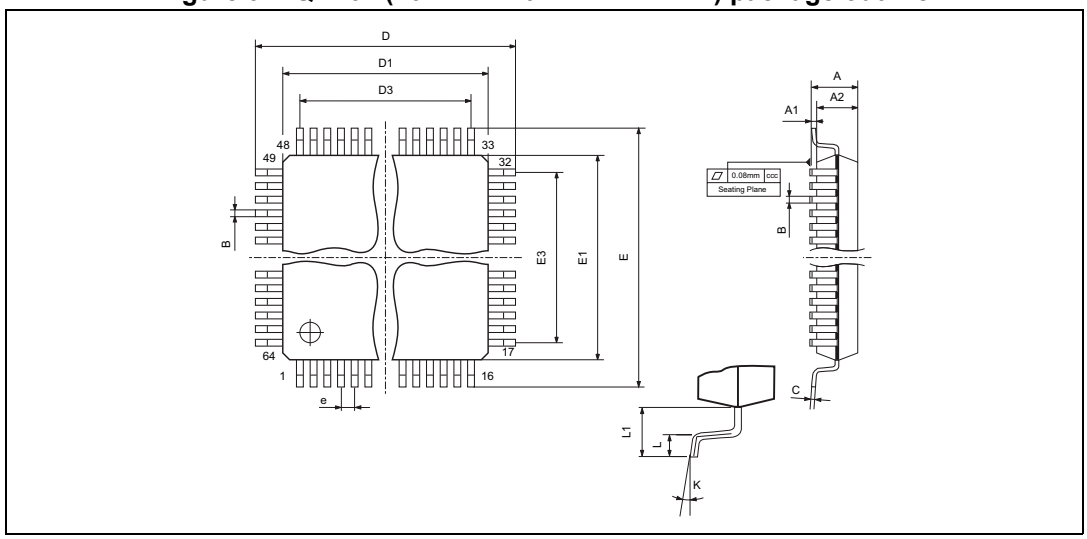

Table 10. TQFP64 (10 mm x 10 mm x 1.4 mm) mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.17	0.22	0.27	0.0066	0.0086	0.0106
C	0.09			0.0035		
D	11.80	12.00	12.20	0.464	0.472	0.480
D1	9.80	10.00	10.20	0.386	0.394	0.401
D3		7.50			0.295	
e		0.50			0.0197	
E	11.80	12.00	12.20	0.464	0.472	0.480
E1	9.80	10.00	10.20	0.386	0.394	0.401
E3		7.50			0.295	
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1		1.00			0.0393	
K	0 ° min, 3.5 ° typ, 7 ° max					
ccc			0.080			0.0031

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10 Revision history

Table 11. Document revision history

Date	Revision	Changes
07-Feb-2012	1	Initial release
20-Dec-2012	2	Updated pins 17, 21, and 22 in Figure 3: Pin connections (top view) and Table 2: Pin description STA321MPL (TQFP64)
05-Mar-2013	3	Updated Description Updated Table 1: Device summary Updated Section 2: Pin connections, Table 2, *3* Updated Table 4, 5, 6, 7 Removed section “Pin description” Added Section 3: Microphone interface, Figure 5, 6, and Table 9 Added Section 4.4: Read operation Removed “Application reference schematics” section Updated Section 5: Registers, Section 5.1, Table 10: Register summary, Section 5.2, added Figure 9 Added Section 5.2.3: Configuration register D (0x03) Added Section 5.2.27: Fine volume (FineVol) (0x5B) Added Section 5.2.32 through Section 5.2.36 Added Section 5.2.42 through Section 5.2.48 Renamed Section 6 and added Section 6.4 and 6.5 Added Section 7: Startup/shutdown pop noise removal
02-May-2013	4	Textual update in Section 3.6: Normal channel attenuation and Interpolation ratio select
03-Sep-2013	5	Added sentence “If XTI input is not used, related pin must be tied to GND” Chapter 5.2.1: Configuration register A (0x00) on page 27.
28-Jun-2016	6	Updated document layout Removed VFQFPN56 package Reworked technical content

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