# KAI-29050

# 6576 (H) x 4384 (V) Interline CCD Image Sensor

## Description

The KAI−29050 Image Sensor is a 29 Megapixel CCD in a 35 mm optical format. Based on the TRUESENSE 5.5 micron Interline Transfer CCD Platform, the sensor features broad dynamic range, excellent imaging performance, and a flexible readout architecture that enables use of 1, 2, or 4 outputs for full resolution readout up to 4 frames per second. A vertical overflow drain structure suppresses image blooming and enables electronic shuttering for precise exposure control.

The sensor is available with the TRUESENSE Sparse Color Filter Pattern, which provides a 2x improvement in light sensitivity compared to a standard color Bayer part.

The sensor shares common PGA pin−out and electrical configurations with other devices based on the TRUESENSE 5.5 micron Interline Transfer CCD Platform, allowing a single camera design to be leveraged to support multiple members of this sensor family.

**Table 1. GENERAL SPECIFICATIONS**

| Parameter | Typical Value |
|---|---|
| Architecture | Interline CCD; Progressive Scan |
| Total Number of Pixels | 6644 (H) x 4452 (V) |
| Number of Effective Pixels | 6600 (H) x 4408 (V) |
| Number of Active Pixels | 6576 (H) x 4384 (V) |
| Pixel Size | 5.5 μm (H) x 5.5 μm (V) |
| Active Image Size | 36.17 mm (H) x 24.11 mm (V)<br>43.47 mm (diag.), 35 mm Optical Format |
| Aspect Ratio | 3:2 |
| Number of Outputs | 1, 2, or 4 |
| Charge Capacity | 20,000 electrons |
| Output Sensitivity | 34 μV/e$^{-}$ |
| Quantum Efficiency<br>Pan (−AXA, −QXA, −PXA)<br>R, G, B (−FXA, −QXA)<br>R, G, B (−CXA, −PXA) | <br>43%<br>28%, 35%, 38%<br>29%, 35%, 37% |
| Read Noise (f = 40 MHz) | 12 electrons rms |
| Dark Current<br>Photodiode<br>VCCD | <br>7 electrons/s<br>140 electrons/s |
| Dark Current Doubling Temp.<br>Photodiode<br>VCCD | <br>7°C<br>9°C |
| Dynamic Range | 64 dB |
| Charge Transfer Efficiency | 0.999999 |
| Blooming Suppression | > 300 X |
| Smear | Estimated −100 dB |
| Image Lag | < 10 electrons |
| Maximum Pixel Clock Speed | 40 MHz |
| Maximum Frame Rates<br>Quad Output<br>Dual Output<br>Single Output | <br>4 fps<br>2 fps<br>1 fps |
| Package | 72 pin PGA |
| Cover Glass | AR coated, 2 Sides |

NOTE: All parameters are specified at T = 40°C unless otherwise noted.

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**Figure 1. KAI−29050 CCD Image Sensor**

## Features

- Bayer Color Pattern, TRUESENSE Sparse Color Filter Pattern, and Monochrome Configurations
- Progressive Scan Readout
- Flexible Readout Architecture
- High Frame Rate
- High Sensitivity
- Low Noise Architecture
- Excellent Smear Performance
- Package Pin Reserved for Device Identification

## Applications

- Industrial Imaging and Inspection
- Medical Imaging
- Security

## ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.



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## ORDERING INFORMATION

**Table 2. ORDERING INFORMATION**

| Part Number | Description | Marking Code |
|---|---|---|
| KAI−29050−AXA−JD−B1 | Monochrome, Special Microlens, PGA Package, Sealed Clear Cover Glass with AR coating (both sides), Grade 1 | KAI−29050−AXA Serial Number |
| KAI−29050−AXA−JD−B2 | Monochrome, Special Microlens, PGA Package, Sealed Clear Cover Glass with AR coating (both sides), Grade 2 | |
| KAI−29050−AXA−JD−AE | Monochrome, Special Microlens, PGA Package, Sealed Clear Cover Glass with AR coating (both sides), Engineering Grade | |
| KAI−29050−AXA−JR−B1 | Monochrome, Special Microlens, PGA Package, Taped Clear Cover Glass with AR coating (both sides), Grade 1 | |
| KAI−29050−AXA−JR−B2 | Monochrome, Special Microlens, PGA Package, Taped Clear Cover Glass with AR coating (both sides), Grade 2 | |
| KAI−29050−AXA−JR−AE | Monochrome, Special Microlens, PGA Package, Taped Clear Cover Glass with AR coating (both sides), Engineering Grade | |
| KAI−29050−FXA−JD−B1 | Gen2 Color (Bayer RGB), Special Microlens, PGA Package, Sealed Clear Cover Glass with AR coating (both sides), Grade 1 | KAI−29050−FXA Serial Number |
| KAI−29050−FXA−JD−B2 | Gen2 Color (Bayer RGB), Special Microlens, PGA Package, Sealed Clear Cover Glass with AR coating (both sides), Grade 2 | |
| KAI−29050−FXA−JD−AE | Gen2 Color (Bayer RGB), Special Microlens, PGA Package, Sealed Clear Cover Glass with AR coating (both sides), Engineering Grade | |
| KAI−29050−QXA−JD−B1 | Gen2 Color (TRUESENSE Sparse CFA), Special Microlens, PGA Package, Sealed Clear Cover Glass with AR coating (both sides), Grade 1 | KAI−29050−QXA Serial Number |
| KAI−29050−QXA−JD−B2 | Gen2 Color (TRUESENSE Sparse CFA), Special Microlens, PGA Package, Sealed Clear Cover Glass with AR coating (both sides), Grade 2 | |
| KAI−29050−QXA−JD−AE | Gen2 Color (TRUESENSE Sparse CFA), Special Microlens, PGA Package, Sealed Clear Cover Glass with AR coating (both sides), Engineering Grade | |

**Table 3. EVALUATION SUPPORT**

| Catalog Number | Product Name | Description |
|---|---|---|
| 4H2207 | KEM−4H2207−G2 FPGA Board−14−40 | FPGA Board for IT−CCD Evaluation Hardware |
| 4H2209 | KEH−4H2209−KAI−72 Pin Imager Board | 72 Pin Imager Board for IT−CCD Evaluation Hardware |
| 4H2211 | KEL−4H2211−Lens Mount Kit | Lens Mount Kit for IT−CCD Evaluation Hardware |

See the ON Semiconductor *Device Nomenclature* document (TND310/D) for a full description of the naming convention used for image sensors. For reference documentation, including information on evaluation kits, please visit our web site at www.onsemi.com.

**Table 4. NOT RECOMMENDED FOR NEW DESIGNS**

| Part Number | Description | Marking Code |
|---|---|---|
| KAI−29050−CXA−JD−B1 | Gen1 Color (Bayer RGB), Special Microlens, PGA Package, Sealed Clear Cover Glass with AR coating (both sides), Grade 1 | KAI−29050−CXA<br>Serial Number |
| KAI−29050−CXA−JD−B2 | Gen1 Color (Bayer RGB), Special Microlens, PGA Package, Sealed Clear Cover Glass with AR coating (both sides), Grade 2 | |
| KAI−29050−CXA−JD−AE | Gen1 Color (Bayer RGB), Special Microlens, PGA Package, Sealed Clear Cover Glass with AR coating (both sides), Engineering Grade | |
| KAI−29050−PXA−JD−B1 | Gen1 Color (TRUESENSE Sparse CFA), Special Microlens, PGA Package, Sealed Clear Cover Glass with AR coating (both sides), Grade 1 | KAI−29050−PXA<br>Serial Number |
| KAI−29050−PXA−JD−B2 | Gen1 Color (TRUESENSE Sparse CFA), Special Microlens, PGA Package, Sealed Clear Cover Glass with AR coating (both sides), Grade 2 | |
| KAI−29050−PXA−JD−AE | Gen1 Color (TRUESENSE Sparse CFA), Special Microlens, PGA Package, Sealed Clear Cover Glass with AR coating (both sides), Engineering Grade | |

## DEVICE DESCRIPTION

### Architecture

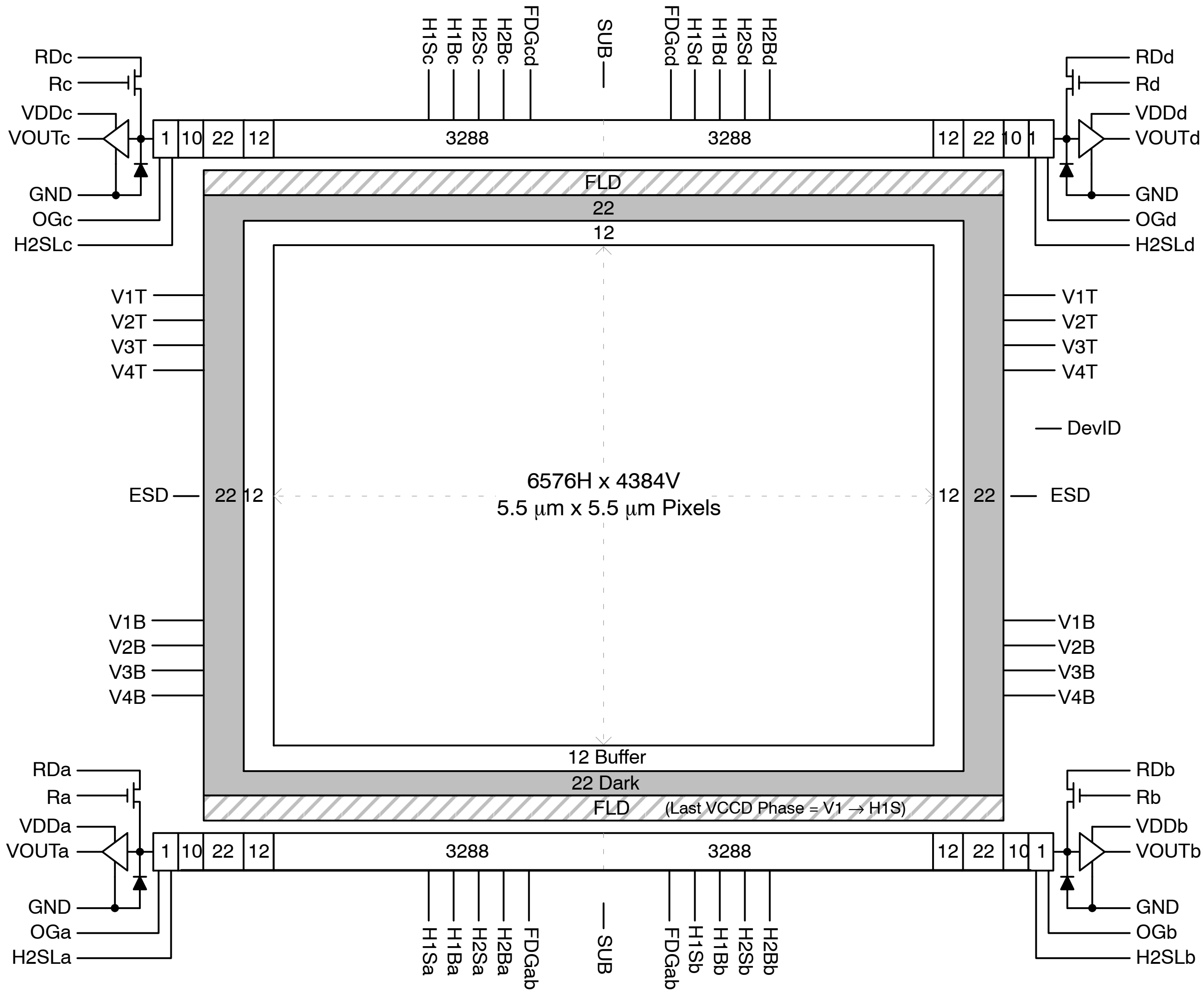



**Figure 2. Block Diagram**

### Dark Reference Pixels

There are 22 dark reference rows at the top and 22 dark rows at the bottom of the image sensor. The dark rows are not entirely dark and so should not be used for a dark reference level. Use the 22 dark columns on the left or right side of the image sensor as a dark reference.

Under normal circumstances use only the center 20 columns of the 22 column dark reference due to potential light leakage.

### Dummy Pixels

Within each horizontal shift register there are 11 leading additional shift phases. These pixels are designated as dummy pixels and should not be used to determine a dark reference level.

In addition, there is one dummy row of pixels at the top and bottom of the image.

### Active Buffer Pixels

12 unshielded pixels adjacent to any leading or trailing dark reference regions are classified as active buffer pixels. These pixels are light sensitive but are not tested for defects and non−uniformities.

### Image Acquisition

An electronic representation of an image is formed when incident photons falling on the sensor plane create electron−hole pairs within the individual silicon photodiodes. These photoelectrons are collected locally by the formation of potential wells at each photosite. Below photodiode saturation, the number of photoelectrons collected at each pixel is linearly dependent upon light level and exposure time and non−linearly dependent on wavelength. When the photodiodes charge capacity is reached, excess electrons are discharged into the substrate to prevent blooming.

### ESD Protection

Adherence to the power−up and power−down sequence is critical. Failure to follow the proper power−up and power−down sequences may cause damage to the sensor. See Power−Up and Power−Down Sequence section.

### Bayer Color Filter Pattern

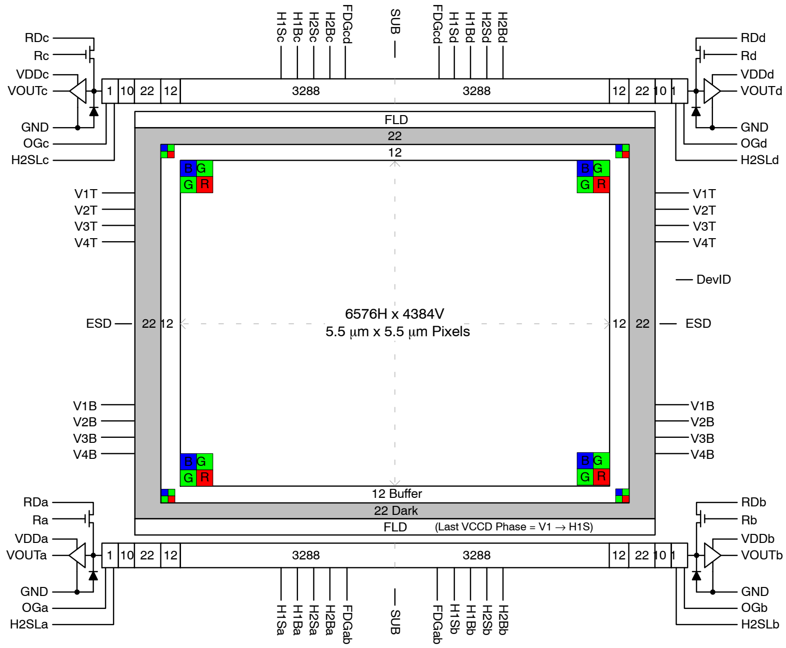



**Figure 3. Bayer Color Filter Pattern**

### TRUESENSE Sparse Color Filter Pattern

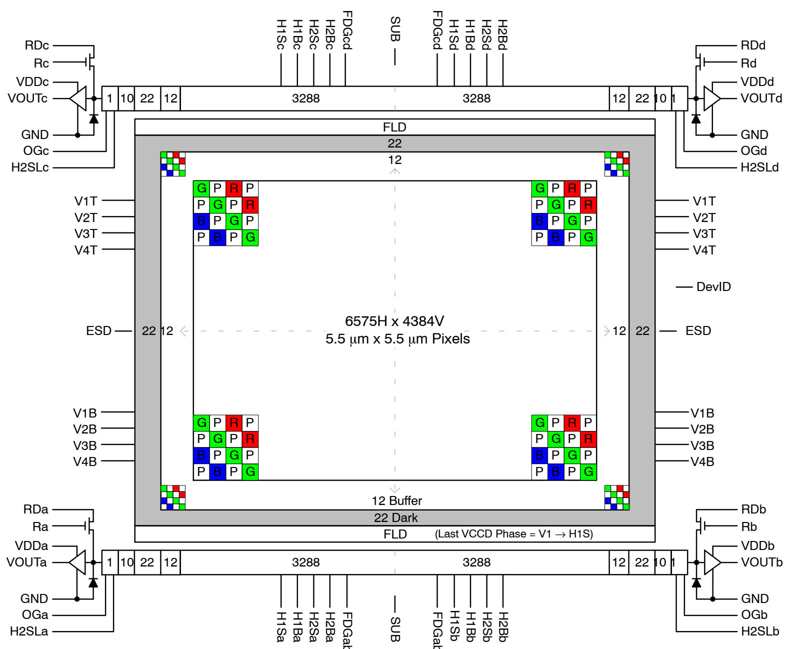



**Figure 4. TRUESENSE Sparse Color Filter Pattern**

## PHYSICAL DESCRIPTION

### Pin Description and Device Orientation

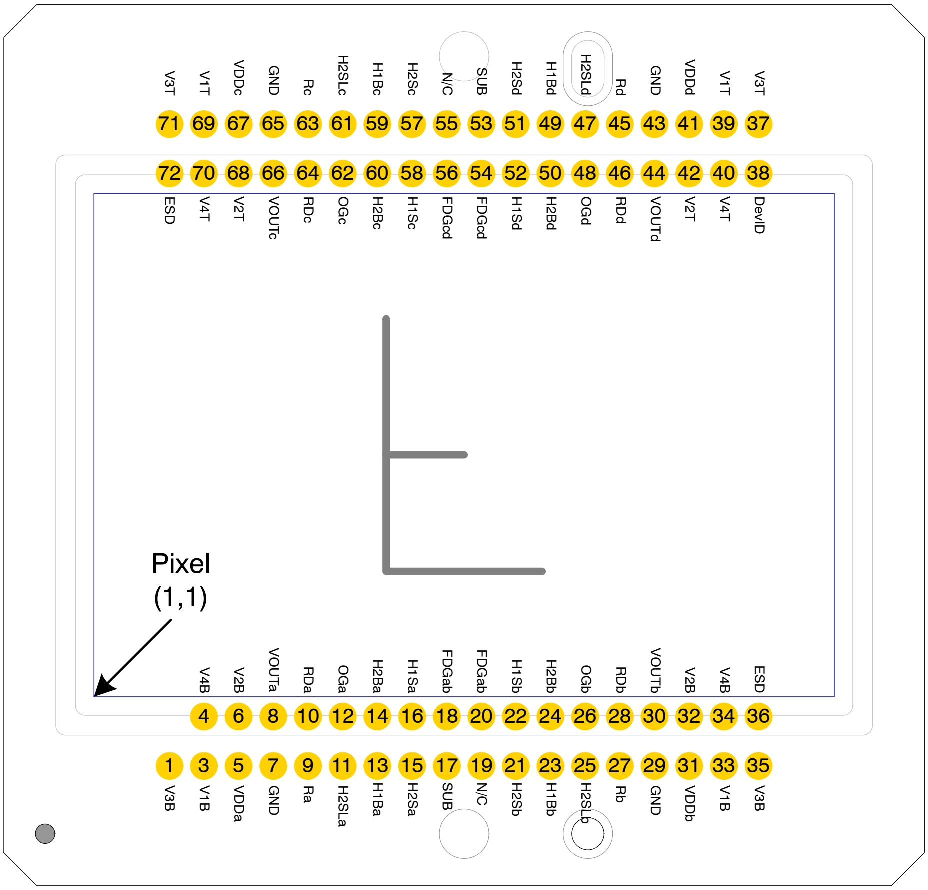



**Figure 5. Package Pin Designations − Top View**

**Table 5. PIN DESCRIPTION**

| Pin | Name | Description |
|---|---|---|
| 1 | V3B | Vertical CCD Clock, Phase 3, Bottom |
| | | |
| 3 | V1B | Vertical CCD Clock, Phase 1, Bottom |
| 4 | V4B | Vertical CCD Clock, Phase 4, Bottom |
| 5 | VDDa | Output Amplifier Supply, Quadrant a |
| 6 | V2B | Vertical CCD Clock, Phase 2, Bottom |
| 7 | GND | Ground |
| 8 | VOUTa | Video Output, Quadrant a |
| 9 | Ra | Reset Gate, Quadrant a |
| 10 | RDa | Reset Drain, Quadrant a |
| 11 | H2SLa | Horizontal CCD Clock, Phase 2, Storage, Last Phase, Quadrant a |
| 12 | OGa | Output Gate, Quadrant a |
| 13 | H1Ba | Horizontal CCD Clock, Phase 1, Barrier, Quadrant a |
| 14 | H2Ba | Horizontal CCD Clock, Phase 2, Barrier, Quadrant a |
| 15 | H2Sa | Horizontal CCD Clock, Phase 2, Storage, Quadrant a |
| 16 | H1Sa | Horizontal CCD Clock, Phase 1, Storage, Quadrant a |
| 17 | SUB | Substrate |
| 18 | FDGab | Fast Line Dump Gate, Bottom |
| 19 | N/C | No Connect |
| 20 | FDGab | Fast Line Dump Gate, Bottom |
| 21 | H2Sb | Horizontal CCD Clock, Phase 2, Storage, Quadrant b |
| 22 | H1Sb | Horizontal CCD Clock, Phase 1, Storage, Quadrant b |
| 23 | H1Bb | Horizontal CCD Clock, Phase 1, Barrier, Quadrant b |
| 24 | H2Bb | Horizontal CCD Clock, Phase 2, Barrier, Quadrant b |
| 25 | H2SLb | Horizontal CCD Clock, Phase 2, Storage, Last Phase, Quadrant b |
| 26 | OGb | Output Gate, Quadrant b |
| 27 | Rb | Reset Gate, Quadrant b |
| 28 | RDb | Reset Drain, Quadrant b |
| 29 | GND | Ground |
| 30 | VOUTb | Video Output, Quadrant b |
| 31 | VDDb | Output Amplifier Supply, Quadrant b |
| 32 | V2B | Vertical CCD Clock, Phase 2, Bottom |
| 33 | V1B | Vertical CCD Clock, Phase 1, Bottom |
| 34 | V4B | Vertical CCD Clock, Phase 4, Bottom |
| 35 | V3B | Vertical CCD Clock, Phase 3, Bottom |
| 36 | ESD | ESD Protection Disable |

| Pin | Name | Description |
|---|---|---|
| 72 | ESD | ESD Protection Disable |
| 71 | V3T | Vertical CCD Clock, Phase 3, Top |
| 70 | V4T | Vertical CCD Clock, Phase 4, Top |
| 69 | V1T | Vertical CCD Clock, Phase 1, Top |
| 68 | V2T | Vertical CCD Clock, Phase 2, Top |
| 67 | VDDc | Output Amplifier Supply, Quadrant c |
| 66 | VOUTc | Video Output, Quadrant c |
| 65 | GND | Ground |
| 64 | RDc | Reset Drain, Quadrant c |
| 63 | Rc | Reset Gate, Quadrant c |
| 62 | OGc | Output Gate, Quadrant c |
| 61 | H2SLc | Horizontal CCD Clock, Phase 2, Storage, Last Phase, Quadrant c |
| 60 | H2Bc | Horizontal CCD Clock, Phase 2, Barrier, Quadrant c |
| 59 | H1Bc | Horizontal CCD Clock, Phase 1, Barrier, Quadrant c |
| 58 | H1Sc | Horizontal CCD Clock, Phase 1, Storage, Quadrant c |
| 57 | H2Sc | Horizontal CCD Clock, Phase 2, Storage, Quadrant c |
| 56 | FDGcd | Fast Line Dump Gate, Top |
| 55 | N/C | No Connect |
| 54 | FDGcd | Fast Line Dump Gate, Top |
| 53 | SUB | Substrate |
| 52 | H1Sd | Horizontal CCD Clock, Phase 1, Storage, Quadrant d |
| 51 | H2Sd | Horizontal CCD Clock, Phase 2, Storage, Quadrant d |
| 50 | H2Bd | Horizontal CCD Clock, Phase 2, Barrier, Quadrant d |
| 49 | H1Bd | Horizontal CCD Clock, Phase 1, Barrier, Quadrant d |
| 48 | OGd | Output Gate, Quadrant d |
| 47 | H2SLd | Horizontal CCD Clock, Phase 2, Storage, Last Phase, Quadrant d |
| 46 | RDd | Reset Drain, Quadrant d |
| 45 | Rd | Reset Gate, Quadrant d |
| 44 | VOUTd | Video Output, Quadrant d |
| 43 | GND | Ground |
| 42 | V2T | Vertical CCD Clock, Phase 2, Top |
| 41 | VDDd | Output Amplifier Supply, Quadrant d |
| 40 | V4T | Vertical CCD Clock, Phase 4, Top |
| 39 | V1T | Vertical CCD Clock, Phase 1, Top |
| 38 | DevID | Device Identification |
| 37 | V3T | Vertical CCD Clock, Phase 3, Top |

1. Liked named pins are internally connected and should have a common drive signal.
2. N/C pins (19, 55) should be left floating.

## IMAGING PERFORMANCE

### Table 6. TYPICAL OPERATION CONDITIONS

Unless otherwise noted, the Imaging Performance Specifications are measured using the following conditions.

| Description | Condition | Notes |
|---|---|---|
| Light Source | Continuous red, green and blue LED illumination | For monochrome sensor, only green LED used. |
| Operation | Nominal operating voltages and timing | |

### Table 7. SPECIFICATIONS
### All Configurations

| Description | Symbol | Min. | Nom. | Max. | Units | Sampling Plan | Temperature Tested At (°C) | Notes |
|---|---|---|---|---|---|---|---|---|
| Dark Field Global Non−Uniformity | DSNU | – | – | 5 | mVpp | Die | 27, 40 | |
| Bright Field Global Non−Uniformity | | – | 2 | 5 | %rms | Die | 27, 40 | 1 |
| Bright Field Global Peak to Peak Non−Uniformity | PRNU | – | 10 | 30 | %pp | Die | 27, 40 | 1 |
| Bright Field Center Non−Uniformity | | – | 1 | 2 | %rms | Die | 27, 40 | 1 |
| Maximum Photoresponse Nonlinearity | NL | – | 2 | – | % | Design | | 2 |
| Maximum Gain Difference Between Outputs | ΔG | – | 10 | – | % | Design | | 2 |
| Maximum Signal Error due to Nonlinearity Differences | ΔNL | – | 1 | – | % | Design | | 2 |
| Horizontal CCD Charge Capacity | HNe | – | 50 | – | ke⁻ | Design | | |
| Vertical CCD Charge Capacity | VNe | – | 45 | – | ke⁻ | Design | | |
| Photodiode Charge Capacity | PNe | – | 20 | – | ke⁻ | Die | 27, 40 | 3 |
| Horizontal CCD Charge Transfer Efficiency | HCTE | 0.999995 | 0.999999 | – | | Die | | |
| Vertical CCD Charge Transfer Efficiency | VCTE | 0.999995 | 0.999999 | – | | Die | | |
| Photodiode Dark Current | Ipd | – | 7 | 70 | e/p/s | Die | 40 | |
| Vertical CCD Dark Current | Ivd | – | 140 | 400 | e/p/s | Die | 40 | |
| Image Lag | Lag | – | – | 10 | e⁻ | Design | | |
| Antiblooming Factor | Xab | 300 | – | – | | Design | | |
| Vertical Smear | Smr | – | −100 | – | dB | Design | | |
| Read Noise | $n_{e-T}$ | – | 12 | – | e⁻rms | Design | | 4 |
| Dynamic Range | DR | – | 64 | – | dB | Design | | 4, 5 |
| Output Amplifier DC Offset | $V_{odc}$ | – | 9.4 | – | V | Die | 27, 40 | |
| Output Amplifier Bandwidth | $f_{-3db}$ | – | 250 | – | MHz | Die | | 6 |
| Output Amplifier Impedance | $R_{OUT}$ | – | 127 | – | Ω | Die | 27, 40 | |
| Output Amplifier Sensitivity | ΔV/ΔN | – | 34 | – | μV/e⁻ | Design | | |

1. Per color
2. Value is over the range of 10% to 90% of photodiode saturation.
3. The operating value of the substrate voltage, VAB, will be marked on the shipping container for each device. The value of VAB is set such that the photodiode charge capacity is 680 mV.
4. At 40 MHz
5. Uses 20LOG (PNe/ $n_{e-T}$)
6. Assumes 5 pF load.

**Table 8. KAI−29050−AXA, KAI−29050−QXA, AND KAI−29050−PXA[1] CONFIGURATIONS**

| Description | Symbol | Min. | Nom. | Max. | Units | Sampling Plan | Temperature Tested At (°C) | Notes |
|---|---|---|---|---|---|---|---|---|
| Peak Quantum Efficiency | $QE_{max}$ | – | 43 | – | % | Design | | |
| Peak Quantum Efficiency Wavelength | $\lambda QE$ | – | 470 | – | nm | Design | | |

1. This color filter set configuration (Gen1) is not recommended for new designs.

**Table 9. KAI−29050−FBA AND KAI−29050−QBA GEN2 COLOR CONFIGURATIONS WITH MAR GLASS**

| Description | | Symbol | Min. | Nom. | Max. | Units | Sampling Plan | Temperature Tested At (°C) | Notes |
|---|---|---|---|---|---|---|---|---|---|
| Peak Quantum Efficiency | Blue<br>Green<br>Red | $QE_{max}$ | – | 37<br>35<br>29 | – | % | Design | | |
| Peak Quantum Efficiency Wavelength | Blue<br>Green<br>Red | $\lambda QE$ | – | 460<br>530<br>605 | – | nm | Design | | |

**Table 10. KAI−29050−CBA AND KAI−29050−PBA GEN1 COLOR CONFIGURATIONS WITH MAR GLASS**

| Description | | Symbol | Min. | Nom. | Max. | Units | Sampling Plan | Temperature Tested At (°C) | Notes |
|---|---|---|---|---|---|---|---|---|---|
| Peak Quantum Efficiency | Blue<br>Green<br>Red | $QE_{max}$ | – | 38<br>35<br>28 | – | % | Design | | 1 |
| Peak Quantum Efficiency Wavelength | Blue<br>Green<br>Red | $\lambda QE$ | – | 470<br>540<br>620 | – | nm | Design | | 1 |

1. This color filter set configuration (Gen1) is not recommended for new designs.

## TYPICAL PERFORMANCE CURVES

### Quantum Efficiency

Monochrome with Microlens

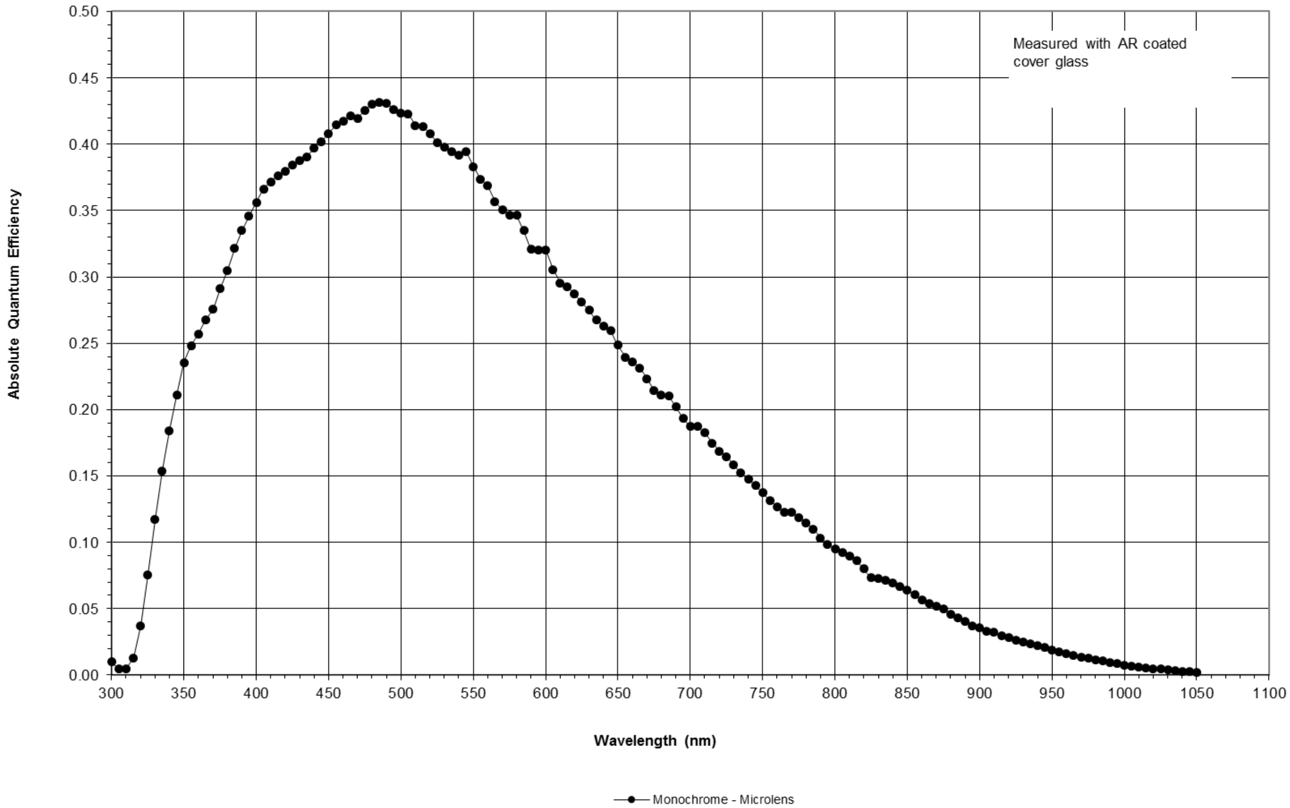



**Figure 6. Monochrome with Microlens Quantum Efficiency**

Color (Bayer RGB) with Microlens and MAR Cover Glass (Gen2 and Gen1 CFA)

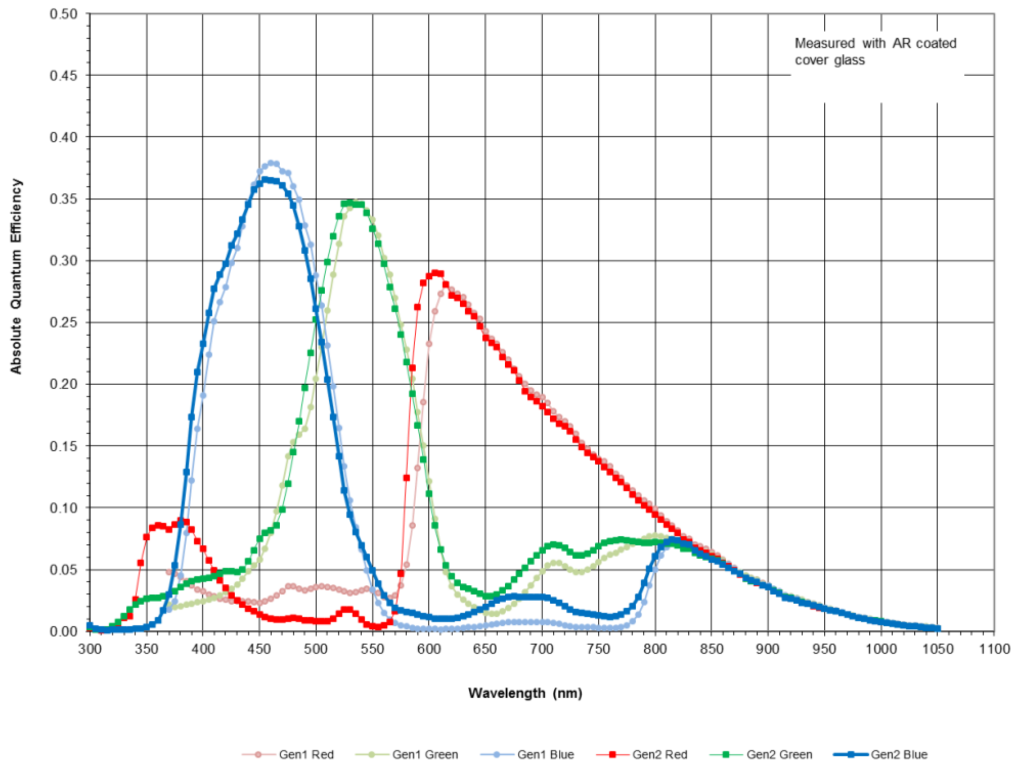



**Figure 7. Color (Bayer) with Microlens Quantum Efficiency**

Color (TRUESENSE Sparse CFA) with Microlens (Gen2 and Gen1 CFA)

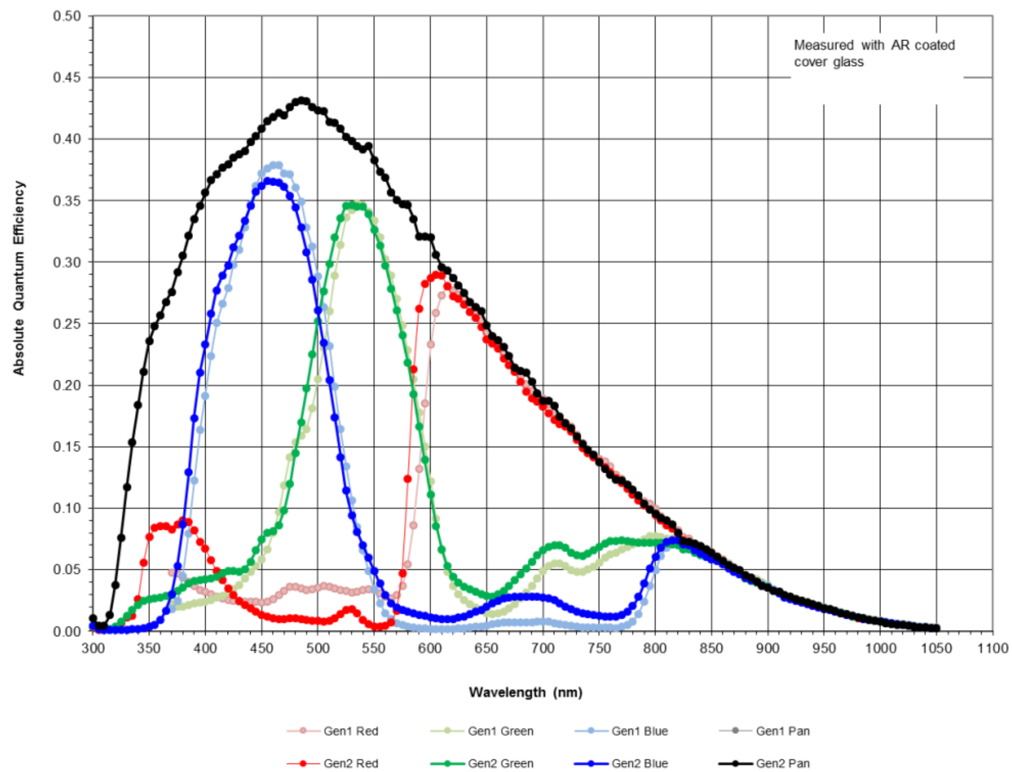



**Figure 8. Color (TRUESENSE Sparse CFA) with Microlens Quantum Efficiency**

### Angular Quantum Efficiency

For the curves marked "Horizontal", the incident light angle is varied in a plane parallel to the HCCD.

For the curves marked "Vertical", the incident light angle is varied in a plane parallel to the VCCD.

Monochrome with Microlens

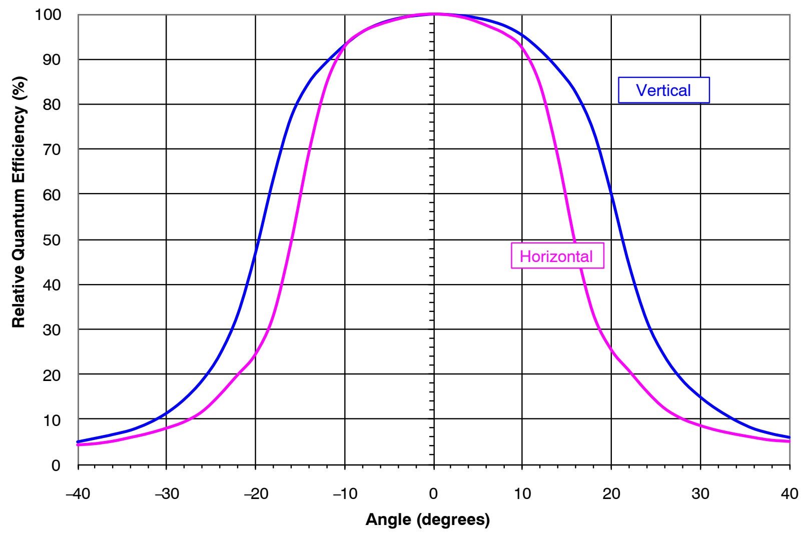



**Figure 9. Monochrome with Microlens Angular Quantum Efficiency**

### Dark Current versus Temperature

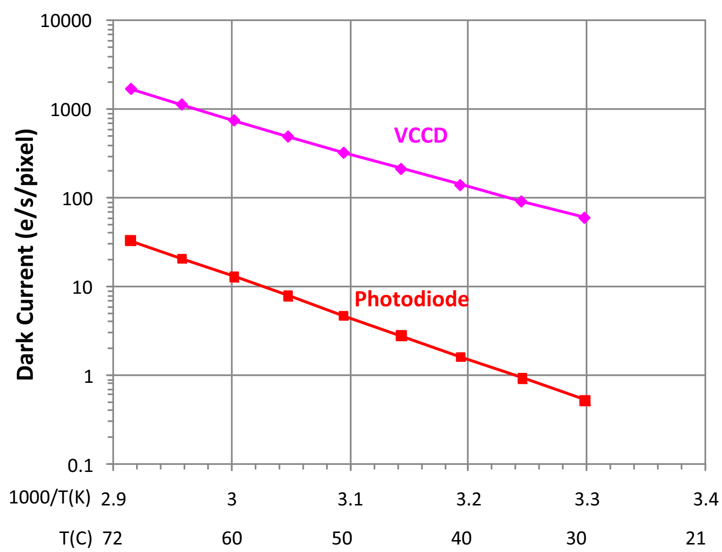



**Figure 10. Dark Current versus Temperature**

### Power − Estimated

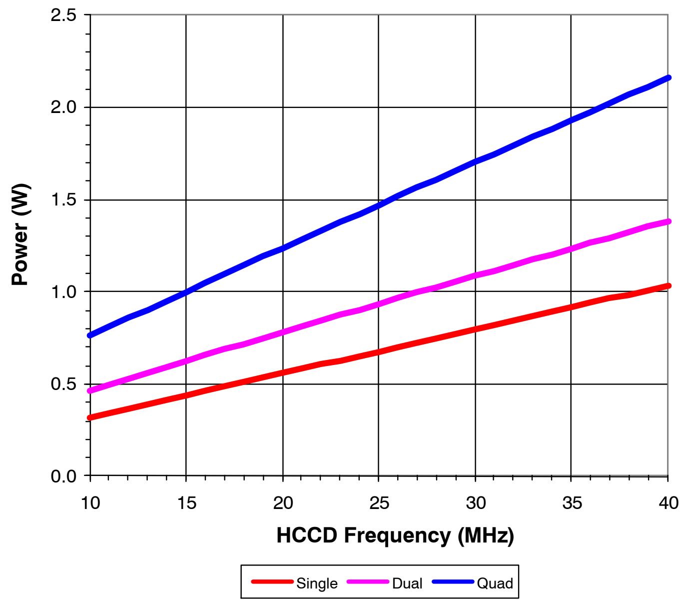



**Figure 11. Power**

### Frame Rates

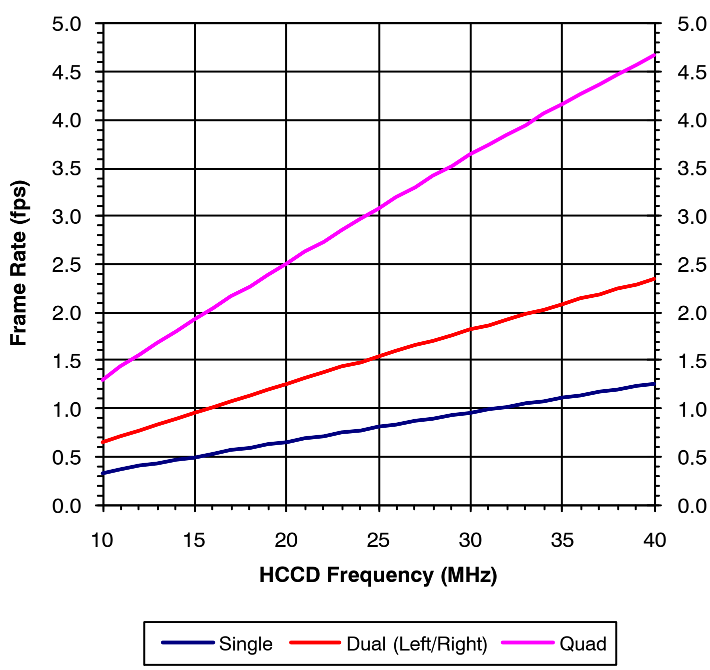



**Figure 12. Frame Rates**

## DEFECT DEFINITIONS

**Table 11. OPERATION CONDITIONS FOR DEFECT TESTING AT 40°C**

| Description | Condition | Notes |
|---|---|---|
| Operational Mode | Two outputs, using VOUTa and VOUTc, continuous readout | |
| HCCD Clock Frequency | 10 MHz | |
| Pixels Per Line | 6800 | 1 |
| Lines Per Frame | 2320 | 2 |
| Line Time | 715.7 μsec | |
| Frame Time | 1660.5 msec | |
| Photodiode Integration Time (PD_Tint) | Mode A: PD_Tint = Frame Time = 1660.5 msec, no electronic shutter used | |
| VCCD Integration Time | 1593.1 msec | 3 |
| Temperature | 40°C | |
| Light Source | Continuous red, green and blue LED illumination | 4 |
| Operation | Nominal operating voltages and timing | |

1. Horizontal overclocking used.
2. Vertical overclocking used.
3. VCCD Integration Time = 2226 lines x Line Time, which is the total time a pixel will spend in the VCCD registers.
4. For monochrome sensor, only the green LED is used.

**Table 12. DEFECT DEFINITIONS FOR TESTING AT 40°C**

| Description | Definition | Grade 1 | Grade 2 Mono | Grade 2 Color | Notes |
|---|---|---|---|---|---|
| Major dark field defective bright pixel | PD_Tint = Mode A → Defect ≥ 565 mV | 270 | 540 | 540 | 1 |
| Major bright field defective dark pixel | Defect ≥ 12% | | | | |
| Minor dark field defective bright pixel | PD_Tint = Mode A → Defect ≥ 282 mV | 2700 | 5400 | 5400 | |
| Cluster defect | A group of 2 to 19 contiguous major defective pixels, but no more than 4 adjacent defects horizontally. | 20 | n/a | n/a | 2 |
| Cluster defect | A group of 2 to 38 contiguous major defective pixels, but no more than 5 adjacent defects horizontally. | n/a | 50 | 50 | 2 |
| Column defect | A group of more than 10 contiguous major defective pixels along a single column | 0 | 7 | 27 | 2 |

1. For the color devices (KAI−29050−CXA and KAI−29050−PXA), a bright field defective pixel deviates by 12% with respect to pixels of the same color.
2. Column and cluster defects are separated by no less than two (2) good pixels in any direction (excluding single pixel defects).

**Table 13. OPERATION CONDITIONS FOR DEFECT TESTING AT 27°C**

| Description | Condition | Notes |
|---|---|---|
| Operational Mode | Two outputs, using VOUTa and VOUTc, continuous readout | |
| HCCD Clock Frequency | 10 MHz | |
| Pixels Per Line | 6800 | 1 |
| Lines Per Frame | 4544 | 2 |
| Line Time | 715.7 μsec | |
| Frame Time | 3252.2 msec | |
| Photodiode Integration Time (PD_Tint) | Mode A: PD_Tint = Frame Time = 3252.2 msec, no electronic shutter used | |
| VCCD Integration Time | 1593.1 msec | 3 |
| Temperature | 27°C | |
| Light Source | Continuous red, green and blue LED illumination | 4 |
| Operation | Nominal operating voltages and timing | |

1. Horizontal overclocking used.
2. Vertical overclocking used.
3. VCCD Integration Time = 2226 lines x Line Time, which is the total time a pixel will spend in the VCCD registers.
4. For monochrome sensor, only the green LED is used.

**Table 14. DEFECT DEFINITIONS FOR TESTING AT 27°C**

| Description | Definition | Grade 1 | Grade 2 Mono | Grade 2 Color | Notes |
|---|---|---|---|---|---|
| Major dark field defective bright pixel | PD_Tint = Mode A → Defect ≥ 183 mV | 270 | 540 | 540 | 1 |
| Major bright field defective dark pixel | Defect ≥ 12% | | | | |
| Cluster defect | A group of 2 to 19 contiguous major defective pixels, but no more than 4 adjacent defects horizontally. | 20 | n/a | n/a | 2 |
| Cluster defect | A group of 2 to 38 contiguous major defective pixels, but no more than 5 adjacent defects horizontally. | n/a | 50 | 50 | 2 |
| Column defect | A group of more than 10 contiguous major defective pixels along a single column | 0 | 7 | 27 | 2 |

1. For the color devices (KAI−29050−CXA and KAI−29050−PXA), a bright field defective pixel deviates by 12% with respect to pixels of the same color.
2. Column and cluster defects are separated by no less than two (2) good pixels in any direction (excluding single pixel defects).

### Defect Map

The defect map supplied with each sensor is based upon testing at an ambient (27°C) temperature. Minor point defects are not included in the defect map. All defective pixels are reference to pixel 1, 1 in the defect maps. See Figure 13: Regions of interest for the location of pixel 1,1.

## TEST DEFINITIONS

### Test Regions of Interest

| | |
|---|---|
| Image Area ROI: | Pixel (1, 1) to Pixel (6600, 4408) |
| Active Area ROI: | Pixel (13, 13) to Pixel (6588, 4396) |
| Center ROI: | Pixel (3251, 2155) to Pixel (3350, 2254) |

Only the Active Area ROI pixels are used for performance and defect tests.

### Overclocking

The test system timing is configured such that the sensor is overclocked in both the vertical and horizontal directions. See Figure 13 for a pictorial representation of the regions of interest.

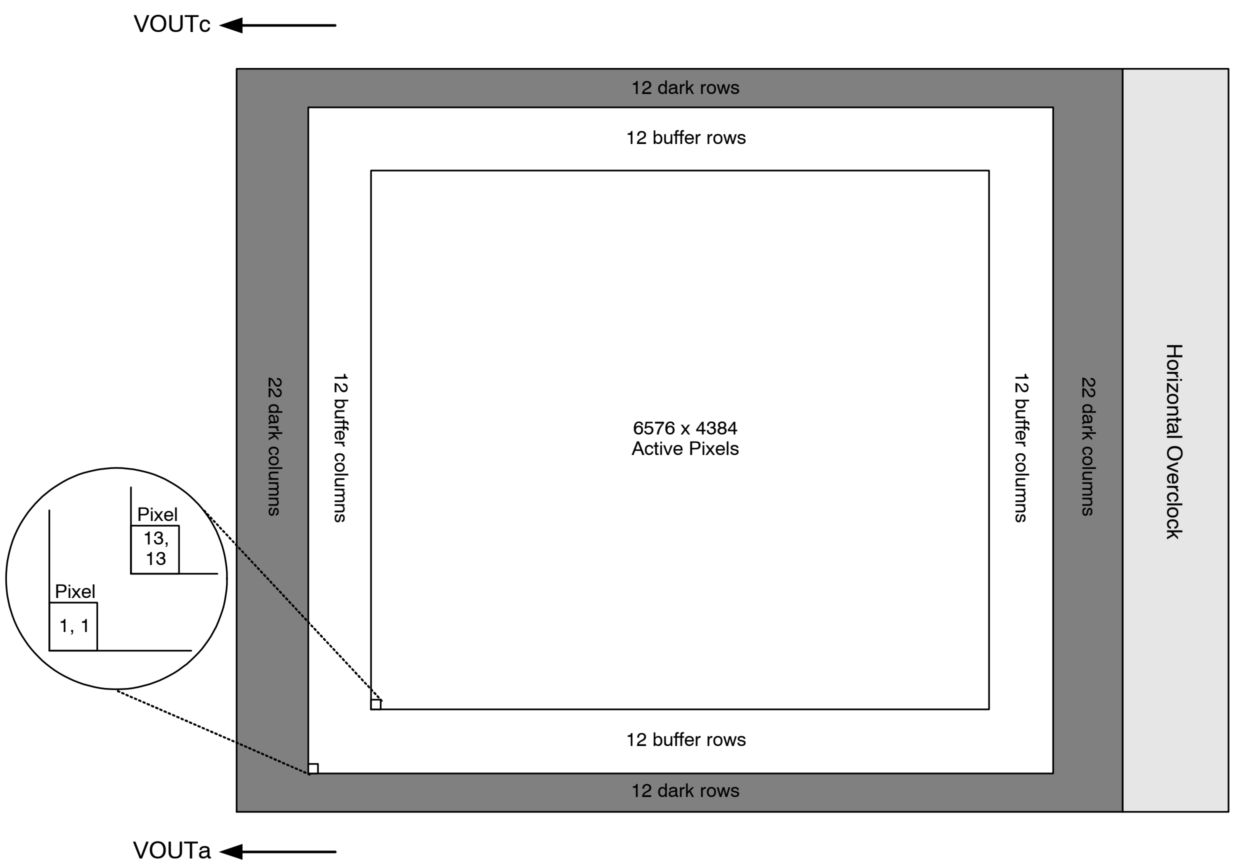



**Figure 13. Regions of Interest**

## Tests

*Dark Field Global Non−Uniformity*

This test is performed under dark field conditions. The sensor is partitioned into 1536 sub regions of interest, each of which is 137 by 137 pixels in size. The average signal level of each of the 1536 sub regions of interest is calculated. The signal level of each of the sub regions of interest is calculated using the following formula:

Signal of ROI[i] = (ROI Average in counts − Horizontal overclock average in counts) * mV per count

Where i = 1 to 1536. During this calculation on the 1536 sub regions of interest, the maximum and minimum signal levels are found. The dark field global uniformity is then calculated as the maximum signal found minus the minimum signal level found.

Units: mVpp (millivolts peak to peak)

*Global Non−Uniformity*

This test is performed with the imager illuminated to a level such that the output is at 70% of saturation (approximately 476 mV). Prior to this test being performed the substrate voltage has been set such that the charge capacity of the sensor is 680 mV. Global non−uniformity is defined as

$$\text{GlobalNon–Uniformity} = 100 \times \left(\frac{\text{ActiveAreaStandardDeviation}}{\text{ActiveAreaSignal}}\right)$$

Units: %rms.

Active Area Signal = Active Area Average − Dark Column Average

*Global Peak to Peak Non−Uniformity*

This test is performed with the imager illuminated to a level such that the output is at 70% of saturation (approximately 476 mV). Prior to this test being performed the substrate voltage has been set such that the charge capacity of the sensor is 680 mV. The sensor is partitioned into 1536 sub regions of interest, each of which is 137 by 137 pixels in size. The average signal level of each of the 1536 sub regions of interest (ROI) is calculated. The signal level of each of the sub regions of interest is calculated using the following formula:

Signal of ROI[i] = (ROI Average in counts − Horizontal overclock average in counts) * mV per count

Where i = 1 to 1536. During this calculation on the 1536 sub regions of interest, the maximum and minimum signal levels are found. The global peak to peak uniformity is then calculated as:

$$\text{GlobalUniformity} = 100 \times \frac{\text{MaximumSignal} - \text{MinimumSignal}}{\text{ActiveAreaSignal}}$$

Units: %pp

*Center Non−Uniformity*

This test is performed with the imager illuminated to a level such that the output is at 70% of saturation (approximately 476 mV). Prior to this test being performed the substrate voltage has been set such that the charge capacity of the sensor is 680 mV. Defects are excluded for the calculation of this test. This test is performed on the center 100 by 100 pixels of the sensor. Center uniformity is defined as:

$$\text{Center ROI Uniformity} = 100 \times \left(\frac{\text{Center ROI Standard Deviation}}{\text{Center ROI Signal}}\right)$$

Units: %rms.

Center ROI Signal = Center ROI Average − Dark Column Average

*Dark Field Defect Test*

This test is performed under dark field conditions. The sensor is partitioned into 1536 sub regions of interest, each of which is 137 by 137 pixels in size. In each region of interest, the median value of all pixels is found. For each region of interest, a pixel is marked defective if it is greater than or equal to the median value of that region of interest plus the defect threshold specified in the "Defect Definitions" section.

*Bright Field Defect Test*

This test is performed with the imager illuminated to a level such that the output is at approximately 476 mV. Prior to this test being performed the substrate voltage has been set such that the charge capacity of the sensor is 680 mV. The average signal level of all active pixels is found. The bright and dark thresholds are set as:

Dark defect threshold = Active Area Signal * threshold

The sensor is then partitioned into 1536 sub regions of interest, each of which is 137 by 137 pixels in size. In each region of interest, the average value of all pixels is found. For each region of interest, a pixel is marked defective if it is greater than or equal to the median value of that region of interest plus the bright threshold specified or if it is less than or equal to the median value of that region of interest minus the dark threshold specified.

Example for major bright field defective pixels:

- Average value of all active pixels is found to be 476 mV
- Dark defect threshold: 476 mV * 12 % = 57 mV
- Region of interest #1 selected. This region of interest is pixels 13, 13 to pixels 149, 149.
  - Median of this region of interest is found to be 470 mV.
  - Any pixel in this region of interest that is ≤ (470 − 57 mV) 413 mV in intensity will be marked defective.
- All remaining 1536 sub regions of interest are analyzed for defective pixels in the same manner.

## OPERATION

**Table 15. ABSOLUTE MAXIMUM RATINGS**

| Description | Symbol | Minimum | Maximum | Units | Notes |
|---|---|---|---|---|---|
| Operating Temperature | $T_{OP}$ | −50 | +70 | °C | 1 |
| Humidity | RH | +5 | +90 | % | 2 |
| Output Bias Current | $I_{out}$ | | 60 | mA | 3 |
| Off−chip Load | CL | | 10 | pF | |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Noise performance will degrade at higher temperatures.
2. T = 25°C. Excessive humidity will degrade MTTF.
3. Total for all outputs. Maximum current is −15 mA for each output. Avoid shorting output pins to ground or any low impedance source during operation. Amplifier bandwidth increases at higher current and lower load capacitance at the expense of reduced gain (sensitivity).

**Table 16. ABSOLUTE MAXIMUM VOLTAGE RATINGS BETWEEN PINS AND GROUND**

| Description | Minimum | Maximum | Units | Notes |
|---|---|---|---|---|
| VDDα, VOUTα | −0.4 | 17.5 | V | 1 |
| RDα | −0.4 | 15.5 | V | 1 |
| V1B, V1T | ESD − 0.4 | ESD + 24.0 | V | |
| V2B, V2T, V3B, V3T, V4B, V4T | ESD − 0.4 | ESD + 14.0 | V | |
| FDGab, FDGcd | ESD − 0.4 | ESD + 15.0 | V | |
| H1Sα, H1Bα, H2Sα, H2Bα, H2SLα, Rα, OGα | ESD − 0.4 | ESD + 14.0 | V | 1 |
| ESD | −10.0 | 0.0 | V | |
| SUB | −0.4 | 40.0 | V | 2 |

1. α denotes a, b, c or d
2. Refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible Lighting Conditions.*

### Power−Up and Power−Down Sequence

Adherence to the power−up and power−down sequence is critical. Failure to follow the proper power−up and power−down sequences may cause damage to the sensor.

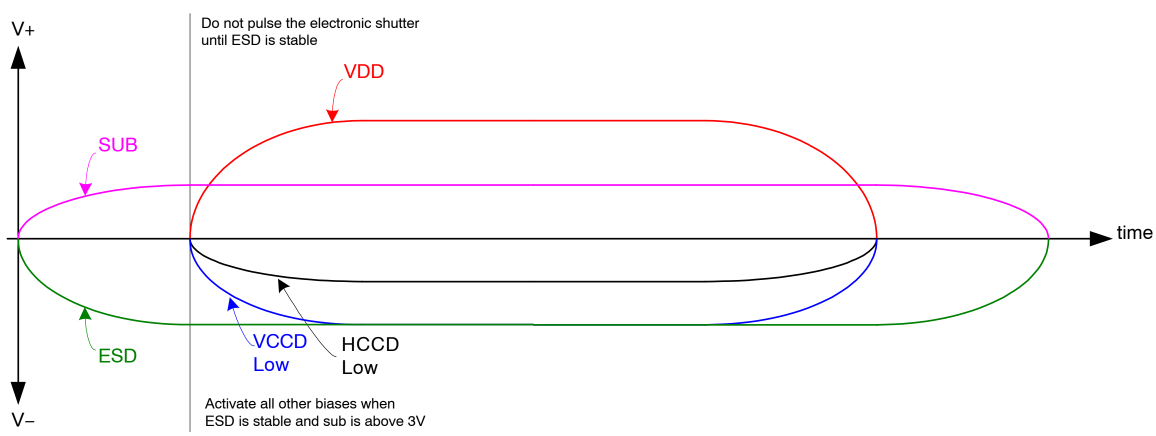



**Figure 14. Power−Up and Power−Down Sequence**

Notes:

1. Activate all other biases when ESD is stable and SUB is above 3 V
2. Do not pulse the electronic shutter until ESD is stable
3. VDD cannot be +15 V when SUB is 0 V
4. The image sensor can be protected from an accidental improper ESD voltage by current limiting the SUB current to less than 10 mA. SUB and VDD must always be greater than GND. ESD must always be less than GND. Placing diodes between SUB, VDD, ESD and ground will protect

the sensor from accidental overshoots of SUB, VDD and ESD during power on and power off. See the figure below.

The VCCD clock waveform must not have a negative overshoot more than 0.4 V below the ESD voltage.

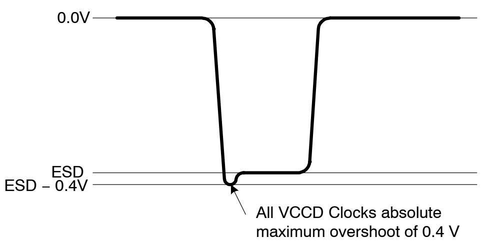



**Figure 15.**

Example of external diode protection for SUB, VDD and ESD. α denotes a, b, c or d

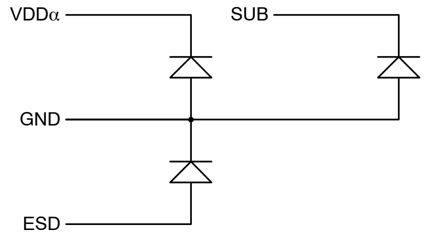



**Figure 16.**

**Table 17. DC BIAS OPERATING CONDITIONS**

| Description | Pins | Symbol | Minimum | Nominal | Maximum | Units | Maximum DC Current | Notes |
|---|---|---|---|---|---|---|---|---|
| Reset Drain | RDα | RD | +11.8 | +12.0 | +12.2 | V | 10 μA | 1 |
| Output Gate | OGα | OG | −2.2 | −2.0 | −1.8 | V | 10 μA | 1 |
| Output Amplifier Supply | VDDα | VDD | +14.5 | +15.0 | +15.5 | V | 11.0 mA | 1,2 |
| Ground | GND | GND | 0.0 | 0.0 | 0.0 | V | −1.0 mA | |
| Substrate | SUB | VSUB | +5.0 | VAB | VDD | V | 50 μA | 3, 8 |
| ESD Protection Disable | ESD | ESD | −9.2 | −9.0 | −8.8 | V | 50 μA | 6, 7 |
| Output Bias Current | VOUTα | Iout | −3.0 | −7.0 | −10.0 | mA | | 1, 4, 5 |

1. α denotes a, b, c or d
2. The maximum DC current is for one output. Idd = Iout + Iss. See Figure 17.
3. The operating value of the substrate voltage, VAB, will be marked on the shipping container for each device. The value of VAB is set such that the photodiode charge capacity is the nominal PNe (see Specifications).
4. An output load sink must be applied to each VOUT pin to activate each output amplifier.
5. Nominal value required for 40 MHz operation per output. May be reduced for slower data rates and lower noise.
6. Adherence to the power−up and power−down sequence is critical. See Power−Up and Power−Down Sequence section.
7. ESD maximum value must be less than or equal to V1_L + 0.4 V and V2_L + 0.4 V
8. Refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible Lighting Conditions*

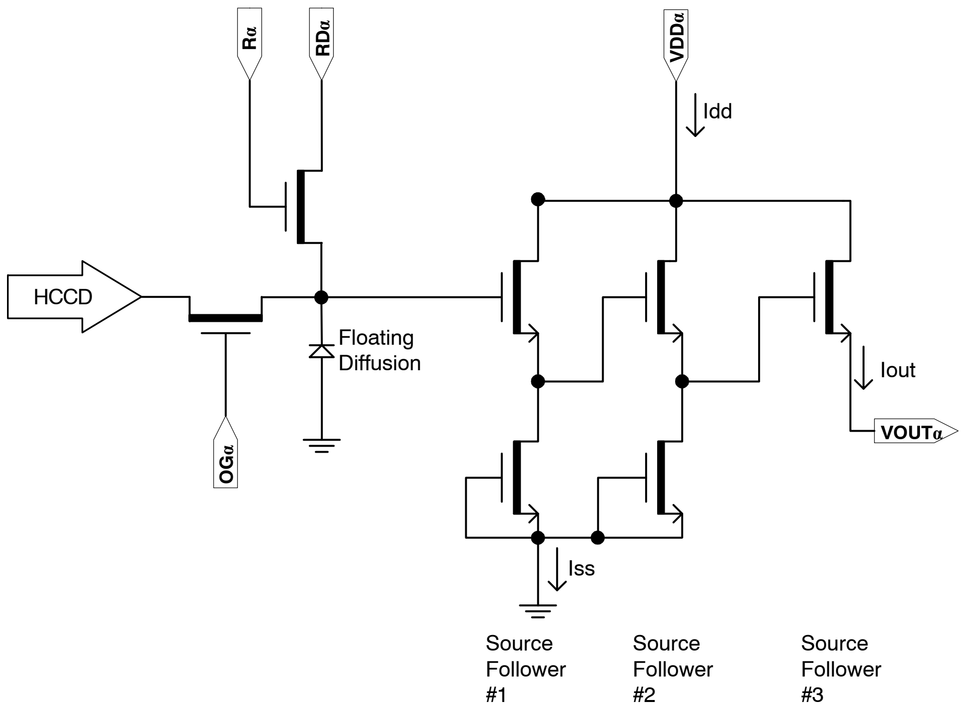



**Figure 17. Output Amplifier**

## AC Operating Conditions

**Table 18. CLOCK LEVELS**

| Description | Pins[1] | Symbol | Level | Minimum | Nominal | Maximum | Units | Capacitance[2] |
|---|---|---|---|---|---|---|---|---|
| Vertical CCD Clock, Phase 1 | V1B, V1T | V1_L | Low | −9.2 | −9.0 | −8.8 | V | 180 nF (6) |
| | | V1_M | Mid | −0.2 | 0.0 | +0.2 | | |
| | | V1_H | High | +12.8 | +13.0 | +14.0 | | |
| Vertical CCD Clock, Phase 2 | V2B, V2T | V2_L | Low | −9.2 | −9.0 | −8.8 | V | 180 nF (6) |
| | | V2_H | High | −0.2 | 0.0 | +0.2 | | |
| Vertical CCD Clock, Phase 3 | V3B, V3T | V3_L | Low | −9.2 | −9.0 | −8.8 | V | 180 nF (6) |
| | | V3_H | High | −0.2 | 0.0 | +0.2 | | |
| Vertical CCD Clock, Phase 4 | V4B, V4T | V4_L | Low | −9.2 | −9.0 | −8.8 | V | 180 nF (6) |
| | | V4_H | High | −0.2 | 0.0 | +0.2 | | |
| Horizontal CCD Clock, Phase 1 Storage | H1Sα | H1S_L | Low | −5.0 (7) | −4.4 | −4.2 | V | 600 pF (6) |
| | | H1S_A | Amplitude | +4.2 | +4.4 | +5.0 (7) | | |
| Horizontal CCD Clock, Phase 1 Barrier | H1Bα | H1B_L | Low | −5.0 (7) | −4.4 | −4.2 | V | 400 pF (6) |
| | | H1B_A | Amplitude | +4.2 | +4.4 | +5.0 (7) | | |
| Horizontal CCD Clock, Phase 2 Storage | H2Sα | H2S_L | Low | −5.0 (7) | −4.4 | −4.2 | V | 580 pF (6) |
| | | H2S_A | Amplitude | +4.2 | +4.4 | +5.0 (7) | | |
| Horizontal CCD Clock, Phase 2 Barrier | H2Bα | H2B_L | Low | −5.0 (7) | −4.4 | −4.2 | V | 400 pF (6) |
| | | H2B_A | Amplitude | +4.2 | +4.4 | +5.0 (7) | | |
| Horizontal CCD Clock, Last Phase [3] | H2SLα | H2SL_L | Low | −5.2 | −5.0 | −4.8 | V | 20 pF (6) |
| | | H2SL_A | Amplitude | +4.8 | +5.0 | +5.2 | | |
| Reset Gate | Rα | R_L [4] | Low | −3.5 | −2.0 | −1.5 | V | 16 pF (6) |
| | | R_H | High | +2.5 | +3.0 | +4.0 | | |
| Electronic Shutter [5] | SUB | VES | High | +29.0 | +30.0 | +40.0 | V | 12 nF (6) |
| Fast Line Dump Gate | FDGα | FDG_L | Low | −9.2 | −9.0 | −8.8 | V | 50 pF (6) |
| | | FDG_H | High | +4.5 | +5.0 | +5.5 | | |

1. α denotes a, b, c or d
2. Capacitance is total for all like named pins
3. Use separate clock driver for improved speed performance.
4. Reset low should be set to –3 volts for signal levels greater than 40,000 electrons.
5. Refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible Lighting Conditions*
6. Capacitance values are estimated
7. If the minimum horizontal clock low level is used (–5.0 V), then the maximum horizontal clock amplitude should be used (5 V amplitude) to create a –5.0 V to 0.0 V clock.

The figure below shows the DC bias (VSUB) and AC clock (VES) applied to the SUB pin. Both the DC bias and AC clock are referenced to ground.

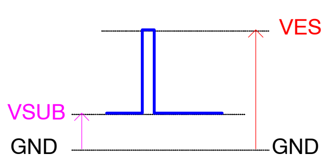



**Figure 18.**

### Device Identification

The device identification pin (DevID) may be used to determine which ON Semiconductor 5.5 micron pixel interline CCD sensor is being used.

**Table 19. DEVICE IDENTIFICATION**

| Description | Pins | Symbol | Minimum | Nominal | Maximum | Units | Maximum DC Current | Notes |
|---|---|---|---|---|---|---|---|---|
| Device Identification | DevID | DevID | 200,000 | 300,000 | 400,000 | Ω | 50 μA | 1, 2, 3 |

1. Nominal value subject to verification and/or change during release of preliminary specifications.
2. If the Device Identification is not used, it may be left disconnected.
3. After Device Identification resistance has been read during camera initialization, it is recommended that the circuit be disabled to prevent localized heating of the sensor due to current flow through the R_DeviceID resistor.

*Recommended Circuit*

Note that V1 must be a different value than V2.

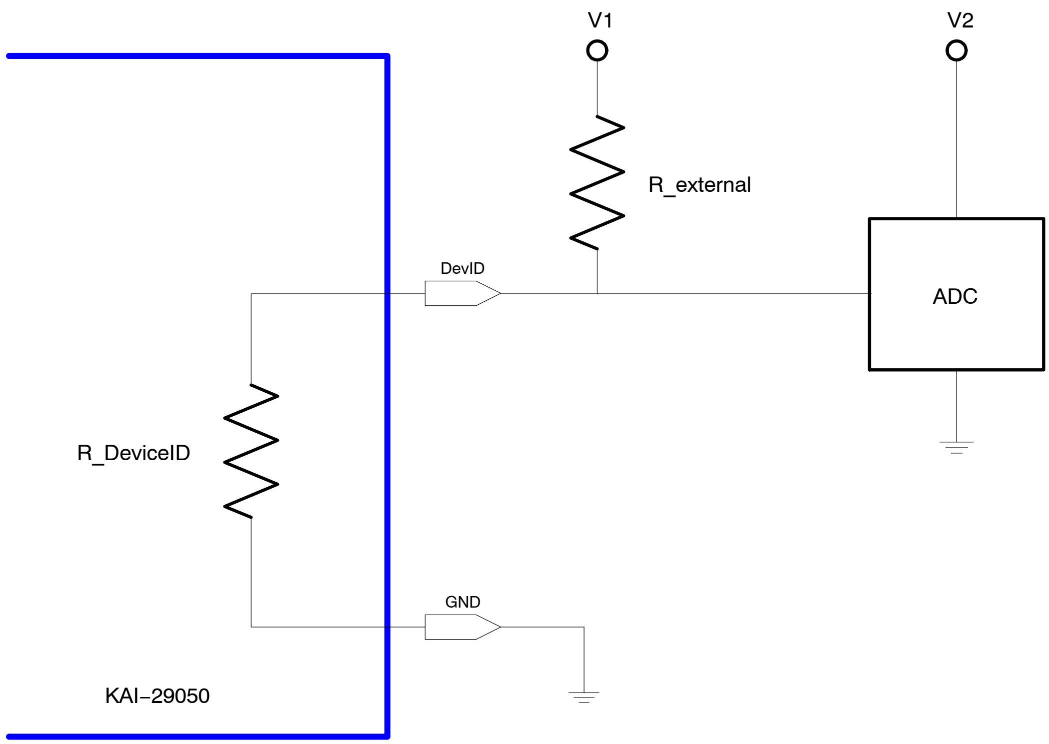



**Figure 19. Device Identification Recommended Circuit**

## TIMING

### Table 20. REQUIREMENTS AND CHARACTERISTICS

| Description | Symbol | Minimum | Nominal | Maximum | Units | Notes |
|---|---|---|---|---|---|---|
| Photodiode Transfer | $t_{pd}$ | 6 | – | – | μs | |
| VCCD Leading Pedestal | $t_{3p}$ | 16 | – | – | μs | |
| VCCD Trailing Pedestal | $t_{3d}$ | 16 | – | – | μs | |
| VCCD Transfer Delay | $t_d$ | 4 | – | – | μs | |
| VCCD Transfer | $t_v$ | 8 | – | – | μs | |
| VCCD Clock Cross−over | $v_{VCR}$ | 75 | | 100 | % | 1 |
| VCCD Rise, Fall Times | $t_{VR}$, $t_{VF}$ | 5 | – | 10 | % | 1, 2 |
| FDG Delay | $t_{fdg}$ | 2 | – | – | μs | |
| HCCD Delay | $t_{hs}$ | 1 | – | – | μs | |
| HCCD Transfer | $t_e$ | 25.0 | 29.4 | – | ns | |
| Shutter Transfer | $t_{sub}$ | 1 | – | – | μs | |
| Shutter Delay | $t_{hd}$ | 1 | – | – | μs | |
| Reset Pulse | $t_r$ | 2.5 | – | – | ns | |
| Reset – Video Delay | $t_{rv}$ | – | 2.2 | – | ns | |
| H2SL – Video Delay | $t_{hv}$ | – | 3.1 | – | ns | |
| Line Time | $t_{line}$ | 96.3 | 110.0 | – | μs | Dual HCCD Readout |
| | | 179.4 | 208.7 | – | | Single HCCD Readout |
| Frame Time | $t_{frame}$ | 213.5 | 246.1 | – | ms | Quad HCCD Readout |
| | | 427.0 | 492.2 | – | | Dual HCCD Readout |
| | | 795.1 | 925.2 | – | | Single HCCD Readout |

1. Refer to Figure 25: VCCD Clock Rise Time, Fall Time and Edge Alignment
2. Relative to the pulse width
3. Refer to timing diagrams as shown in Figures 21, 22, 23, 24 and 25.

### Timing Diagrams

The timing sequence for the clocked device pins may be represented as one of seven patterns (P1−P7) as shown in the table below. The patterns are defined in Figure 21 and Figure 22. Contact ON Semiconductor Application Engineering for other readout modes.

**Table 21.**

<table>
<tr><th>Device Pin</th><th>Quad Readout</th><th>Dual Readout VOUTa, VOUTb</th><th>Dual Readout VOUTa, VOUTc</th><th>Single Readout VOUTa</th></tr>
<tr><td>V1T</td><td>P1T</td><td>P1B</td><td>P1T</td><td>P1B</td></tr>
<tr><td>V2T</td><td>P2T</td><td>P4B</td><td>P2T</td><td>P4B</td></tr>
<tr><td>V3T</td><td>P3T</td><td>P3B</td><td>P3T</td><td>P3B</td></tr>
<tr><td>V4T</td><td>P4T</td><td>P2B</td><td>P4T</td><td>P2B</td></tr>
<tr><td>V1B</td><td colspan="4">P1B</td></tr>
<tr><td>V2B</td><td colspan="4">P2B</td></tr>
<tr><td>V3B</td><td colspan="4">P3B</td></tr>
<tr><td>V4B</td><td colspan="4">P4B</td></tr>
<tr><td>H1Sa</td><td colspan="4" rowspan="2">P5</td></tr>
<tr><td>H1Ba</td></tr>
<tr><td>H2Sa [2]</td><td colspan="4" rowspan="2">P6</td></tr>
<tr><td>H2Ba</td></tr>
<tr><td>Ra</td><td colspan="4">P7</td></tr>
<tr><td>H1Sb</td><td colspan="2" rowspan="2">P5</td><td colspan="2">P5</td></tr>
<tr><td>H1Bb</td><td colspan="2">P6</td></tr>
<tr><td>H2Sb [2]</td><td colspan="2" rowspan="2">P6</td><td colspan="2">P6</td></tr>
<tr><td>H2Bb</td><td colspan="2">P5</td></tr>
<tr><td>Rb</td><td colspan="2">P7</td><td>P7 [1] or Off [3]</td><td>P7 [1] or Off [3]</td></tr>
<tr><td>H1Sc</td><td rowspan="2">P5</td><td rowspan="2">P5 [1] or Off [3]</td><td rowspan="2">P5</td><td rowspan="2">P5 [1] or Off [3]</td></tr>
<tr><td>H1Bc</td></tr>
<tr><td>H2Sc [2]</td><td rowspan="2">P6</td><td rowspan="2">P6 [1] or Off [3]</td><td rowspan="2">P6</td><td rowspan="2">P6 [1] or Off [3]</td></tr>
<tr><td>H2Bc</td></tr>
<tr><td>Rc</td><td>P7</td><td>P7 [1] or Off [3]</td><td>P7</td><td>P7 [1] or Off [3]</td></tr>
<tr><td>H1Sd</td><td rowspan="2">P5</td><td rowspan="2">P5 [1] or Off [3]</td><td>P5</td><td rowspan="2">P5 [1] or Off [3]</td></tr>
<tr><td>H1Bd</td><td>P6</td></tr>
<tr><td>H2Sd [2]</td><td rowspan="2">P6</td><td rowspan="2">P6 [1] or Off [3]</td><td>P6</td><td rowspan="2">P6 [1] or Off [3]</td></tr>
<tr><td>H2Bd</td><td>P5</td></tr>
<tr><td>Rd</td><td>P7</td><td>P7 [1] or Off [3]</td><td>P7 [1] or Off [3]</td><td>P7 [1] or Off [3]</td></tr>
</table>

<table>
<tr><td># Lines/Frame (Minimum)</td><td>2226</td><td>4452</td><td>2226</td><td>4452</td></tr>
<tr><td># Pixels/Line (Minimum)</td><td colspan="2">3333</td><td colspan="2">6666</td></tr>
</table>

1. For optimal performance of the sensor. May be clocked at a lower frequency. If clocked at a lower frequency, the frequency selected should be a multiple of the frequency used on the a and b register.
2. H2SLx follows the same pattern as H2Sx For optimal speed performance, use a separate clock driver.
3. Off = +5 V. Note that there may be operating conditions (high temperature and/or very bright light sources) that will cause blooming from the unused c/d register into the image area.

### Photodiode Transfer Timing

A row of charge is transferred to the HCCD on the falling edge of V1 as indicated in the P1 pattern below. Using this timing sequence, the leading dummy row or line is combined with the first dark row in the HCCD. The “Last Line” is dependent on readout mode – either 2226 or 4452 minimum counts required. It is important to note that, in general, the rising edge of a vertical clock (patterns P1−P4) should be coincident or slightly leading a falling edge at the same time interval. This is particularly true at the point where P1 returns from the high (3rd level) state to the mid−state when P4 transitions from the low state to the high state.

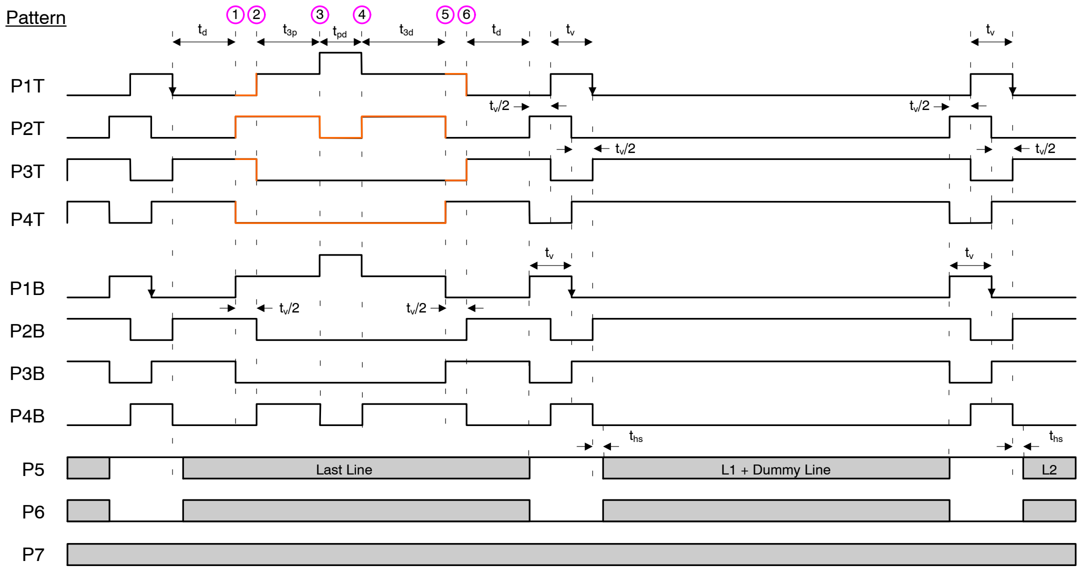



**Figure 20. Photodiode Transfer Timing**

### Line and Pixel Timing

Each row of charge is transferred to the output, as illustrated below, on the falling edge of H2SL (indicated as P6 pattern). The number of pixels in a row is dependent on readout mode – either 3333 or 6666 minimum counts required.

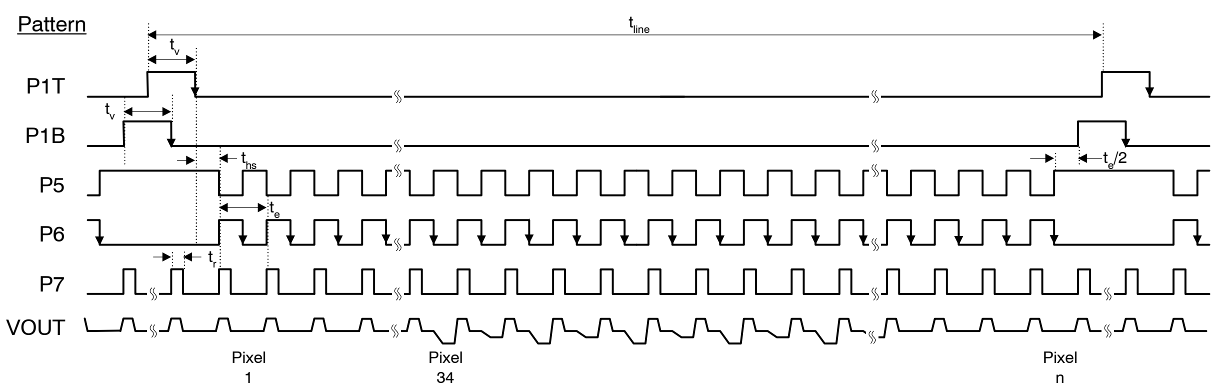



**Figure 21. Line and Pixel Timing**

### Pixel Timing Detail

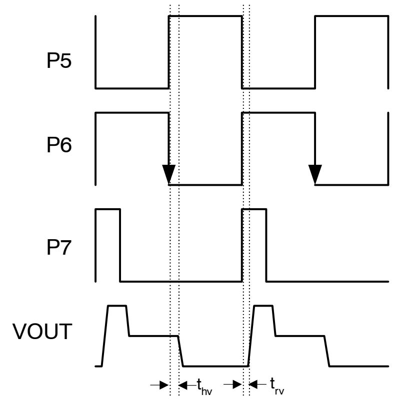



**Figure 22. Pixel Timing Detail**

### Frame/Electronic Shutter Timing

The SUB pin may be optionally clocked to provide electronic shuttering capability as shown below.

The resulting photodiode integration time is defined from the falling edge of SUB to the falling edge of V1 (P1 pattern).

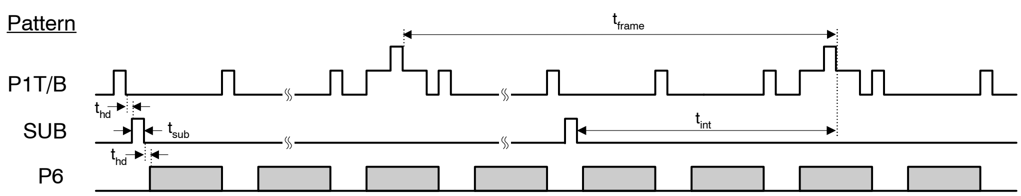



**Figure 23. Frame/Electronic Shutter Timing**

### VCCD Clock Edge Alignment

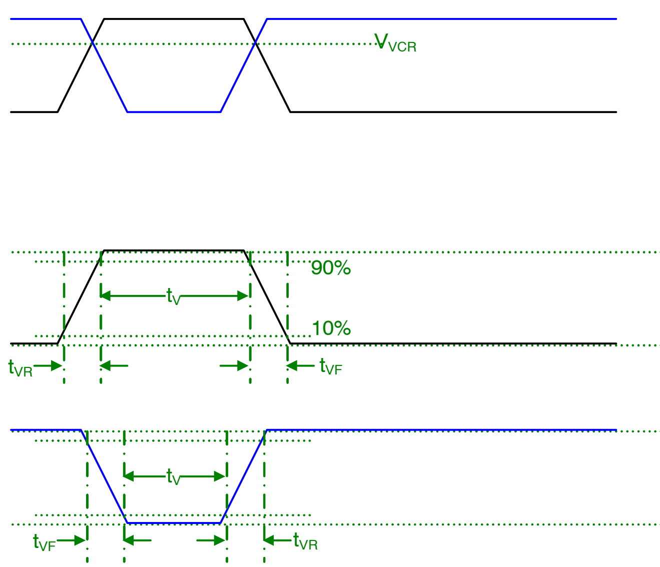



**Figure 24. VCCD Clock Rise Time, Fall Time and Edge Alignment**

### Line and Pixel Timing − Vertical Binning by 2

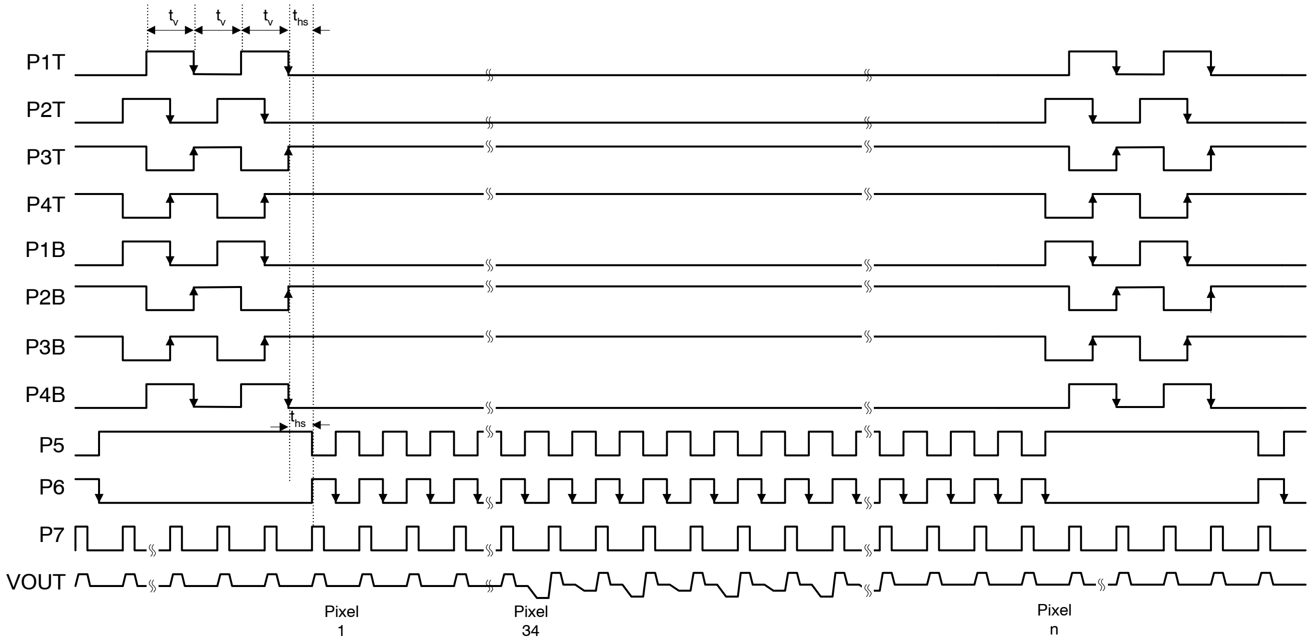



**Figure 25. Line and Pixel Timing − Vertical Binning by 2**

### Fast Line Dump Timing

The FDG pins may be optionally clocked to efficiently remove unwanted lines in the image resulting for increased frame rates at the expense of resolution. Below is an example of a 2 line dump sequence followed by a normal readout line. Note that the FDG timing transitions should complete prior to the beginning of V1 timing transitions as illustrated below.

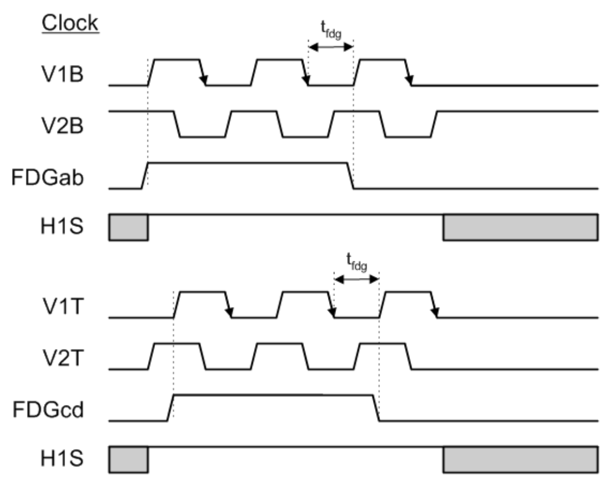



**Figure 26. Fast Line Dump Timing**

## STORAGE AND HANDLING

**Table 22. STORAGE CONDITIONS**

| Description | Symbol | Minimum | Maximum | Units | Notes |
|---|---|---|---|---|---|
| Storage Temperature | $T_{ST}$ | −55 | +80 | °C | 1 |
| Humidity | RH | 5 | 90 | % | 2 |

1. Long term storage toward the maximum temperature will accelerate color filter degradation.
2. T = 25°C. Excessive humidity will degrade MTTF.

For information on ESD and cover glass care and cleanliness, please download the *Image Sensor Handling and Best Practices* Application Note (AN52561/D) from www.onsemi.com.

For information on soldering recommendations, please download the Soldering and Mounting Techniques Reference Manual (SOLDERRM/D) from www.onsemi.com.

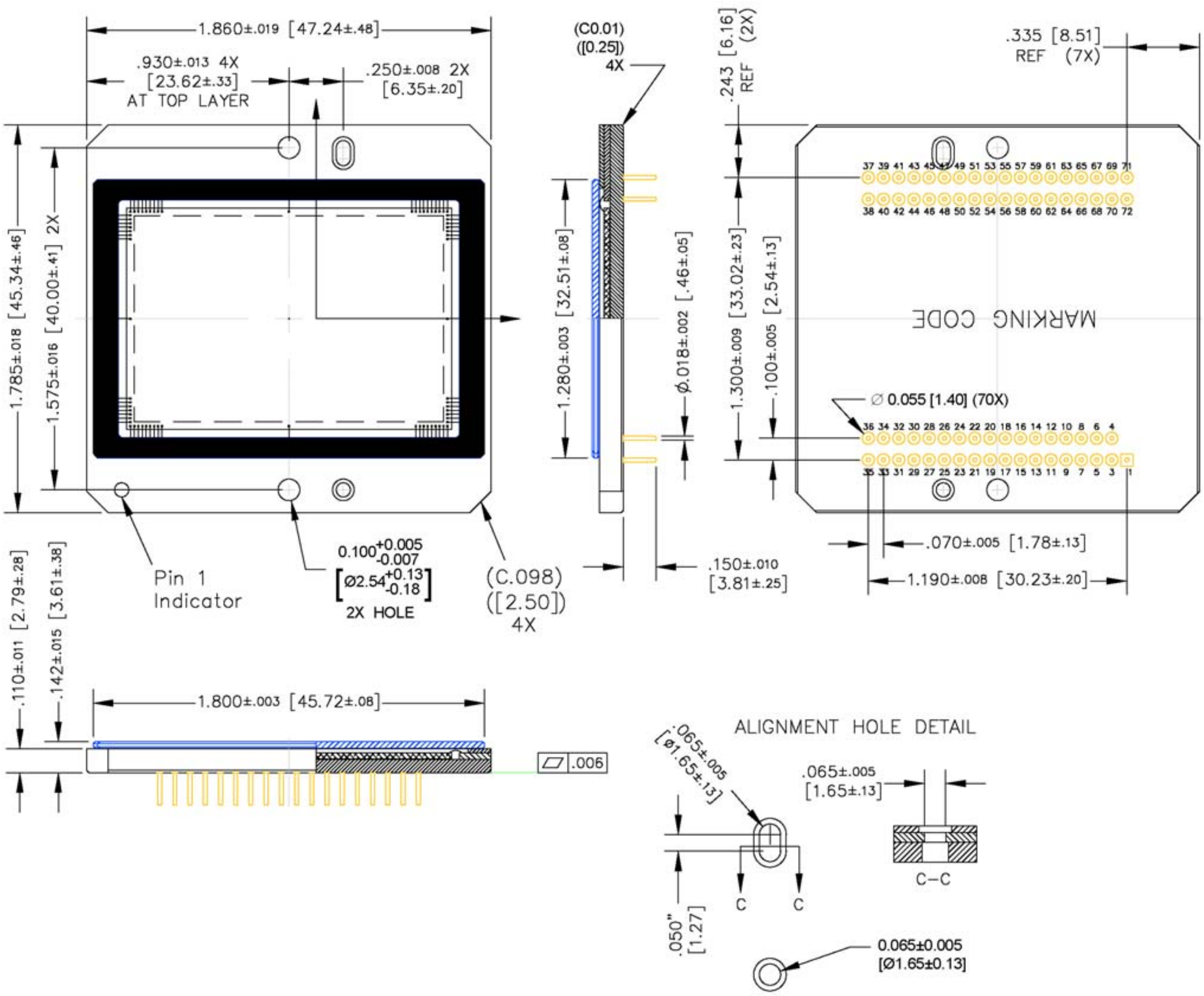
For quality and reliability information, please download the *Quality & Reliability* Handbook (HBD851/D) from www.onsemi.com.

For information on device numbering and ordering codes, please download the *Device Nomenclature* technical note (TND310/D) from www.onsemi.com.

For information on Standard terms and Conditions of Sale, please download Terms and Conditions from www.onsemi.com.

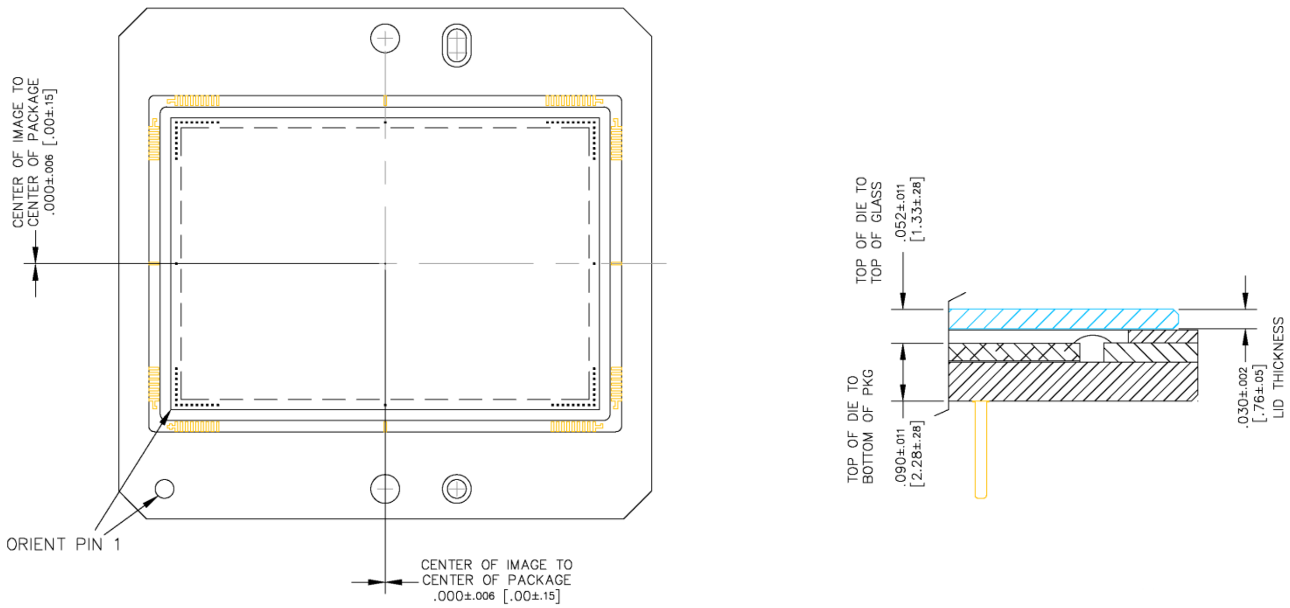
## MECHANICAL INFORMATION

### Completed Assembly




Notes:
1. See Ordering Information for marking code.
2. Cover glass not to overhang package holes or outer ceramic edges.
3. Glass epoxy not to extend over image array.
4. No materials to interfere with clearance through package holes.
5. Units: IN [MM]

**Figure 27. Completed Assembly (1 of 2)**

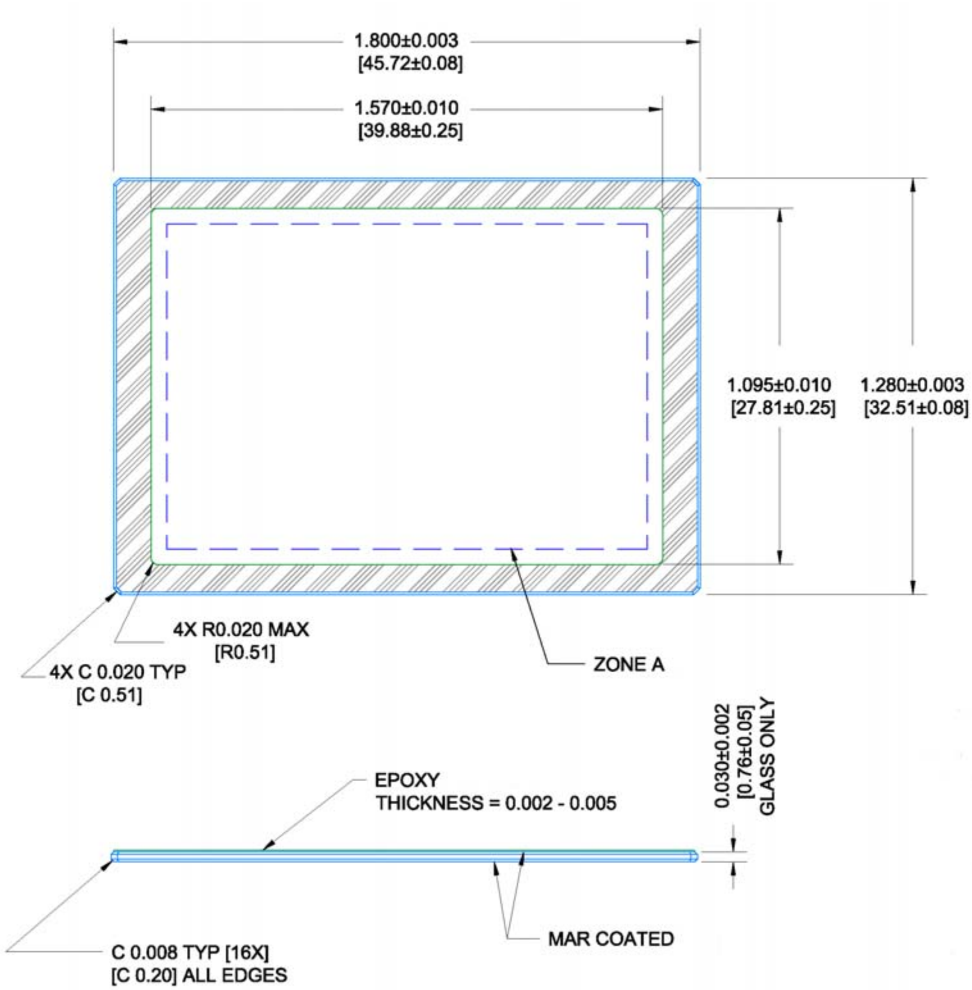



Notes:

1. Units IN [MM]

**Figure 28. Completed Assembly (2 of 2)**

## Cover Glass




Notes:

1. Substrate = Schott D263T eco
2. Dust, Scratch, Inclusion Specification:
   a.) 20 μm Max size in Zone A
   b.) Zone A = 1.474 x 1.000 [16.43 x 10.08] Centered
3. MAR coated both sides
4. Spectral Transmission
   a.) 350 − 365 nm: T ≥ 88%
   b.) 365 − 405 nm: T ≥ 94%
   c.) 405 − 450 nm: T ≥ 98%
   d.) 450 − 650 nm: T ≥ 99%
   e.) 650 − 690 nm: T ≥ 98%
   f.) 690 − 770 nm: T ≥ 94%
   g.) 770 − 870 nm: T ≥ 88%
5. Units: IN [MM]

**Figure 29. Cover Glass**

## Cover Glass Transmission

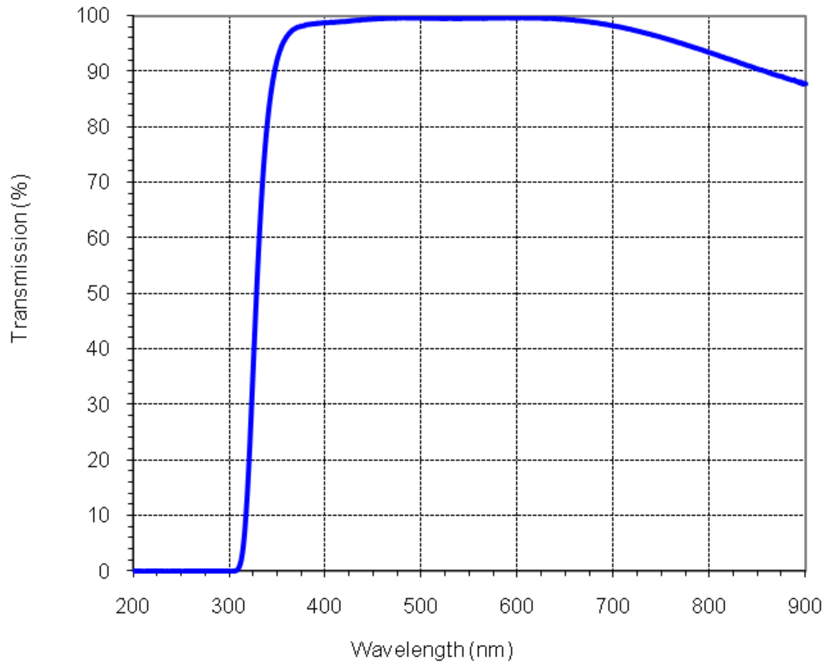



**Figure 30. Cover Glass Transmission**



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