

BUK6E2R0-30C

N-channel TrenchMOS intermediate level FET Rev. 02 — 7 September 2010

Product data sheet

1. **Product profile**

1.1 General description

Intermediate level gate drive N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using advanced TrenchMOS technology. This product has been designed and qualified to the appropriate AEC Q101 standard for use in high performance automotive applications.

1.2 Features and benefits

- AEC Q101 compliant
- Suitable for intermediate level gate drive sources
- Suitable for thermally demanding environments due to 175 °C rating

1.3 Applications

- 12 V Automotive systems
- Electric and electro-hydraulic power steering
- Motors, lamps and solenoid control
- Start-Stop micro-hybrid applications
- Transmission control
- Ultra high performance power switching

1.4 Quick reference data

Table 1. **Quick reference data**

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
V_{DS}	drain-source voltage	$T_j \ge 25 ^{\circ}\text{C}; T_j \le 175 ^{\circ}\text{C}$		-	-	30	V
I _D	drain current	$V_{GS} = 10 \text{ V}; T_{mb} = 25 \text{ °C};$ see Figure 1	[1]	-	-	120	Α
P _{tot}	total power dissipation	T _{mb} = 25 °C; see <u>Figure 2</u>		-	-	306	W
Static chara	acteristics						
R _{DSon}	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A};$ $T_j = 25 \text{ °C}; \text{ see } \frac{\text{Figure 16}}{\text{ of } 100 \text{ m}}$		-	1.9	2.2	mΩ
Avalanche ruggedness							
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I_D = 120 A; $V_{sup} \le 30$ V; R_{GS} = 50 Ω ; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; unclamped		-	-	1.7	J

^[1] Continuous current is limited by package.



2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		
2	D	Drain	mb	D
3	S	source		G (EX)
mb	D	mounting base; connected to drain	1 2 3	mbb076 S
			SOT226 (I2PAK)	

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK6E2R0-30C	I2PAK	plastic single-ended package (I2PAK); TO-262	SOT226

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4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 175 °C		-	30	V
V_{GS}	gate-source voltage		[1][2]	-16	16	V
			[3][4]	-20	20	V
I _D	drain current	$T_{mb} = 25 \text{ °C}; V_{GS} = 10 \text{ V}; \text{ see } \frac{\text{Figure 1}}{\text{Model}}$	<u>[5]</u>	-	120	Α
		$T_{mb} = 100 ^{\circ}C; V_{GS} = 10 V; see \underline{Figure 1}$	<u>[5]</u>	-	120	Α
I _{DM}	peak drain current	T_{mb} = 25 °C; t_p ≤ 10 μs; pulsed; see <u>Figure 3</u>		-	1082	Α
P _{tot}	total power dissipation	T _{mb} = 25 °C; see <u>Figure 2</u>		-	306	W
T _{stg}	storage temperature			-55	175	°C
Tj	junction temperature			-55	175	°C
Source-drain	diode					
Is	source current	T _{mb} = 25 °C	<u>[5]</u>	-	120	Α
I _{SM}	peak source current	$t_p \le 10 \ \mu s$; pulsed; $T_{mb} = 25 \ ^{\circ}C$		-	1082	Α
Avalanche rug	ggedness					
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I_D = 120 A; $V_{sup} \le$ 30 V; R_{GS} = 50 Ω ; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; unclamped		-	1.7	J
E _{DS(AL)R}	repetitive drain-source avalanche energy		[6][7][8]	-	-	J

^[1] DC

^{[2] -16}V accumulated duration not to exceed 168 hrs.

^[3] Pulsed

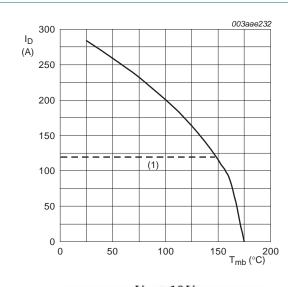
^[4] Accumulated pulse duration not to exceed 5mins.

^[5] Continuous current is limited by package.

^[6] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.

^[7] Repetitive avalanche rating limited by an average junction temperature of 170 °C.

^[8] Refer to application note AN10273 for further information.



 $V_{\rm GS} \geq 10\,V \label{eq:VGS}$ (1) Capped at 120 A due to package.

Fig 1. Continuous drain current as a function of mounting base temperature

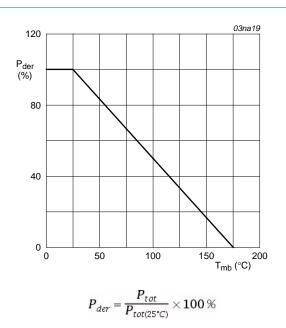
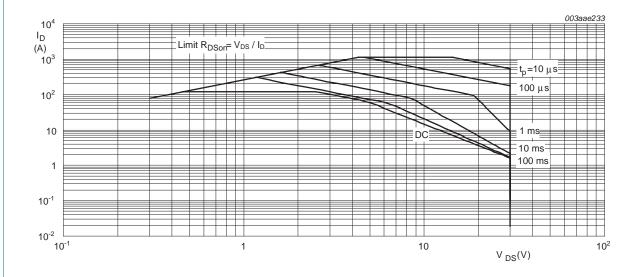


Fig 2. Normalized total power dissipation as a function of mounting base temperature



 $T_{mb} = 25 \,^{\circ}C$; I_{DM} is single pulse

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

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5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 4	-	-	0.49	K/W
R _{th(j-a)}	thermal resistance from junction to ambient	vertical in free air	-	50	-	K/W

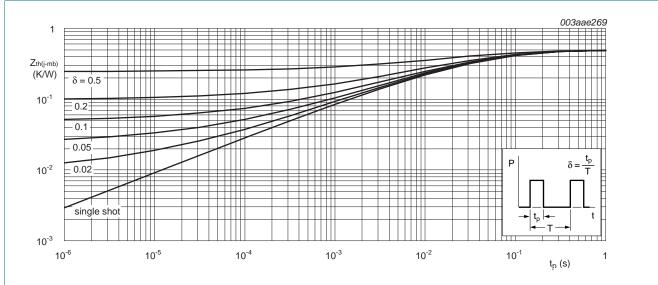


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

6. Characteristics

Table 6. Characteristics

Table 6.	Characteristics					
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static cha	aracteristics					
V _{(BR)DSS}	drain-source	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 °C$	30	-	-	V
	breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 °C$	27	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}$; $V_{DS} = V_{GS}$; $T_j = 25 \text{ °C}$; see <u>Figure 9</u> ; see <u>Figure 10</u>	1.8	2.3	2.8	V
		I_D = 1 mA; V_{DS} = V_{GS} ; T_j = -55 °C; see <u>Figure 10</u>	-	-	3.3	V
		I_D = 2.5 mA; V_{DS} = V_{GS} ; T_j = 175 °C; see <u>Figure 10</u>	0.8	-	-	V
I _{DSS}	drain leakage current	$V_{DS} = 30 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 \text{ °C}$	-	-	500	μΑ
		$V_{DS} = 30 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	0.02	1	μΑ
I _{GSS}	gate leakage current	$V_{DS} = 0 \text{ V}; V_{GS} = 20 \text{ V}; T_j = 25 \text{ °C}$	-	2	100	nΑ
		$V_{DS} = 0 \text{ V}; V_{GS} = -20 \text{ V}; T_j = 25 \text{ °C}$	-	2	100	nΑ
R _{DSon} drain-source on- resistance	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 ^{\circ}\text{C};$ see <u>Figure 16</u>	-	1.9	2.2	mΩ
		$V_{GS} = 5 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ °C};$ see Figure 16	-	2.3	3	mΩ
		$V_{GS} = 4.5 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ °C};$ see <u>Figure 16</u>	-	2.6	3.7	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 175 °C; see <u>Figure 11</u> ; see <u>Figure 16</u>	-	3.4	4.2	mΩ
Dynamic	characteristics					
$Q_{G(tot)}$	total gate charge	$I_D = 25 \text{ A}$; $V_{DS} = 24 \text{ V}$; $V_{GS} = 5 \text{ V}$; see <u>Figure 12</u> ; see <u>Figure 13</u>	-	131	-	nC
		$I_D = 25 \text{ A}; V_{DS} = 24 \text{ V}; V_{GS} = 10 \text{ V};$	-	229	-	nC
Q_{GS}	gate-source charge	see Figure 12; see Figure 13	-	38	-	nC
Q_{GD}	gate-drain charge		-	63	-	nC
C _{iss}	input capacitance	$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}; f = 1 \text{ MHz};$	-	11223	14964	pF
C _{oss}	output capacitance	T _j = 25 °C; see <u>Figure 14</u>	-	1780	2136	pF
C _{rss}	reverse transfer capacitance		-	1085	1486	pF
t _{d(on)}	turn-on delay time	$V_{DS} = 25 \text{ V}; R_L = 1 \Omega; V_{GS} = 10 \text{ V};$	-	53	-	ns
t _r	rise time	$R_{G(ext)} = 10 \Omega$	-	114	-	ns
t _{d(off)}	turn-off delay time		-	363	-	ns
t _f	fall time		-	192	-	ns
L _D	internal drain inductance	from drain lead 6 mm from package to centre of die ; $T_i = 25 ^{\circ}\text{C}$	-	4.5	-	nΗ
L _S	internal source inductance	from source lead to source bond pad ; $T_j = 25 ^{\circ}\text{C}$	-	7.5	-	nΗ

Table 6. Characteristics ... continued

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Source-drai	in diode					
V _{SD}	source-drain voltage	$I_S = 25 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 ^{\circ}\text{C};$ see <u>Figure 15</u>	-	0.8	1.2	V
t _{rr}	reverse recovery time	$I_S = 20 \text{ A}$; $dI_S/dt = -100 \text{ A/}\mu\text{s}$; $V_{GS} = 0 \text{ V}$;	-	70	-	ns
Q _r	recovered charge	$V_{DS} = 25 \text{ V}$	-	138	-	nC

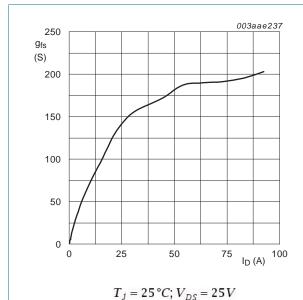


Fig 5. Forward transconductance as a function of drain current; typical values

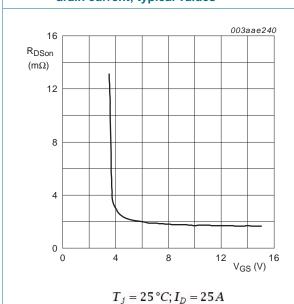
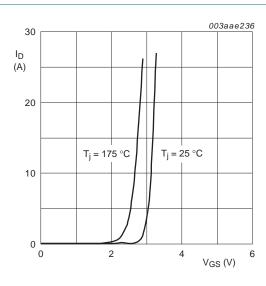
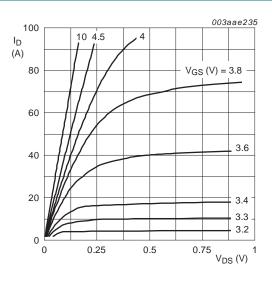


Fig 7. Drain-source on-state resistance as a function of gate-source voltage; typical values



 $V_{DS} > I_D \times R_{DSon}$

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values



 $T_j = 25\,^{\circ}C$

Fig 8. Output characteristics: drain current as a function of drain-source voltage; typical values

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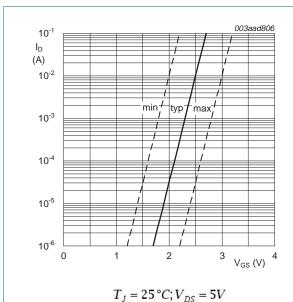


Fig 9. Sub-threshold drain current as a function of gate-source voltage

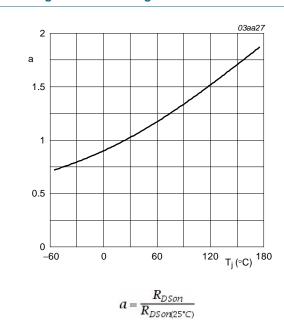


Fig 11. Normalized drain-source on-state resistance factor as a function of junction temperature

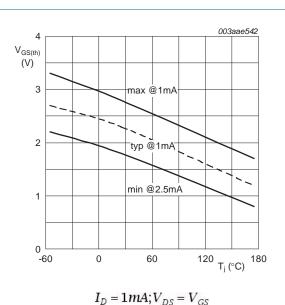


Fig 10. Gate-source threshold voltage as a function of junction temperature

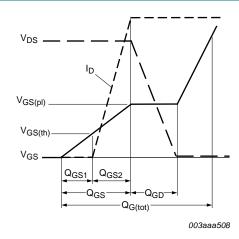


Fig 12. Gate charge waveform definitions

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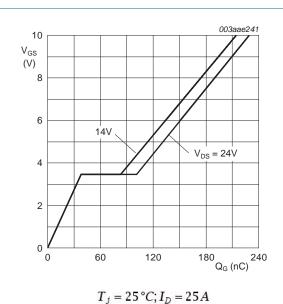
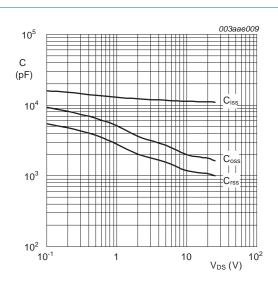


Fig 13. Gate-source voltage as a function of gate charge; typical values



 $V_{GS} = 0 V; f = 1 MHz$

Fig 14. Input, output and reverse transfer capacitance as a function of drain-source voltage; typical values

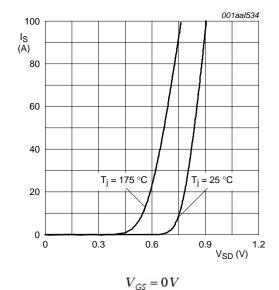
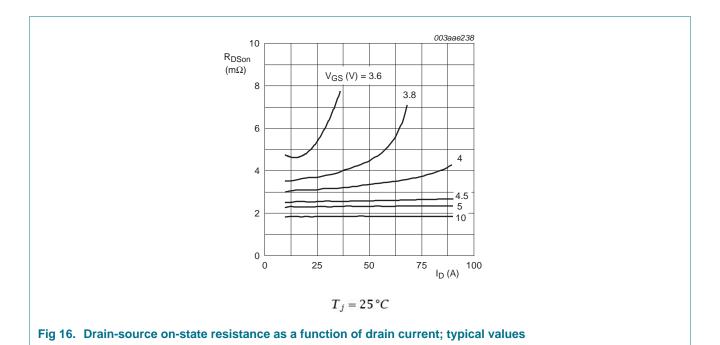


Fig 15. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

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7. Package outline

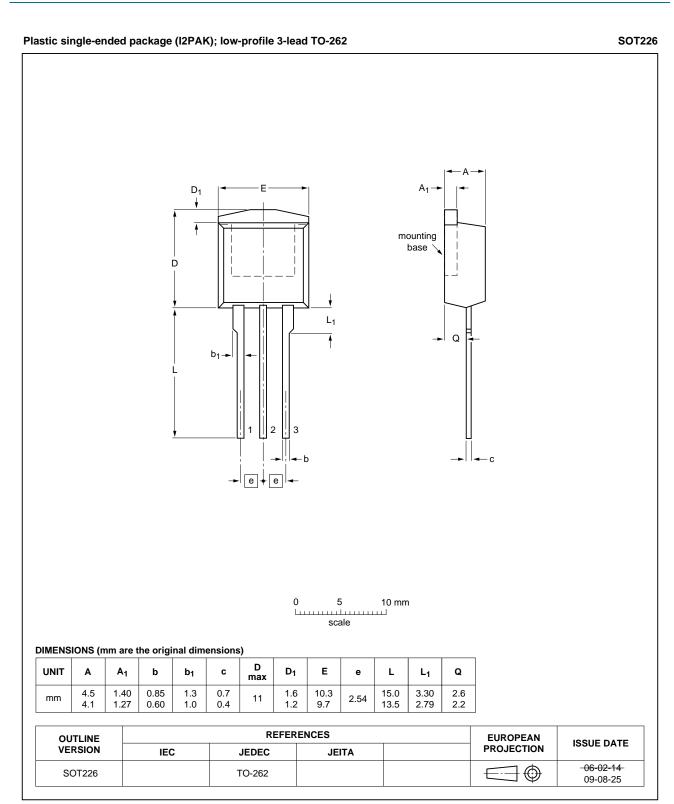


Fig 17. Package outline SOT226 (I2PAK)

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8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BUK6E2R0-30C v.2	20100907	Product data sheet	-	BUK6E2R0-30C v.1
Modifications:	 Various change 	es to content.		
BUK6E2R0-30C v.1	20100824	Product data sheet	-	-

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9. Legal information

9.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
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Nexperia

N-channel TrenchMOS intermediate level FET

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