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May 2007

74F240, 74F244 Octal Buffers/Line Drivers with 3-STATE Outputs

Features

- 3-STATE outputs drive bus lines or buffer memory address registers
- Outputs sink 64mA (48mA mil)
- 12mA source current
- Input clamp diodes limit high-speed termination effects

General Description

The 74F240 and 74F244 are octal buffers and line drivers designed to be employed as memory and address drivers, clock drivers and bus-oriented transmitters/ receivers which provide improved PC and board density.

Order Code	Package Number	Package Description
74F240SC ⁽¹⁾	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74F240SJ ⁽¹⁾	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74F240PC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
74F244SC ⁽¹⁾	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74F244SJ ⁽¹⁾	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74F244MSA ⁽¹⁾	MSA20	20-Lead Shrink Small Outline Package (SSOP), JEDEC MO-150, 5.3mm Wide
74F244PC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Ordering Information

Note:

1. Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering number.

Connection Diagrams



74F244



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Truth Tables

 $\overline{O}_0 - \overline{O}_7, O_0 - O_7$

Pin Names

 $\overline{OE}_1, \overline{OE}_2$

 OE_2

 $|_{0} - |_{7}$

 $|_{0} - |_{7}$

Note:

OE ₁	D _{1n}	O _{1n}	OE ₂	D _{2n}	O _{2n}
Н	Х	Z	Н	Х	Z
L	Н	L	L	Н	L
L	L	Н	L	L	Н

Inputs (74F240)

Inputs (74F244)

Outputs

2. Worst-case 74F240 enabled; 74F244 disabled.

Description

3-STATE Output Enable Input (Active LOW)

3-STATE Output Enable Input (Active HIGH)

H = HIGH Voltage Level L = LOW Voltage Level

X = Immaterial

Z = High Impedance

74F244

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\overline{OE}_1	D _{1n}	O _{1n}	\overline{OE}_2	D _{2n}	O _{2n}
Н	Х	Z	Н	Х	Z
L	Н	Н	L	Н	Н
L	L	L	L	L	L

U.L.

HIGH/LOW

1.0 / 1.667

1.0 / 1.667

1.0 / 1.667⁽²⁾

1.0 / 2.667⁽²⁾

600 / 106.6 (80)





Input I_{IH} / I_{IL}, Output I_{OH} / I_{OL}

20µA / -1mA

20µA / -1mA

20µA / -1mA

20µA / -1.6mA

-12mA / 64mA (48mA)

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
T _{STG}	Storage Temperature	–65°C to +150°C
T _A	Ambient Temperature Under Bias	–55°C to +125°C
TJ	Junction Temperature Under Bias	–55°C to +150°C
V _{CC}	V _{CC} Pin Potential to Ground Pin	-0.5V to +7.0V
V _{IN}	Input Voltage ⁽³⁾	-0.5V to +7.0V
I _{IN}	Input Current ⁽³⁾	-30mA to +5.0mA
Vo	Voltage Applied to Output in HIGH State (with V _{CC} = 0V)	
	Standard Output	–0.5V to V _{CC}
	3-STATE Output	–0.5V to 5.5V
	Current Applied to Output in LOW State (Max.)	twice the rated I _{OL} (mA)
	ESD Last Passing Voltage (Min.)	4000V

Note:

3. Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating
T _A	Free Air Ambient Temperature	0°C to +70°C
V _{CC}	Supply Voltage	+4.5V to +5.5V

DC Elec	C Electrical Characteristics								
Symbol	Paramete	r	V _{CC}	Conditions	Min.	Тур.	Max.	Units	
V _{IH}	Input HIGH Voltage			Recognized as a HIGH Sig- nal	2.0			V	
V _{IL}	Input LOW Voltage			Recognized as a LOW Sig- nal			0.8	V	
V _{CD}	Input Clamp Diode Voltage		Min.	I _{IN} = -18mA			-1.2	V	
V _{OH}	Output HIGH Voltage	10% V _{CC}	Min.	I _{OH} = -3mA	2.4			V	
		10% V _{CC}		I _{OH} = -15mA	2.0				
		5% V _{CC}		I _{OH} = -3mA	2.7				
V _{OL}	Output LOW Voltage	10% V _{CC}	Min.	$I_{OL} = 64 \text{mA}$			0.55	V	
I _{IH}	Input HIGH Current	•	Max.	V _{IN} = 2.7V			5.0	μA	
I _{BVI}	Input HIGH Current Breakdown Test		Max.	V _{IN} = 7.0V			7.0	μA	
I _{CEX}	Output HIGH Leakage	Current	Max.	V _{OUT} = V _{CC}			50	μA	
V _{ID}	Input Leakage Test		0.0	I _{ID} = 1.9μA	4.75			V	
				All Other Pins Grounded					
I _{OD}	Output Leakage Circuit Current		0.0	V _{IOD} = 150mV			3.75	μA	
				All Other Pins Grounded					
IIL	Input LOW Current		Max.	$V_{IN} = 0.5V (\overline{OE}_1, \overline{OE}_2, OE_2, D_n (74F240))$			-1.0	mA	
				V _{IN} = 0.5V (D _n (74F244))			-1.6		
I _{OZH}	Output Leakage Curre	nt	Max.	$V_{OUT} = 2.7V$			50	μA	
I _{OZL}	Output Leakage Curre	nt	Max.	$V_{OUT} = 0.5V$			-50	μA	
I _{OS}	Output Short-Circuit C	urrent	Max.	$V_{OUT} = 0V$	-100		-225	mA	
I _{ZZ}	Bus Drainage Test		0.0V	V _{OUT} = 5.25V			500	μA	
I _{CCH}	Power Supply Current (74F240)		Max.	V _O = HIGH		19	29	mA	
I _{CCL}	Power Supply Current (74F240)		Max.	$V_0 = LOW$		50	75	mA	
I _{CCZ}	Power Supply Current (74F240)		Max.	V _O = HIGH Z		42	63	mA	
I _{CCH}	Power Supply Current (74F244)		Max.	V _O = HIGH		40	60	mA	
I _{CCL}	Power Supply Current	(74F244)	Max.	V _O = LOW		60	90	mA	
I _{CCZ}	Power Supply Current (74F244)		Max.	V _O = HIGH Z		60	90	mA	

		$\label{eq:transform} \begin{array}{l} T_A = +25^\circ C,\\ V_{CC} = +5.0V,\\ C_L = 50 pF \end{array}$				$ \begin{array}{c} T_{A}=0^{\circ}C \text{ to }+70^{\circ}C,\\ V_{CC}=5.0V,\\ C_{L}=50pF \end{array} \end{array} $			
Symbol	Parameter	Min.	Тур.	Max.	Min.	Max.	Min.	Max.	Units
t _{PLH} , t _{PHL}	Propagation Delay	3.0	5.1	7.0	3.0	9.0	3.0	8.0	ns
Data to Output (74F240)	2.0	3.5	4.7	2.0	6.0	2.0	5.7		
t _{PZH} , t _{PZL}	t _{PZH} , t _{PZL} Output Enable Time (74F240)	2.0	3.5	4.7	2.0	6.5	2.0	5.7	ns
		4.0	6.9	9.0	4.0	10.5	4.0	10.0	1
t _{PHZ} , t _{PLZ}	Output Disable Time	2.0	4.0	5.3	2.0	6.5	2.0	6.3	
	(74F240)	2.0	6.0	8.0	2.0	12.5	2.0	9.5	
t _{PLH} , t _{PHL}	Propagation Delay,	2.5	4.0	5.2	2.0	6.5	2.5	6.2	ns
Data to Output (74F244)	2.5	4.0	5.2	2.0	7.0	2.5	6.5		
t _{PZH} , t _{PZL} Output Enable Time (74F244)	2.0	4.3	5.7	2.0	7.0	2.0	6.7	ns	
	(74F244)	2.0	5.4	7.0	2.0	8.5	2.0	8.0	1
t _{PHZ} , t _{PLZ}	Output Disable Time	2.0	4.5	6.0	2.0	7.0	2.0	7.0]
	(74F244)		4.5	6.0	2.0	7.5	2.0	7.0]







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