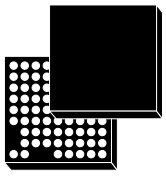
STA8090WG

Fully Integrated GPS/Galileo/Glonass/QZSS receiver with embedded RF

Datasheet - preliminary data



WLCSP77

GAPG1305150801PS

Features

- STMicroelectronics positioning receiver with 48 tracking channels and 2 fast acquisition channels supporting GPS, Galileo, GLONASS, BeiDou and QZSS systems
- Single die standalone receiver embedding RF Front-End and low noise amplifier
- -162 dBm indoor sensitivity (tracking mode)
- Fast TTFF < 1 s in Hot start and 30 s in Cold Start
- High performance ARM946 MCU (up to 196 MHz)
- 256 Kbyte embedded SRAM
- External SQI Flash interface
- 8 free running timers/ counters (32 bit)
- Real Time Clock (RTC) circuit
- 32-bit Watch-dog timer
- 3 UARTs
- 1 I^2C master interface
- 1 Synchronous Serial Port (SSP, Motorola-SPI supported)
- USB2.0 full speed (12 MHz) with integrated physical layer transceiver
- 1 Controller Area Network (CAN) (STA8090WGBD only)
- Power Management Unit (PMU) embedding switching regulator
- Operating condition:
  - Main voltage regulator (V_{INL}): 1.6 V to 4.3 V
  - Backup voltage (V_{INB}): 1.6 V to 4.3 V
  - Digital voltage (V_{DD}): 1.0 V to 1.32 V
  - RF core voltage (V_{CC}): 1.2 V ± 10%
  - IO Ring Voltage (V_{ddIO}): 1.8 V ± 5% or 3.3 V ± 10%
- Package:
  - WLCSP77 (3.861 x 3.843 x 0.6 mm) 0.4 pitch
- Packing in Tape and Reel
- Operating temperature range: -40/ +85 °C

Description

STA8090WG belongs to Teseo III family products.

STA8090WG is a single die standalone positioning receiver which embeds the new ST GNSS positioning engine capable of receiving signals from multiple satellite navigation systems, including GPS, Galileo, Glonass, BeiDou QZSS.

The minimum BOM and small WLCSP package make STA8090WG the ideal solution for low-cost and small footprint products such hand-held computers, cameras, data loggers, and sports accessories.

The device is offered with a complete GNSS firmware which performs all GNSS operations including tracking, acquisition, navigation and data output.

Table 1. Device summary

Root Part Number	Package	Packaging
STA8090WG	WLCSP77 3.861 x 3.843 mm	Tape and Reel

Contents

List of tables

List of figures

1 Overview

STA8090WG is one of the part number of Teseo III STA8090x series.

STA8090WG is a highly integrated System-On-Chip GNSS receiver designed for high-flexible and cost effective solution addressing hand-held, in-dash navigation and Telematics applications.

STA8090WG embeds the new ST GNSS positioning engine capable of receiving signals from multiple satellite navigation systems, including the US GPS, European Galileo, Russia's GLONASS, Chinese BeiDou and Japan's QZSS.

The STA8090WG ability of tracking simultaneously the signals from multiple satellites regardless of their constellation, make this chip capable of delivering exceptional accuracy in urban canyons and in the environments where buildings and other obstructions make satellite visibility challenging.

STA8090WG embeds innovative power management unit with switching regulator for power consumption optimization.

The extended voltage supply range from 1.6 V to 4.3 V, the 1.8 V and 3.3 V I/O compliance support make the STA8090WG the suitable solution for different user applications.

The STA8090WG combines a high performance ARM946 microprocessor with I/O capabilities and enhanced peripherals.

It supports USB2.0 standard at full speed (12 Mbps) with on-chip PHY.

The chip embeds backup logic with real time clock.

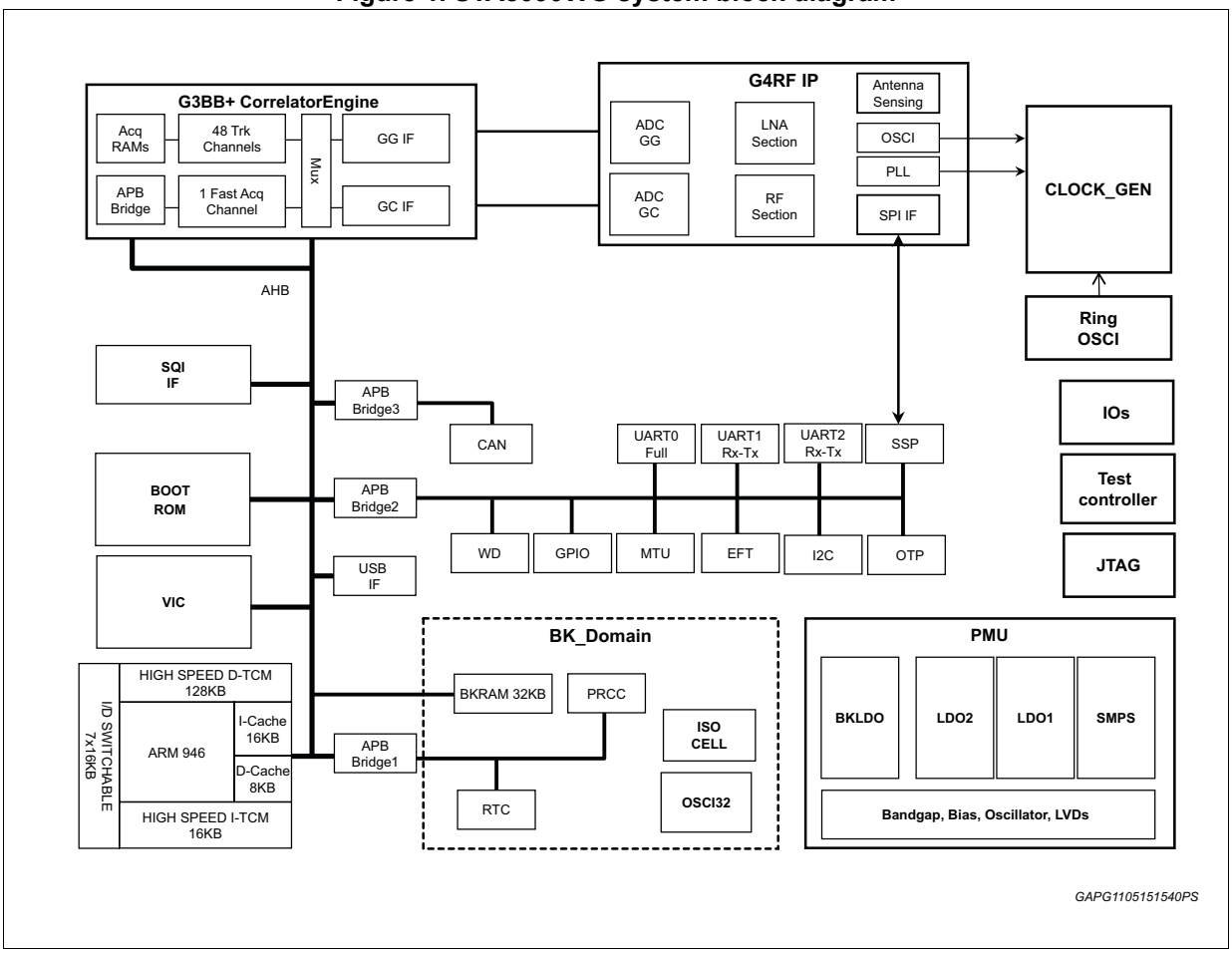
STA8090WGBD can be offered also bundled with STMicroelectronics dead reckoning firmware called TESEO-DRAW; TESEO-DRAW firmware is a multi-sensors data fusion hub for Teseo family IC’s.

The STA8090WG, using STMicroelectronics CMOSRF Technology, is housed in a WLCSP77 (3.861 x 3.843 x 0.6 mm) 0.4 pitch with a Tape and Reel packing.

2 Pin description

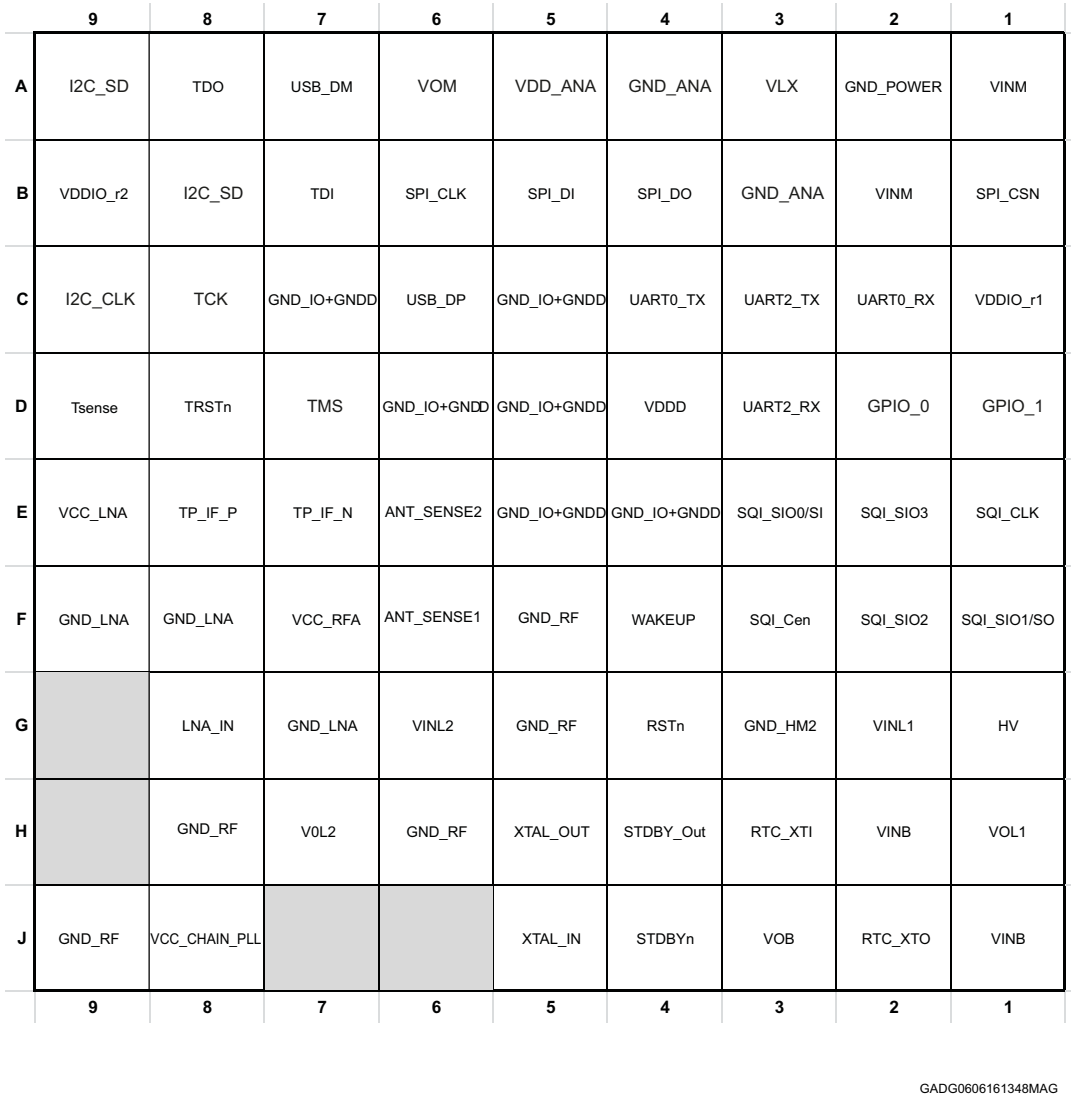
2.1 Block diagram

Figure 1. STA8090WG system block diagram



2.2 WLCSP 77 ball out

Figure 2. WLCSP 77 ball out diagram (bottom view)



2.3 Power supply pins

Table 2. Power supply pins

Name	I/O voltage	I/O	Description	Pin #
VCC_CHAIN_PLL	1.2 V	PWR	Analog supply voltage for RF chain and PLL (1.2 V)	J8
VCC_RFA	1.2 V	PWR	Analog supply voltage for RF (1.2 V)	F7
VCC_LNA	1.2 V	PWR	Analog supply voltage for LNA (1.2 V)	E9

Table 2. Power supply pins (continued)

Name	I/O voltage	I/O	Description	Pin #
VDDD	1.2 V	PWR	Digital supply voltage	D4
VDDIO_r1	1.8 V or 3.3 V	PWR	Digital supply voltage for I/O ring 1 (1.8 V or 3.3V)	C1
VDDIO_r2	3.3 V	PWR	Digital supply voltage for I/O ring 2 (3.3 V)	B9
VINB	1.6 V - 4.3 V	PWR	Backup LDO input supply voltage (1.6 V to 4.3 V)	H2, J1
VINL1	1.6 V - 4.3 V	PWR	LDO1 input supply voltage (1.6 V to 4.3 V)	G2
VINL2	1.6 V - 4.3 V	PWR	LDO2 input supply voltage (1.6 V to 4.3 V)	G6
VINM	1.6 V - 4.3 V	PWR	SMPS coil input supply (1.6 V to 4.3 V)	A1, B2
VDD_ANA	1.6 V - 4.3 V	PWR	SMPS input supply (1.6 V to 4.3 V)	A5
VLX	0 V - 4.3 V	PWR	SMPS coil output	A3
VOB	1.0 V	PWR	LDO backup output voltage (1.0 V)	J3
VOL1	1.2 V or 1.8 V	PWR	LDO1 output voltage (1.8 V)	H1
VOL2	1.2 V	PWR	LDO2 output voltage (1.2 V)	H7
VOM	1.2 V or 1.8 V	PWR	SMPS output voltage (1.2 V)	A6
GND_RF	GND	GND	Ground	F5, G5, H8, H6, J9
GND_LNA	GND	GND	Ground	F9, F8, G7
GND_IO+GNDD	GND	GND	Ground	C5, C7, D5, D6, E4, E5
GND_ANA	GND	GND	Ground	A4, B3
GND_POWER	GND	GND	Ground	A2
GND_HM2	GND	GND	Ground	G3

2.4 Main function pins

Table 3. Main function pins

Name	I/O voltage	I/O	Description	Pin #
RSTn	1.0 V	I	Reset Input with Schmitt-Trigger characteristics and noise filter.	G4
RTC_XTI	1.0 V (max)	I	Input of the 32 KHz oscillator amplifier circuit and input of the internal real time clock circuit.	H3
RTC_XTO	1.0 V (max)	O	Output of the oscillator amplifier circuit.	J2
STDBY_OUT	1.0 V	O	When low, indicates the chip is in Standby mode	H4
STDBYn	1.0 V	I	When low, the chip is forced in Standby Mode - All pins in high impedance except the ones powered by Backup supply	J4
WAKEUP	1.0 V	I	WAKEUP from STANDBY mode	F4

2.5 Test / emulated dedicated pins

Table 4. Test/emulated dedicated pins

Name	I/O voltage	I/O	Description	Pin #
TCK	VDDIO_R2	I	JTAG Test Clock	C8
TDI	VDDIO_R2	I	JTAG Test Data In	B7
TDO	VDDIO_R2	O	JTAG Test Data Out	A8
TMS	VDDIO_R2	I	JTAG Test Mode Select	D7
TRSTn	VDDIO_R2	I	JTAG Test Circuit Reset	D8
TP_IF_N	1.2 V	O	Diff.Test Point for IF — Neg.	E7
TP_IF_P	1.2 V	O	Diff.Test Point for IF — Pos.	E8

2.6 SQI pins

Table 5. SQI pins

Name	I/O voltage	I/O	Description	Pin #
SQI_Cen	VDD_SQI	O	SQI Flash chip enable / IO_Power Sel Ring SQI	F3
SQI_CLK	VDD_SQI	O	SQI Flash clock	E1
SQI_SIO0/SI	VDD_SQI	I/O	SQI Flash data IO 0 / ser. I	E3
SQI_SIO1/SO	VDD_SQI	I/O	SQI Flash data IO 1 / ser. O	F1
SQI_SIO2	VDD_SQI	I/O	SQI Flash data IO 2	F2
SQI_SIO3	VDD_SQI	I/O	SQI Flash data IO 3	E2

2.7 Communication interface pins

Table 6. Communication interface pins

Name	I/O voltage	I/O	Alternative function	Function	Description	Pin #
I2C_CLK	VDDIO_R2	O	AF0 (default)	I2C_CLK	I2C clock	C9
		I/O	AF1	GPIO8	General purpose I/O #8	
		O	AF2	CAN1_TX(1)	CAN1 transmit data output	
		O	AF3	SPI_CLK	SPI clock	
I2C_SD	VDDIO_R2	I/O	AF0 (default)	MMC_D0	Multimedia card data 0	A9, B8
		I/O	AF1	i2s_out_sclk	MSP serial clock output	
		I	AF2	I2C_SD	I2C serial data	
		I/O	AF3	GPIO20	General purpose I/O #20	
SPI_CLK	VDDIO_R1	O	AF0 (default)	SPI_CLK	SPI clock	B6
		I/O	AF1	GPIO25	General purpose I/O #25	
		O	AF2	SQI_CLK	SQI Flash clock	
		O	AF3	MMC_CLK	Multimedia Clock line	
SPI_CSN	VDDIO_R1	O	AF0 (default)	SPI_CSN	SPI chip select active low / IO_Power Sel Ring 1	B1
		I/O	AF1	GPIO24	General purpose I/O #24	
		I/O	AF2	SQI_CEN	SQI Flash chip enable	
		I/O	AF3	MMC_CMD	Multimedia card command line	
SPI_DI	VDDIO_R1	I	AF0 (default)	SPI_DI	SPI serial data input / BOOT2	B5
		I/O	AF1	Tsense	External temperature capture port	
		I/O	AF2	SQI_SIO1/SO	SQI Flash data IO 1 / ser. 0	
		I/O	AF3	MMC_D0	Multimedia card data 0	
SPI_DO	VDDIO_R1	O	AF0 (default)	SPI_DO	SPI serial data output	B4
		I/O	AF1	GPIO27	General purpose I/O #27	
		I/O	AF2	SQI_SIO0/SI	SQI Flash data IO 0 / ser. 1	
		I/O	AF3	MMC_D1	Multimedia card data 1	
Tsense	VDDIO_R2	I	AF0 (default)	Reserved	Reserved	D9
		I	AF1	Reserved	Reserved	
		I	AF2	Reserved	Reserved	
		I	AF3	Tsense	External temperature capture port	

Table 6. Communication interface pins (continued)

Name	I/O voltage	I/O	Alternative function	Function	Description	Pin #
UART0_RX	VDDIO_R1	I	AF0 (default)	UART0_RX	UART0 Rx data	C2
		O	AF1	SPI_DO	SPI serial data output	
		I/O	AF2	SQI_SIO2	SQI Flash data IO 2	
		I	AF3	Timer_ICAPA	Extended Function Timer - Input Capture A	
UART0_TX	VDDIO_R1	O	AF0 (default)	UART0_TX	UART0 Tx data / BOOT1	C4
		I	AF1	SPI_DI	SPI serial data input	
		I/O	AF2	SQI_SIO3	SQI Flash data IO 3	
		O	AF3	Timer_OCMPA	Extended Function Timer – Output Compare A	
UART2_RX	VDDIO_R1	I	AF0 (default)	UART2_RX	UART 2 Rx data	D3
		I/O	AF1	GPIO28	General purpose I/O #28	
		I/O	AF2	I2C_SD	I2C serial data	
		I/O	AF3	Reserved	Reserved	
UART2_TX	VDDIO_R1	O	AF0 (default)	UART2_TX	UART 2 Tx data / BOOT0	C3
		I/O	AF1	GPIO29	General purpose I/O #29	
		O	AF2	I2C_CLK	I2C clock	
		I/O	AF3	Reserved	Reserved	
USB_DM	VDDIO_R2	USB	AF0	USB_DM	USB D- signal	A7
		I	AF1 (default)	UART1_RX	UART1 Rx data	
		I	AF2	CAN1_RX(1)	CAN1 receive data input	
		I/O	AF3	I2C_SD	I2C serial data	
USB_DP	VDDIO_R2	USB	AF0	USB_DP	USB D+ signal	C6
		O	AF1 (default)	UART1_TX	UART1 Tx data	
		O	AF2	CAN1_TX(1)	CAN1 transmit data output	
		O	AF3	I2C_CLK	I2C clock	

1. Only for STA8090WGBD.

2.8 General purpose pins

Table 7. General purpose pins

Name	I/O voltage	I/O	Alternative function	Function	Description	Pin #
GPIO0	VDDIO_R1	I/O	AF0 (default)	GPIO0	General purpose I/O #0	D2
		I	AF1	PPS_IN	Pulse per second input	
		O	AF2	Timer_OCMPB	Extended Function Timer – Output Compare B	
		O	AF3	Mag_0 GC	GLONASS and BeiDou 3-bit coding Output (MAG0)	
GPIO1	VDDIO_R1	I/O	AF0 (default)	GPIO1	General purpose I/O #1 / BOOT3	D1
		I	AF1	Reserved	Reserved	
		O	AF2	PPS_OUT	Pulse per second output	
		I/O	AF3	Tsense	External temperature capture port	

2.9 RF front-end pins

Table 8. RF front-end pins

Name	I/O voltage	I/O	Description	Pin #
LNA_IN	1.2 V	I	Low Noise Amplifier Input	G8
XTAL_IN	1.2 V	I	Input Side of Crystal Oscillator or TCXO Input	J5
XTAL_OUT	1.2 V	O	Output Side of Crystal Oscillator	H5

3 General description

3.1 RF front end

The RF front-end is able to down-convert both the GPS-Galileo signal from 1575.42 MHz to 4.092 MHz (4 Fo, being F0 = 1.023 MHz), the GLONASS signal from 1601.718 MHz to 8.57 MHz and the BeiDou signal from 1561.098 MHz to 10.23 MHz.

It embeds high performance LNA minimizing external component count and a LDO to supply the internal core facilitating requirements for external power supply. A three bits ADC converts the IF signals to sign (SIGN) and magnitude (MAG0 and MAG1). They can be sampled or not by SPI. The magnitude bits are internally integrated in order to control the variable gain amplifiers. The VGA gain can be also set by the SPI interface.

The RF tuner accepts a wide range of reference clocks (10 to 52 MHz) and can generate 64 Fo sampling clock for the baseband and 192 Fo clock for MCU subsystem.

3.2 GPS/Galileo/GLONASS/BeiDou Base Band (G3BB+) processor

STA8090WG integrates G3BB+ proprietary IP, which is the ST last generation high-sensitivity Baseband processor fully compliant with GPS, Galileo, GLONASS and BeiDou systems.

The baseband receives, from the embedded RF Front-End, two separate IF signals coded in sign-magnitude digital format on 3 bits and the related clocks. The Galileo/GPS (GALGPS) and GLONASS/BeiDou (GNSCOM) signals at the base band inputs are centered on 4.092 MHz, 8.57 MHz and 10.23 MHz.

The baseband processes the two IF signals performing data codification, sample rate conversion and final frequency conversion to zero IF before acquisition and tracking correlations.

The baseband processor has the capability of acquiring and tracking the Galileo, GPS, GLONASS and BeiDou signals in a simultaneous or single way, or a combination of three, being GLONASS and BeiDou mutually exclusive. The number of tracking channels to be used is programmable; the not used tracking channels can be powered down.

A complete multi-OS software library is provided by ST to handle GPS processing, managing satellite acquisition, tracking, pseudo-range calculation and positioning, generating the output in the standard NMEA message format or in a ST binary format. The library includes support of ST self-trained assisted GPS (ST-AGPS), a complete and scalable solution for assisting GPS start-up with autonomous and server-based ephemeris prediction and extension.

3.3 MCU Subsystem

The implemented sub-system includes an AHB Lite bus matrix.

An ARM946 core is embedded in the sub-system and masters the AHB bus. The totally available TCM SRAM is 256 KB. The amount of memory on ITCM and DTCM can be

configured by the ARM946 (see *Table 9: TCM Configuration*). ITCM can be configured as Ni x 16 KB; DTCM can be configured as 128 + Nd x 16 KB, where Ni + Nd = 8, Ni ≥ 1.

Table 9. TCM Configuration

TCMcfg [2]	TCMcfg [1]	TCMcfg [0]	ITCM	DTCM
0	0	0	16 KB	240 KB
0	0	1	32 KB	224 KB
0	1	0	48 KB	208 KB
0	1	1	64 KB	192 KB
1	0	0	80 KB	176 KB
1	0	1	96 KB	160 KB
1	1	0	112 KB	144 KB
1	1	1	128 KB	128 KB

3.3.1 AHB slaves

- G3 APB port that allows to interface with the G3BB acquisition memory and control registers
- 512 Kbytes ROM
- Vectored Interrupt Controller (VIC)
- SQI flash memory controller
- 3 x ARM946 APB peripheral bus (APB1, APB2, APB3)

Vectored Interrupt Controller (VIC)

This Vectored Interrupt Controller (VIC) allows the operative system interrupt handler to quickly dispatch interrupt service routines in response to peripheral interrupts. It provides a software interface to the interrupt system. There are up to 64 interrupt lines. The VIC uses a bit position for each different interrupt source.

The software can control each request line to generate software interrupts. Each interrupt line can be independently enabled and configured to trigger a non-vectored Normal Interrupt Request (IRQ) or Fast Interrupt Request (FIQ) to the ARM946 CPU. Sixteen interrupt lines can also be selected to trigger a vectored IRQ.

The VIC has two operation modes: the user mode and the privilege mode, in order to have the possibility to set (or not) one level of protection during execution.

FS USB device controller

Full speed USB device with transceiver. It is an AHB slave. When active requires a 48 MHz clock XTAL_IN.

SQI Flash interface

STA8090WG includes a high-performance interface to Serial Quad Interface (SQI) NOR Flash chips, to support a low-cost simple implementation.

3.4 APB peripherals

3.4.1 EFT

The Extended Function Timer (EFT) consists of a 16-bit counter driven by a programmable prescaler.

It may be used for a variety of purposes, including pulse length measurement of up to two input signals (input capture), generation of up to two output waveforms (output compare) and one PWM generation. Pulse lengths and waveform periods can be modulated from a very wide range using the timer prescaler.

EFT features

- Programmable prescaler: f_{APB} divided from 1 to 256, prescaler register (0 to 255) value +1.
- Overflow status flag and maskable interrupts.
- Output compare functions with:
  - 2 dedicated 16-bit registers
  - 2 dedicated programmable signals
  - 2 dedicated status flags
  - 2 dedicated interrupt flags
- Input capture functions with:
  - 2 dedicated 16-bit registers
  - 2 dedicated active edge selection signals
  - 2 dedicated status flags
  - 2 dedicated interrupt flags
- Pulse Width Modulation mode (PWM).
- One Pulse Mode (OPM).
- PWM input mode.
- Timer global interrupt (5 internally ORed)
  - ICIA: timer input capture A interrupt
  - ICIB: timer input capture B interrupt
  - OCIA: timer output compare A interrupt
  - OCIB: timer output compare B interrupt
  - TOI: timer overflow interrupt

3.4.2 SSP

The SSP is a master interface for synchronous serial communication with peripheral devices that have Motorola SPI.

The SSP performs serial-to-parallel conversion on data received from a peripheral device on SPI_DI pin, and parallel-to-serial conversion on data written by CPU for transmission on SPI_DO pin. The transmit and receive paths are buffered with internal FIFO memories allowing up to 32 x 32-bit values to be stored independently in both transmit and receive modes. FIFOs may be burst-loaded or emptied by the system processor or DMA, from one to eight words per transfer. Each 32-bit word from the system fills one entry in FIFO.

The SSP includes a programmable bit rate clock divider and prescaler to generate the serial output clock SSPCLK from the on-chip clock. One combined interrupt is delivered, which is asserted from several internal maskable events.

SSP features

The SSP has the following features:

- Parallel-to-serial conversion on data written to an internal 32-bit wide, 32-location deep
- transmit FIFO
- Serial-to-parallel conversion on received data, buffering it in a 32-bit wide, 32-location
- deep receive FIFO
- Programmable data frame size from 4 to 32 bits
- Programmable clock bit rate and prescaler
- Programmable clock phase and polarity in SPI mode

3.4.3 UART

The UARTx (x = 0|1|2) performs serial-to-parallel conversion on data asynchronously received from a peripheral device on UARTx_RX pin, and parallel-to-serial conversion on data written by CPU for transmission on UARTx_TX pin. The transmit and receive paths are buffered with internal FIFO memories allowing up to 64 data byte for transmission, and 64 data byte with 4-bit status (break, frame, parity, and overrun) for receive.

UART features

The UARTx (x = 0|1|2) are Universal Asynchronous Receiver/Transmitter that support much of the functionality of the industry-standard 16C650 UART. The main features are:

- Programmable baud rates up to UARTCLK / 16 (1.5 Mbps with UARTCLK at 24 MHz), or up to UARTCLK / 8 (3.0 Mbps with UARTCLK at 24 MHz), with fractional baud-rate generator
- 5, 6, 7 or 8 bits of data
- Even, odd, stick or no-parity bit generation and detection
- 1 or 2 stop bit generation
- Support of software flow control using programmable Xon/Xoff characters
- False start bit detection
- Line break generation and detection
- Separate 8-bit wide, 64-deep transmit FIFO and 12-bit wide, 64-deep receive FIFO
- Programmable FIFO disabling for 1-byte depth data path

These UARTs vary from industry-standard 16C650 on some minor points which are:

- Receive FIFO trigger levels
- The internal register map address space, and the bit function of each register differ
- The deltas of the modem status signals are not available
- 1.5 stop bits is not supported
- Independent receive clock feature is not supported

3.4.4 I2C

STA8090WG includes an I2C interface configurable as master or slave.

3.4.5 MTU

The 2 Multi Timer Units provide access to eight interrupt generating programmable 32-bit Free-Running decrementing Counters (FRCs). The FRCs have their own clock input, allowing the counters to run from a much slower clock than the system clock.

The FRC is the part of the timer that performs the counting. There are four instantiations of the FRC block in each MTU, allowing eight counts to be performed in parallel. The 32-bit counter in the FRC is split up into two 16-bit counters.

3.4.6 WDT

Watchdog Timer (WDT) provides a way of recovering from software crashes. The watchdog clock is used to generate a regular interrupt (WDOGINT), depending on a programmed value.

The watchdog monitors the interrupt and asserts a reset signal (WDOGRES) if the interrupt remains unserviced for the entire programmed period. You can enable or disable the watchdog unit as required.

Note: Watchdog is stalled when the ARM processor is in Debug mode.

3.4.7 GPIO

The GPIO block provides Twelve (12) programmable inputs or outputs. Each input or output can be controlled in two modes:

- software mode through an APB bus interface
- alternate mode, where GPIO becomes a peripheral input or output line

Any GPIO input can be independently enabled or disabled (masked) for interrupt generation. User can select for each GPIO which edge (rising, falling, both) will trigger an interrupt.

3.4.8 RTC

This is an always-on power domain dedicated to RTC logic (backup system) with 32 Kbyte SRAM and supplied with a dedicated voltage regulator.

The RTC provides a high resolution clock which can be used for GPS. It keeps the time when the system is inactive and can be used to wake the system up when a programmed alarm time is reached. It has a clock trimming feature to compensate for the accuracy of the 32.768 kHz crystal and a secured time update.

RTC features

- 47-bit counter clocked by 32.768 kHz clock
- 32-bit for the integer part (seconds) and 15-bit for the fractional part
- The integer part and the fractional part are readable independently
- The counter, once enabled, can be stopped
- Integer part load register (32-bit)
- Fractional part load register (15-bit)
- Load bit to transfer the content of the entire load register (integer+fractional part) to the 47-bit counter. Once set by the MCU this bits is cleared by the hardware to signal to the MCU that the RTC has been updated.

3.4.9 CAN (only in STA8090WGBD)

The CAN core performs communication according to the CAN protocol version 2.0 part A and B. The bit rate can be programmed to values up to 1 MBit/s. For the connection to the physical layer, additional transceiver hardware is required.

CAN consists of the CAN core, message RAM, message handler, control registers and module. For communication on a CAN network, individual message objects are configured. The message objects and identifier masks for acceptance filtering of received messages are stored in the message RAM. All functions concerning the handling of messages are implemented in the message handler. These functions include acceptance filtering, the transfer of messages between the CAN core and the message RAM, and the handling of transmission requests as well as the generation of the module interrupt.

The register set of the CAN can be accessed directly by the CPU through the module interface. These registers are used to control/configure the CAN core and the message handler and to access the message RAM.

CAN features

- Supports CAN protocol version 2.0 part A and B
- 32 messages objects
- Each message object has its own identifier mask
- Maskable interrupt
- Disabled automatic re-transmission mode for time triggered CAN applications
- Programmable loop-back mode for self-test operation.

4 Electrical characteristics

4.1 Parameter conditions

Unless otherwise specified, all voltages are referred to GND.

4.2 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25°C.

4.3 Typical values

Unless otherwise specified, typical data are based on T_A = 25°C, V_{ddio} = 1.8 V, V_{dd} = 1.20 V. They are given only as design guidelines and are not tested.

4.4 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

4.5 Absolute maximum ratings

This product contains devices to protect the inputs against damage due to high static voltages, however it is advisable to take normal precautions to avoid application of any voltage higher than the specified maximum rated voltages.

Table 10 lists the absolute maximum rating for STA8090WG.

Table 10. Voltage characteristics

Symbol	Parameter	Min.	Max.	Unit
V_{CC_CHAIN}	Analog supply voltage for RF chain (1.2 V)	-0.3	1.32	V
V_{CC_PLL}	Analog supply voltage for PLL RF (1.2 V)	-0.3	1.32	V
V_{CC_RF}	Analog supply voltage for RF (1.2 V)	-0.3	1.32	V
V_{DD_SQI}	Digital supply voltage for SQI	-0.3	3.63	V
V_{DDD}	Power supply pins for the core logic.	-0.3	1.32	V
V_{DDIO_R1}	Digital supply voltage for I/O ring 1 (1.8 V or 3.3 V)	-0.3	3.63	V
V_{DDIO_R2}	Digital supply voltage for I/O ring 2 (3.3 V)	-0.3	3.63	V
V_{INB}	Backup LDO input supply voltage (1.6 V to 4.3 V)	-0.3	4.8	V
V_{INL1}	LDO1 input supply voltage (1.6 V to 4.3 V)	-0.3	4.8	V
V_{INL2}	LDO2 input supply voltage (1.6 V to 4.3 V)	-0.3	4.8	V

Table 10. Voltage characteristics (continued)

Symbol	Parameter	Min.	Max.	Unit
V_{INM}	SMPS coil input supply (1.6 V to 4.3 V)	-0.3	4.8	V
V_{DD_ANA}	SMPS input supply (1.6 V to 4.3 V)	-0.3	4.8	V
$V_{ESD\text{-}HBM}$(1)	Electrostatic discharge, human body model.	-2	+2	KV
$V_{ESD\text{-}CDM}$	Electrostatic discharge, charge device model.	-150	+150	V

1. Balls sustaining only ±500 V are A1, A2, A3,A4, A5, A6, B2, B3, G1, G2, G3, H1, H2, H4, H7, H8, J1, J2 and J3.

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 11. Thermal characteristics

Symbol	Parameter	Min.	Max.	Unit
T_{oper}	Operative temperature range	-40	85	°C
T_j	Operative junction temperature	-40	125	°C
T_{stg}	Storage temperature	-40	125	°C
$R_{j\text{-}amb}$	Thermal resistance junction to ambient(1)	TBD	TBD	°C/W

1. According to JEDEC specification on a 2 layers board.

Table 12. Frequency limits

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
F_{CLK}	Operating ARM9 CPU frequency	V_{DDD} = 1.2 V; T_C = 85 °C(1)	–	–	196	MHz
F_{AHB}	AHB frequency		–	–	49	MHz

1. Not tested in production.

Table 13. Power consumption

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
P_{RF}	RFIP power (total V_{INL2})	G2 = GPS/Galileo; T_{amb} = 25 °C; V_{INL2} = 1.8 V	–	35	–	mW
		G2 + GLONASS; T_{amb} = 25 °C; V_{INL2} = 1.8 V	–	35	–	mW
		G2 + BeiDou; T_{amb} = 25 °C; V_{INL2} = 1.8 V	–	35	–	mW

Table 13. Power consumption (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
P_{MVR}	Switchable area power; (total V_{INL1})	f_{ARM} = 196 MHz; f_{AHB} = 49 MHz; T_{amb} = 25 °C; V_{INL1} = 1.8 V; UART active; other peripherals inactive	–	90	–	mW
P_{LPVR}	Always ON area power (total V_{INB})	f_{ARM} = 196 MHz; f_{AHB} = 49 MHz; T_{amb} = 25 °C; V_{INB} = 3.3 V	–	1	–	mW
P_{IO}	IO rings power (total V_{DDIO_R1} + V_{DDIO_R2})	f_{ARM} = 196 MHz; f_{AHB} = 49 MHz; T_{amb} = 25 °C; V_{INL1} = 1.8 V; UART active; other peripherals inactive	–	4	–	mW
$I_{DStandby}$	Standby mode supply current	RTC running = 32.768 KHz; T_{amb} = 25 °C; V_{INB} = 1.8 V	—	29	—	µA
$I_{DDeepStandby}$	Deep standby mode supply current(1)		—	7	—	µA

1. STDBY_OUT pin not supported in deep standby.

4.6 Recommended DC operating conditions

Table 14 lists the functional recommended operating DC parameters for STA8090WG.

Table 14. Recommended DC operating conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC_CHAIN}	Analog supply voltage for RF chain (1.2 V)	1.08	1.20	1.32	V
V_{CC_PLL}	Analog supply voltage for PLL RF (1.2 V)	1.08	1.20	1.32	V
V_{CC_RF}	Analog supply voltage for RF (1.2 V)	1.08	1.20	1.32	V
V_{DD_SQI}	Digital supply voltage for SQI I/O ring (1.8 V)	1.71	1.80	1.89	V
	Digital supply voltage for SQI I/O ring (3.3 V)	3.00	3.30	3.60	V
V_{DDD}	Power supply pins for the core logic.	1.00	1.10	1.32	V
V_{DDIO_R1}	Digital supply voltage for I/O ring 1 (1.8 V)	1.71	1.80	1.89	V
	Digital supply voltage for I/O ring 1 (3.3 V)	3.00	3.30	3.60	V
V_{DDIO_R2}	Digital supply voltage for I/O ring 2 (3.3 V)	3.00	3.30	3.60	V
V_{INB}	Backup LDO input supply voltage (1.6 V to 4.3 V)	1.60	–	4.30	V
V_{INL1}	LDO1 input supply voltage to generate 1.8 V	2.10	–	4.30	V
V_{INL2}	LDO2 input supply voltage to generate 1.2 V	1.60	–	4.30	V
V_{INM}	SMPS coil input supply voltage to generate 1.1 V	2.10	–	4.30	V

Table 14. Recommended DC operating conditions (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD_ANA}	SMPS input supply (1.6 V to 4.3 V)	1.60	–	4.30	V
T_C	Operating temperature range	-40	–	85	°C

4.7 DC characteristics

Table 15 specifies the SMPS voltage regulator characteristics.

Table 15. SMPS DC characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{OM}	Output voltage (1.2 V)	1.6 V ≤ V_{INM} ≤ 4.3 V; I_{OM} ≤ 100 mA	1.08	1.20	1.32	V
	Output voltage (1.1 V)	1.6 V ≤ V_{INM} ≤ 4.3 V; I_{OM} ≤ 100 mA	1.0	1.10	1.2	V
I_{OM}	Output current	–	0	–	100	mA

Table 16 specifies the LDO1 voltage regulator characteristics.

Table 16. LDO1 DC characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{OL1}	Output voltage (1.8V)	2.1 V ≤ V_{INL1} ≤ 4.3 V; I_{OL1} ≤ 70 mA	1.71	1.80	1.89	V
I_{OL1}	Output current	–	0	–	70	mA

Table 17 specifies the LDO2 voltage regulator characteristics.

Table 17. LDO2 DC characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{OL2}	Output voltage	1.6 V ≤ V_{INL2} ≤ 4.3 V; I_{OL2} ≤ 30 mA	1.08	1.20	1.32	V
I_{OL2}	Output current	–	0	–	30	mA

Table 18 specifies the low voltage detection thresholds

Table 18. Low voltage detection thresholds

Parameter		Min.	Typ.	Max.	Unit
Input LVD always on and main VRs(1)	Upper voltage threshold	–	1.680	–	V
	Lower voltage threshold	–	1.650	–	V
Output LVD always on VR(1)	Upper voltage threshold	–	0.995	–	V
	Lower voltage threshold	–	0.935	–	V

Table 18. Low voltage detection thresholds (continued)

Parameter		Min.	Typ.	Max.	Unit
Output LVD main VR (1.1 or 1.2 V)(1)	Upper voltage threshold @ V_{OM} = 1.2 V	–	1.142	–	V
	Lower voltage threshold @ V_{OM} = 1.2 V	–	1.076	–	V
	Upper voltage threshold @ V_{OM} = 1.1 V	–	0.930	–	V
	Lower voltage threshold @ V_{OM} = 1.1 V	–	0.900	–	V
Output LVD main VR (1.8 V)(1)	Upper voltage threshold @ V_{OL1} = 1.8 V	–	1.645	–	V
	Lower voltage threshold @ V_{OL1} = 1.8 V	–	1.626	–	V

1. By design.

Table 19 lists the DC characteristics for all the IO digital buffers expect for the following input buffers: STBYn (J4), STDBY_OUT (H4), WAKEUP (F4) and RSTn (G4).

Table 19. I/O buffers DC characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}(1)	Logical input low level voltage	V_{DDIO} = 1.8 V	-0.3	–	0.3 * V_{DDIO}	V
		V_{DDIO} = 3.3V	-0.3	–	0.8	V
V_{IH}(1)	Logical input high level voltage	V_{DDIO} = 1.8 V	0.7 * V_{DDIO}	–	V_{DDIO} + 0.3	V
		V_{DDIO} = 3.3V	2.0	–	V_{DDIO} + 0.3	V
V_{HYST}(2)	Schmitt-trigger hysteresis	–	50	–	–	mV
V_{OL}	Low level output voltage	V_{DDIO} = 1.8 V	–	–	0.4	V
		V_{DDIO} = 3.3V	–	–	0.4	V
V_{OH}	High level output voltage	V_{DDIO} = 1.8 V	V_{DDIO} - 0.4	–	–	V
		V_{DDIO} = 3.3V	V_{DDIO} - 0.4	–	–	V

1. Excludes oscillator inputs RTC_XTI and XTAL_IN. Refer to oscillator electrical specifications.
2. Apply to all digital inputs unless specified otherwise.

Table 20 lists the DC characteristics for the 1.0 V IO digital buffers input buffers: STBYn (J4), STDBY_OUT (H4), WAKEUP (F4) and RSTn (G4).

Table 20. 1.0 V I/O buffers DC characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Logical input low level voltage	V_{OB} = 1.0 V	-0.3	–	0.35 * V_{OB}	V
V_{IH}	Logical input high level voltage	V_{OB} = 1.0 V	0.65 * V_{OB}	–	V_{OB} + 0.3	V
V_{OL}	Low level output voltage	V_{OB} = 1.0 V	–	–	0.2	V
V_{OH}	High level output voltage	V_{OB} = 1.0 V	V_{OB} - 0.2	–	–	V

4.8 AC characteristics

4.8.1 RF electrical specifications

Table 21. RFCHAIN – GALGPS filter and VGA

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
S11	Input return loss	GPS band	–	-8	–	dB
f_{IF}	IF frequency	PLL in default condition with 26Mhz as reference	–	4.045	–	MHz
NF	Noise figure	NF overall chain with AGC set at 0 dB	–	2(1)	–	dB
C_G	Conversion gain from RF input to ADC input	VGA at max gain	–	69	–	dB
		VGA at min gain	–	119	–	dB
IP_{1dB}	RF-IF-VGA input compression point	VGA min	–	-80	–	dBm
IRR	Image rejection ratio	–	–	20	–	dB
BW_{GPS}	-3dB IF bandwidth	GPS mode	–	2.4	–	MHz
BW_{GAL}		Galileo mode	–	4.8	–	MHz
ATT	Alias frequency rejection	F = 60 MHz (fs = 65.474 MHz)	–	30	–	dB
T_{gGPS}	IF filter group delay variation	GPS mode	–	–	200(1)	ns
T_{gGAL}		Galileo mode	–	–	30(1)	ns

1. Not tested in production.

Table 22. RFCHAIN – GLONASS/BeiDou filter and VGA

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
S11	Input return loss	GLONASS band	–	-10	–	dB
		BeiDou band	–	-7	–	
$f_{IFGNS/BDU}$	IF frequency for GLONASS	PLL in default condition with 26 Mhz as reference	–	8.519	–	MHz
	IF frequency for BeiDou		–	10.277	–	
NF	Noise figure	NF overall chain with AGC set at 0 dB	–	2(1)	–	dB
C_G	Conversion gain from RF input to ADC input	VGA at max gain	–	68	–	dB
		VGA at min gain	–	118	–	dB
IP_{1dB}	RF-IF-VGA input compression point	VGA min	–	-80	–	dBm
IRR	Image rejection ratio	–	–	25	–	dB

Table 22. RFCHAIN – GLONASS/BeiDou filter and VGA (continued)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$BW_{GNS/BDU}$	-3dB IF bandwidth	–	–	10	–	MHz
ATT	Alias frequency rejection	F = 53 MHz (fs = 65.474 MHz)	–	30	–	dB
$T_{gGNS/BDU}$	IF filter group delay variation	–	–	–	20(1)	ns

1. Not tested in production.

Table 23. Synthesizer

Symbol	Parameter	Min.	Typ.	Max.	Unit
F_{TCXO_XTAL}	Input frequency for xtal amplifier (1)	10	–	52	MHz
R_{DIV}	Reference divider range	1	–	63	–
N_{DIV}	Loop divider range	56	–	2047	–
F_{LO}	LO operating frequency	–	3142.656		MHz

1. That amplifier can be used also as a TCXO input buffer.

4.8.2 Oscillator electrical specifications

This device contains two oscillators:

- a 32.768 kHz oscillator/buffer for RTC circuit.
- an OSCI oscillator/buffer in the RF Front-End

When used in oscillator mode, each oscillator requires a specific crystal, with parameters that must be as close as possible to the following recommended values. When used in input buffer mode, an external clock source must be applied.

32.768 kHz OSCI32 oscillator specifications

The 32.768 kHz OSCI32 oscillator is connected between RTC_XTI (oscillator amplifier input) and RTC_XTO (oscillator amplifier output). It also requires two external capacitors of 18 pF(a), as shown on *Figure 3*.

OSCI32 is disabled by default and must be enabled by setting bit28-OSCI_EN of PRCC_BACKUP_REG0 to have 32.768KHz oscillation when an XTAL pi-network is connected to RTC_XTI/RTC_XTO pins.

The recommended oscillator specifications are shown in *Table 24*:

Table 24. Crystal recommended specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
F_{SXTAL}	Crystal frequency(1)	–	32.768	–	kHz
LM_{SXTAL}	Motion inductance(1)	–	5	–	kH

a. Using crystal with recommended characteristics as per *Table 24*.

Table 24. Crystal recommended specifications (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
CM_{SXTAL}	Motional capacitance(1)	–	5.0	–	fF
CO_{SXTAL}	Shunt capacitance(1)	–	1.3	–	pF
ESR	Resonance resistance(1)	–	–	80	kΩ
CL	External load capacitance(1)	–	18	–	pF

1. Not tested in production.

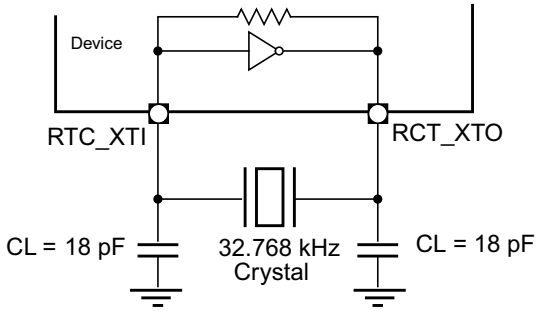
The oscillator amplifier specifications are shown in the following table:

Table 25. Oscillator amplifier specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_S	Startup time(1)	0.2	0.3	0.6	s
DL	Drive level(1)	–	–	<0.1	µW
RLC	Required load capacitance(1)	–	12.5	–	pF
GM	Startup transconductance	22.5	33.6	–	µA/V

1. Not tested in production.

Figure 3. 32.768 kHz crystal connection



To drive the 32.768 kHz crystal pins from an external clock source:

- Disable the oscillator (bit28-OSCI_EN = 0b in PRCC_BACKUP_REG0 register). This disables the internal inverter, thus reducing the power consumption to minimum. This also allows to drive RTC_XTI input even when a crystal is connected between RTC_XTI and RTC_XTO pins.
- Drive the RTC_XTI pin with a square signal or a sine wave.

Table 26. Characteristics of external slow clock input

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_{JIT} (cc)	Cycle-to-cycle jitter	-70	–	70	ps
T_{JIT} (per)	Period jitter	-70	–	70	ps

Table 26. Characteristics of external slow clock input (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Variation	-500	–	500	ppm
T_{DUTY}	Duty cycle	45	–	55	%

4.8.3 OSCI oscillator specifications

Default supported values are 16.368 MHz, 24 MHz, 26 MHz and 48 MHz.

To enable USB peripheral the 48 MHz is mandatory

5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

5.1 WLCSP77 (3.861 x 3.843 x 0.6 mm) 0.4 pitch package information

Figure 4. WLCSP77 package outline

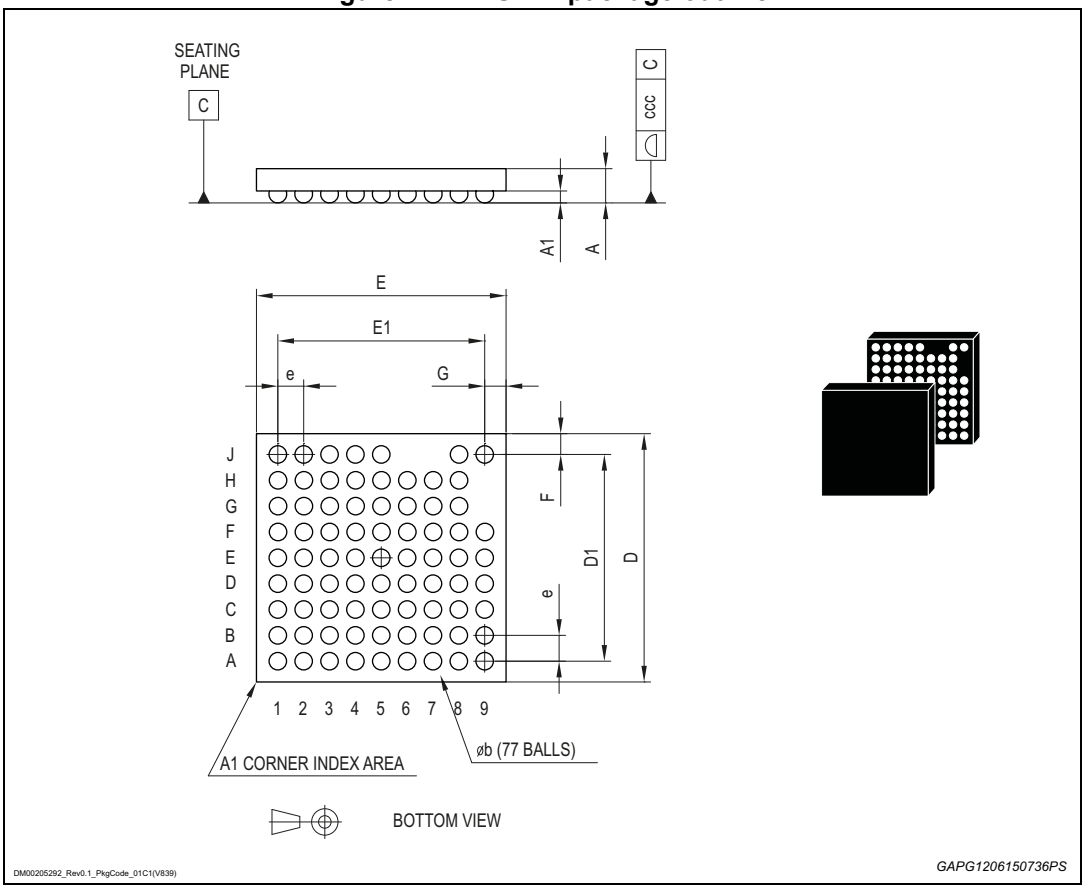


Table 27. WLCSP77 package mechanical data

Ref	Dimensions					
	Millimeters			Inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	–	–	0.600	–	–	0.0236
A1	0.165	–	–	0.0065	–	–

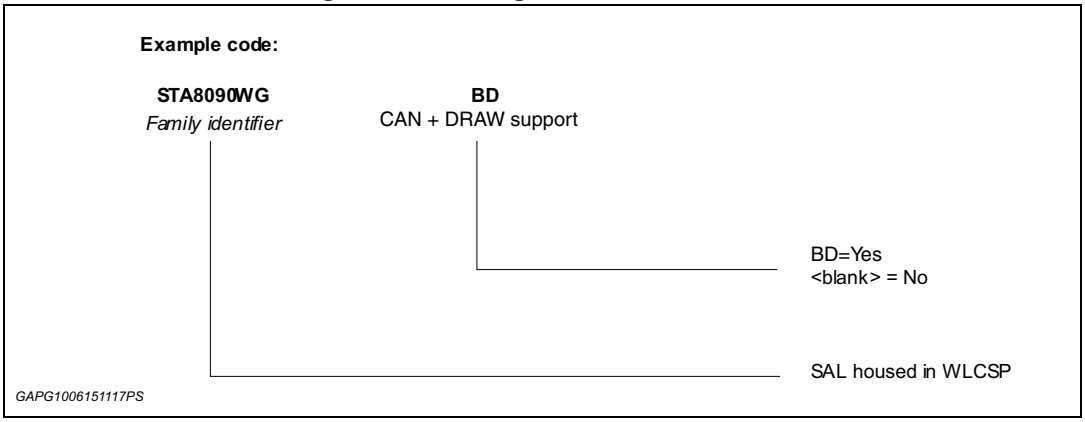
Table 27. WLCSP77 package mechanical data (continued)

Ref	Dimensions					
	Millimeters			Inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
b	0.245	0.275	0.305	0.0096	0.0108	0.0120
D	3.813	3.843	3.873	0.1501	0.1513	0.1525
D1	–	3.200	–	–	0.1260	–
E	3.831	3.861	3.891	0.1508	0.1520	0.1532
E1	–	3.200	–	–	0.1260	–
e	–	0.400	–	–	0.0157	–
F	–	0.321	–	–	0.0126	–
G	–	0.330	–	–	0.0130	–
ccc	–	–	0.050	–	–	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

6 Ordering information

Figure 5. Ordering information scheme



7 Revision history

Table 28. Document revision history

Date	Revision	Changes
22-Jun-2015	1	Initial release.
06-Jul-2016	2	Updated *Figure 1* and *Figure 2* Updated *Table 2* Changed note in *Table 6* Changed title in *Chapter 3.4.9* Updated *Table 13*, *Table 15*,*Table 16* and *Table 17* Changed title in *Table 21* and *Table 22* Updated *Figure 5: Ordering information scheme*
08-Nov-2016	3	Added packing information in cover page Updated in *Table 6* the description of I2C_SD Updated *Figure 5: Ordering information scheme*
09-Jun-2017	4	Updated: – *Table 10: Voltage characteristics*: values of '$V_{ESD-HBM}$ and $V_{ESD-CDM}$' parameters; – *Table 11: Thermal characteristics*: values of 'T_{stg}' parameter; – *Table 13: Power consumption*: removed 'I_{DSLEEP}' and added '$I_{DStandby}$ and $I_{DDeepStandby}$' parameters.
05-Jun-2020	5	Minor text changes.