

# MC74LCX14

## Low Voltage CMOS Hex Schmitt Inverter With 5 V-Tolerant Inputs

The MC74LCX14 is a high performance hex inverter with Schmitt-Trigger inputs operating from a 2.3 to 3.6 V supply. High impedance TTL compatible inputs significantly reduce current loading to input drivers, while TTL compatible outputs offer improved switching noise performance. A  $V_I$  specification of 5.5 V allows MC74LCX14 inputs to be safely driven from 5.0 V devices.

Pin configuration and function are the same as the MC74LCX04, but the inputs have hysteresis and, with its Schmitt trigger function, the LCX14 can be used as a line receiver which will receive slow input signals.

### Features

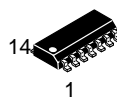
- Designed for 2.3 V to 3.6 V  $V_{CC}$  Operation
- 5.0 V Tolerant Inputs – Interface Capability with 5.0 V TTL Logic
- LVTTTL Compatible
- LVC MOS Compatible
- 24 mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current (10  $\mu$ A) Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 500 mA
- Current Drive Capability is 24 mA at Source/Sink
- Pin and Function Compatible with Other Standard Logic Families
- ESD Performance: Human Body Model >2000 V  
Machine Model >100 V
- Chip Complexity: 41 Equivalent Gates
- Pb-Free Packages are Available\*



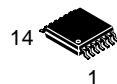
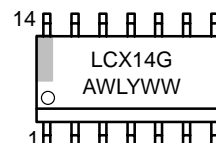
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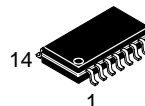
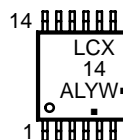
### MARKING DIAGRAMS



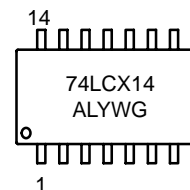
SOIC-14  
D SUFFIX  
CASE 751A



TSSOP-14  
DT SUFFIX  
CASE 948G



SOEIAJ-14  
M SUFFIX  
CASE 965



A = Assembly Location  
L, WL = Wafer Lot  
Y, YY = Year  
W, WW = Work Week  
G = Pb-Free Package  
▪ = Pb-Free Package  
(Note: Microdot may be in either location)

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# MC74LCX14

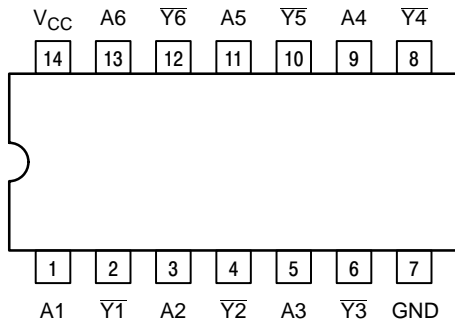


Figure 1. Pinout: 14-Lead (Top View)

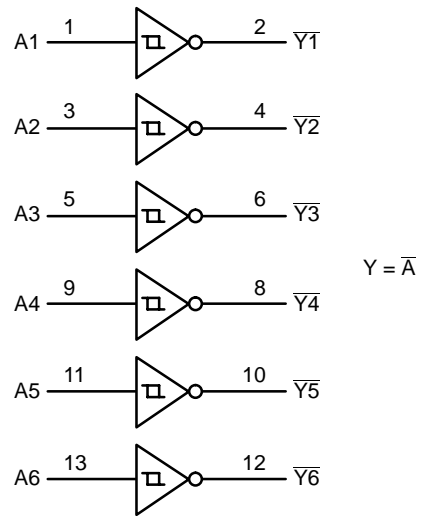


Figure 2. Logic Diagram

## PIN NAMES

Pins	Function
$A_n$	Data Inputs
$\overline{Y}_n$	Outputs

## TRUTH TABLE

Inputs	Outputs
A	$\overline{Y}$
L	H
H	L

## MAXIMUM RATINGS

Symbol	Parameter	Value	Condition	Unit
$V_{CC}$	DC Supply Voltage	-0.5 to +7.0		V
$V_I$	DC Input Voltage	$-0.5 \leq V_I \leq +7.0$		V
$V_O$	DC Output Voltage	$-0.5 \leq V_O \leq V_{CC} + 0.5$	Output in HIGH or LOW State. (Note 1)	V
$I_{IK}$	DC Input Diode Current	-50	$V_I < GND$	mA
$I_{OK}$	DC Output Diode Current	-50	$V_O < GND$	mA
		+50	$V_O > V_{CC}$	mA
$I_O$	DC Output Source/Sink Current	$\pm 50$		mA
$I_{CC}$	DC Supply Current Per Supply Pin	$\pm 100$		mA
$I_{GND}$	DC Ground Current Per Ground Pin	$\pm 100$		mA
$T_{STG}$	Storage Temperature Range	-65 to +150		$^{\circ}C$

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

- $I_O$  absolute maximum rating must be observed.

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## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V <sub>CC</sub>	Supply Voltage	Operating	2.5 to 3.3	3.6	V
		Data Retention Only		1.5	
V <sub>I</sub>	Input Voltage	0		5.5	V
V <sub>O</sub>	Output Voltage (HIGH or LOW State)	0		V <sub>CC</sub>	V
I <sub>OH</sub>	HIGH Level Output Current	V <sub>CC</sub> = 3.0 V–3.6 V		–24	mA
		V <sub>CC</sub> = 2.7 V–3.0 V		–12	
		V <sub>CC</sub> = 2.3 V–2.7 V		–8	
I <sub>OL</sub>	LOW Level Output Current	V <sub>CC</sub> = 3.0 V–3.6 V		+24	mA
		V <sub>CC</sub> = 2.7 V–3.0 V		+12	
		V <sub>CC</sub> = 2.3 V–2.7 V		+8	
T <sub>A</sub>	Operating Free–Air Temperature	–40		+85	°C

## DC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic	Condition	T <sub>A</sub> = –40 to 85°C		Unit
			Min	Max	
V <sub>T+</sub>	Positive Input Threshold Voltage (Figure 3)	V <sub>CC</sub> = 2.5 V V <sub>CC</sub> = 3.0 V	0.9 1.2	1.7 2.2	V
V <sub>T–</sub>	Negative Input Threshold Voltage (Figure 3)	V <sub>CC</sub> = 2.5 V V <sub>CC</sub> = 3.0 V	0.4 0.6	1.1 1.5	V
V <sub>H</sub>	Input Hysteresis Voltage (Figure 3)	V <sub>CC</sub> = 2.5 V V <sub>CC</sub> = 3.0 V	0.3 0.4	1.0 1.2	V
V <sub>OH</sub>	HIGH Level Output Voltage	2.3 V ≤ V <sub>CC</sub> ≤ 3.6 V; I <sub>OL</sub> = 100 μA	V <sub>CC</sub> – 0.2		V
		V <sub>CC</sub> = 2.3 V; I <sub>OH</sub> = –8 mA	1.8		
		V <sub>CC</sub> = 2.7 V; I <sub>OH</sub> = –12 mA	2.2		
		V <sub>CC</sub> = 3.0 V; I <sub>OH</sub> = –18 mA	2.4		
		V <sub>CC</sub> = 3.0 V; I <sub>OH</sub> = –24 mA	2.2		
V <sub>OL</sub>	LOW Level Output Voltage	2.3 V ≤ V <sub>CC</sub> ≤ 3.6 V; I <sub>OL</sub> = 100 μ		0.2	V
		V <sub>CC</sub> = 2.3 V; I <sub>OL</sub> = 8 mA		0.3	
		V <sub>CC</sub> = 2.7 V; I <sub>OL</sub> = 12 mA		0.4	
		V <sub>CC</sub> = 3.0 V; I <sub>OL</sub> = 16 mA		0.4	
		V <sub>CC</sub> = 3.0 V; I <sub>OL</sub> = 24 mA		0.55	
I <sub>I</sub>	Input Leakage Current	2.3 V ≤ V <sub>CC</sub> ≤ 3.6 V; 0 V ≤ V <sub>I</sub> ≤ 5.5 V		±5.0	μA
I <sub>CC</sub>	Quiescent Supply Current	2.3 ≤ V <sub>CC</sub> ≤ 3.6 V; V <sub>I</sub> = GND or V <sub>CC</sub>		10	μA
		2.3 ≤ V <sub>CC</sub> ≤ 3.6 V; 3.6 ≤ V <sub>I</sub> or V <sub>O</sub> ≤ 5.5 V		±10	
ΔI <sub>CC</sub>	Increase in I <sub>CC</sub> per Input	2.3 ≤ V <sub>CC</sub> ≤ 3.6 V; V <sub>IH</sub> = V <sub>CC</sub> – 0.6 V		500	μA

## AC ELECTRICAL CHARACTERISTICS (Input t<sub>r</sub> = t<sub>f</sub> = 2.5 ns)

Symbol	Parameter	Waveform	Limits						Unit
			T <sub>A</sub> = –40°C to +85°C						
			V <sub>CC</sub> = 3.3 V ± 0.3 V		V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 2.5 V ± 0.2 V		
			C <sub>L</sub> = 50 pF		C <sub>L</sub> = 50 pF		C <sub>L</sub> = 30 pF		
			Min	Max	Min	Max	Min	Max	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Input to Output	1	1.5 1.5	6.5 6.5	1.5 1.5	7.5 7.5	1.5 1.5	7.8 7.8	ns
t <sub>OSHL</sub> t <sub>OSLH</sub>	Output-to-Output Skew (Note 2)			1.0 1.0					ns

2. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t<sub>OSHL</sub>) or LOW-to-HIGH (t<sub>OSLH</sub>); parameter guaranteed by design.

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## DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Characteristic	Condition	$T_A = +25^\circ\text{C}$			Unit
			Min	Typ	Max	
$V_{OLP}$	Dynamic LOW Peak Voltage (Note 3)	$V_{CC} = 3.3\text{ V}, C_L = 50\text{ pF}, V_{IH} = 3.3\text{ V}, V_{IL} = 0\text{ V}$ $V_{CC} = 2.5\text{ V}, C_L = 30\text{ pF}, V_{IH} = 2.5\text{ V}, V_{IL} = 0\text{ V}$		0.8 0.6		V
$V_{OLV}$	Dynamic LOW Valley Voltage (Note 3)	$V_{CC} = 3.3\text{ V}, C_L = 50\text{ pF}, V_{IH} = 3.3\text{ V}, V_{IL} = 0\text{ V}$ $V_{CC} = 2.5\text{ V}, C_L = 30\text{ pF}, V_{IH} = 2.5\text{ V}, V_{IL} = 0\text{ V}$		-0.8 -0.6		V

3. Number of outputs defined as "n". Measured with "n-1" outputs switching from HIGH-to-LOW or LOW-to-HIGH. The remaining output is measured in the LOW state.

## CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Unit
$C_{IN}$	Input Capacitance	$V_{CC} = 3.3\text{ V}, V_I = 0\text{ V or } V_{CC}$	7	pF
$C_{OUT}$	Output Capacitance	$V_{CC} = 3.3\text{ V}, V_I = 0\text{ V or } V_{CC}$	8	pF
$C_{PD}$	Power Dissipation Capacitance	10 MHz, $V_{CC} = 3.3\text{ V}, V_I = 0\text{ V or } V_{CC}$	25	pF

## ORDERING INFORMATION

Device	Package	Shipping†
MC74LCX14D	SOIC-14	55 Units / Rail
MC74LCX14DG	SOIC-14 (Pb-Free)	55 Units / Rail
MC74LCX14DR2	SOIC-14	2500 Tape & Reel
MC74LCX14DR2G	SOIC-14 (Pb-Free)	2500 Tape & Reel
MC74LCX14DT	TSSOP-14*	96 Units / Rail
MC74LCX14DTG	TSSOP-14*	96 Units / Rail
MC74LCX14DTR2	TSSOP-14*	2500 Tape & Reel
MC74LCX14DTR2G	TSSOP-14*	2500 Tape & Reel
MC74LCX14M	SOEIAJ-14	50 Units / Rail
MC74LCX14MG	SOEIAJ-14 (Pb-Free)	50 Units / Rail
MC74LCX14MEL	SOEIAJ-14	2000 Tape & Reel
MC74LCX14MELG	SOEIAJ-14 (Pb-Free)	2000 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*This package is inherently Pb-Free.

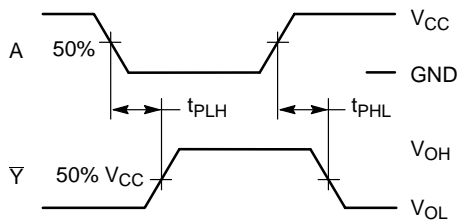


Figure 3. Switching Waveforms

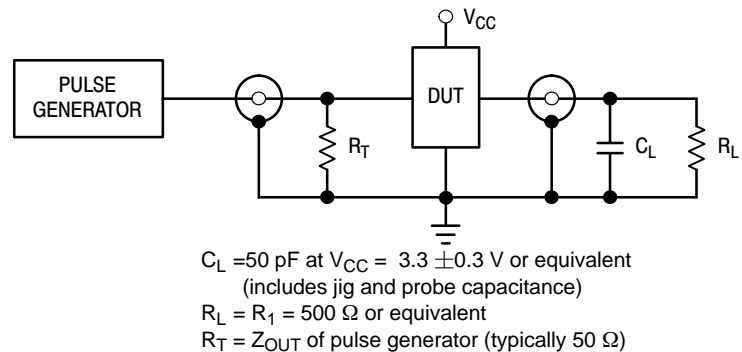
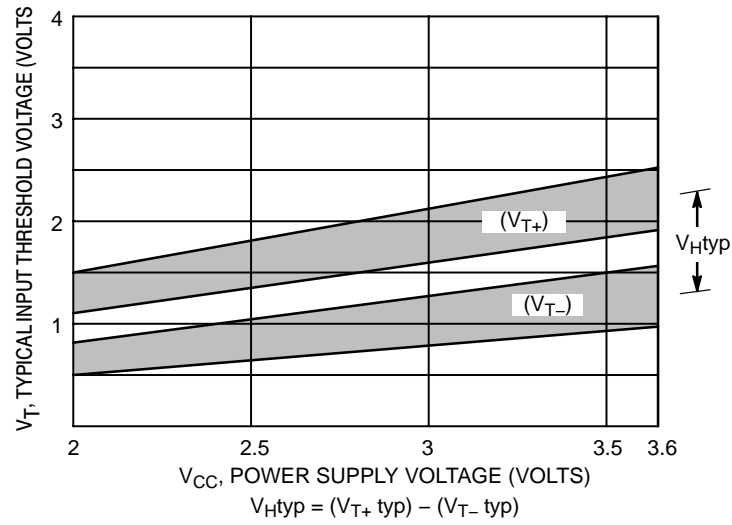


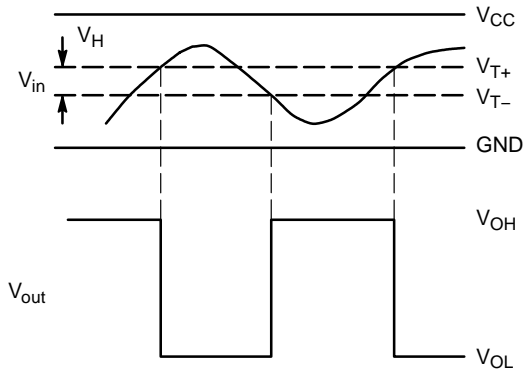
Figure 4. Test Circuit

# MC74LCX14

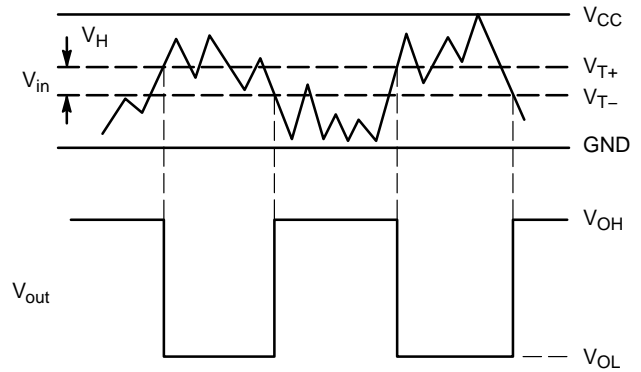


**Figure 5. Typical Input Threshold,  $V_{T+}$ ,  $V_{T-}$  versus Power Supply Voltage**

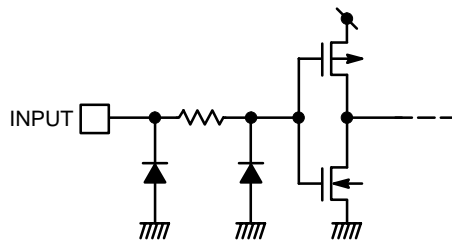
(a) A Schmitt-Trigger Squares Up Inputs With Slow Rise and Fall Times



(b) A Schmitt-Trigger Offers Maximum Noise Immunity



**Figure 6. Typical Schmitt-Trigger Applications**

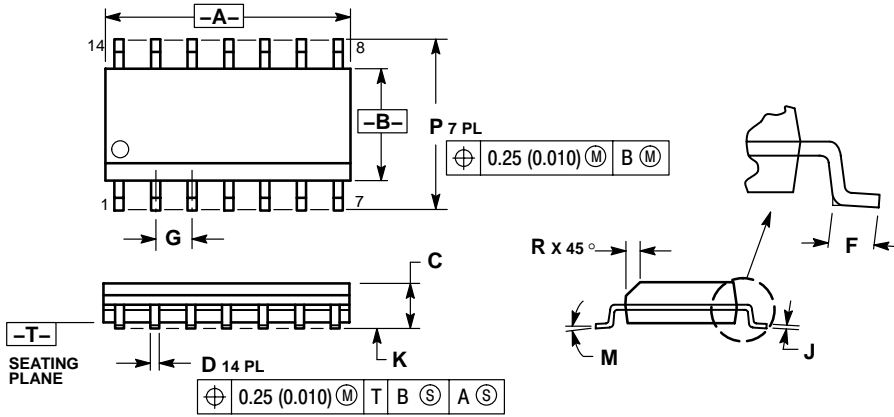


**Figure 7. Input Equivalent Circuit**

# MC74LCX14

## PACKAGE DIMENSIONS

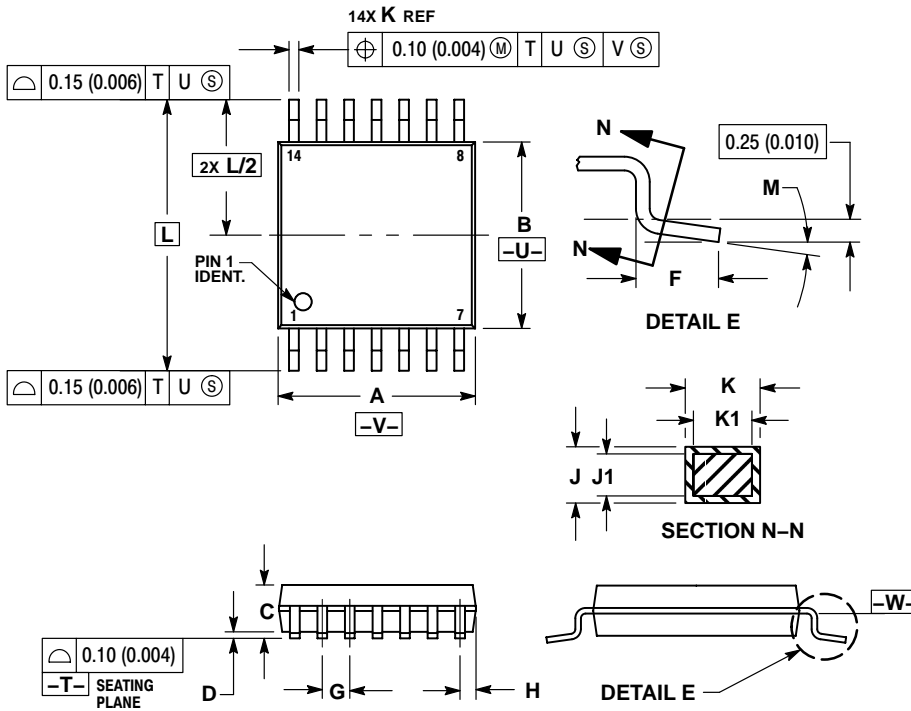
SOIC-14  
D SUFFIX  
CASE 751A-03  
ISSUE G



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
  5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

TSSOP-14  
DT SUFFIX  
CASE 948G-01  
ISSUE A



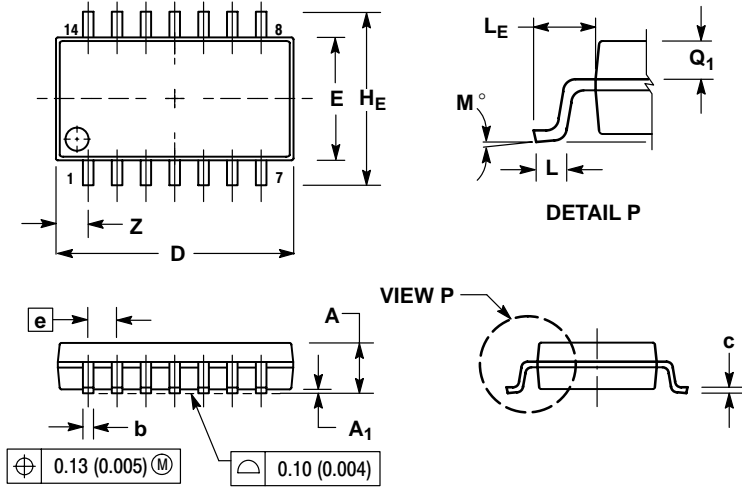
- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
  4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
  5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
  6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
  7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

# MC74LCX14

## PACKAGE DIMENSIONS

SOEIAJ-14  
M SUFFIX  
CASE 965-01  
ISSUE O



### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A <sub>1</sub>	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H <sub>E</sub>	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L <sub>E</sub>	1.10	1.50	0.043	0.059
M	0°	10°	0°	10°
Q <sub>1</sub>	0.70	0.90	0.028	0.035
Z	---	1.42	---	0.056

# MC74LCX14

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**MC74LCX14/D**