

MT29F512G08AUCBBH8-6

[Login or Register to](#)
[Global](#) [Products & Support](#) [NAND Flash](#) [SLC NAND](#) [MT29F512G08AUCBBH8-6](#)
[Add](#) [Email](#)
[See all SLC NAND parts](#) | [See all 512Gb SLC NAND parts](#)

Data Sheets (2)

Data Sheet

[» Download](#)
[Add](#)
[Email](#)

Errata

[» Download](#)
[Add](#)
[Email](#)

Orderable Parts (1)

[» Compare all](#)

Orderable Part Information

Status	Production	Alternative Part	N/A
FBGA Code	NW661	SPD Data	N/A
MBQual Data	N/A	Shipping Media	N/A
PLP	No	Start Date	N/A

Specs

Density	512Gb	Status	Production
RoHS	Yes	Width	x8
Voltage	3.3V	Package	LPGA
Pin Count	152-ball	MT/s	333 MT/s
I/O	Common		

Where to Buy

[View All Distributors](#)

Showing 34 Micron Distributors:

 « [»](#)

Need Help? Contact a sales rep to request samples, get a quote, and receive a callback.

[» Login](#)
[» Find my Rep](#)

Overview Documentation & Support Sim Models & Software FAQs

Recently Added

Date	What was added
11/2014	IBIS: 64Gb 128Gb 256Gb 512Gb Async Sync NAND
11/2014	HSpice: 64Gb 128Gb 256Gb 512Gb Async Sync NAND

FAQs

- » Do you support small block devices?
- » How much ECC do I need to support your devices?
- » I am using the correct amount of error correction code (ECC) for the NAND device, but I'm still seeing bitbyte errors in data I read back from the NAND device.
- » [See all FAQs](#)

Sim Models & Software

Title & Description	Secure	ID	Updated
HSpice: 64Gb 128Gb 256Gb 512Gb Async Sync NAND: Rev.2.2		M84C	11/2014
IBIS: 64Gb 128Gb 256Gb 512Gb Async Sync NAND: Rev.2.2		M84C	11/2014

[» See all Sim Models \(3\)](#)

Documentation & Support

Search

[» Search](#)

Filter

- Case Study
- Customer Service Note
- Data Sheet
- Other Documents
- Part Numbering Guide
- Presentation
- Product Flyer
- RoHS Certification
- Technical Note
- Tool
- Webinar
- White Paper

[+ For MT29F512G08AUCBBH8-6 \(4\)](#)
[+ For SLC NAND \(6\)](#)
[+ For NAND Flash \(32\)](#)
[+ For Products and Support \(14\)](#)

 Please Note: To view Secure Documents, please [click on a secured document to request access.](#)

Search

[» Search](#)

Filter

- NAND Flash Software
- Sim Model

[+ For MT29F512G08AUCBBH8-6 \(3\)](#)
[+ For SLC NAND \(6\)](#)
[+ For NAND Flash \(6\)](#)
[+ For Products and Support \(0\)](#)

 Please Note: To view Secure Documents, please [click on a secured document to request access.](#)

Disclaimers

- Micron Models:** By downloading any Micron model from this site, you must agree to the terms of [this disclaimer](#). If you do not agree to terms, you do not have permission to use the site or download material from it.
- Non-Micron Models:** For your convenience, Micron links to third-party simulation models. Note that Micron does not guarantee functionality or accuracy of these models.

- + Do you support small block devices?
- + How much ECC do I need to support your devices?
- + I am using the correct amount of error correction code (ECC) for the NAND device, but I'm still seeing bitbyte errors in data I read back from the NAND device.

- + How do I achieve greater PROGRAM/READ throughput for the NAND device?
- + How is Nvb specified?
- + I am seeing a lot of READ DISTURB errors. Can you tell me if there is a problem with your part?
- + I've heard that NAND has too many errors to boot from. Is this true?
- + Should I be marking blocks bad due to READ errors?
- + When I issue a Read ID command (90h) to a two-die NAND device, I get a device ID back that states it is a one-die NAND device.
- + Where can I find additional technical information about Micron NAND devices that is not covered in the device data sheets?
- + Where can I find simulation models for NAND Flash devices?
- + Why am I getting a bit/byte error reading back the information I programmed into the NAND device?
- + Why doesn't the NAND Flash device respond correctly to commands issued to it?
- + What is a "bank"?
- + What is the impedance tolerance of the driver in match-impedance mode relative to the expected value base on the perfect reference resistor connected to ZQ pin?
- + Does thermal information change for IT parts?
- + My design was based on a specification stating the JTAG was relative to VDD (1.8V), but now we've discovered that JTAG is actually relative to VDDQ (1.5V). It's a fairly significant board spin to change this; what do I risk by leaving the design as-is? I assume that the specification is still for VDDQ + 0.3V = 1.8V, but with CMOS parts there's no way I can guarantee that it won't swing past that on transitions.
- + Should the ECC memory chip share chip select and CKE signals with the other two main memory chips in our point-to-point application?

[+ Who do I contact if I have questions about my buy@micron.com order?](#)