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February 1984 Revised May 2005

## MM74HCT373 • MM74HCT374 3-STATE Octal D-Type Latch • 3-STATE Octal D-Type Flip-Flop

#### **General Description**

The MM74HCT373 octal D-type latches and MM74HCT374 Octal D-type flip flops advanced silicon-gate CMOS technology, which provides the inherent benefits of low power consumption and wide power supply range, but are LS-TTL input and output characteristic & pin-out compatible. The 3-STATE outputs are capable of driving 15 LS-TTL loads. All inputs are protected from damage due to static discharge by internal diodes to  $\mbox{V}_{\rm CC}$  and ground.

When the MM74HCT373 LATCH ENABLE input is HIGH, the Q outputs will follow the D inputs. When the LATCH ENABLE goes LOW, data at the D inputs will be retained at the outputs until LATCH ENABLE returns HIGH again. When a high logic level is applied to the OUTPUT CONTROL input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

The MM74HCT374 are positive edge triggered flip-flops. Data at the D inputs, meeting the setup and hold time requirements, are transferred to the Q outputs on positive going transitions of the CLOCK (CK) input. When a high logic level is applied to the OUTPUT CONTROL (OC) input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

#### **Features**

- TTL input characteristic compatible
- Typical propagation delay: 20 ns
- Low input current: 1 µA maximum
- Low quiescent current: 80 µA maximum Compatible with bus-oriented systems
- Output drive capability: 15 LS-TTL loads

#### **Ordering Code:**

Order Number	Package Number	Package Descriptions
MM74HCT373WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
MM74HCT373SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
MM74HCT373MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HCT373N	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
MM74HCT374WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
MM74HCT374SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
MM74HCT374MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HCT374N	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

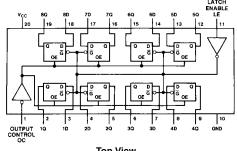
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# MM74HCT373 • MM74HCT374

#### **Connection Diagrams**



Top View MM74HCT374

Top View MM74HCT373

**Truth Tables** 

#### MM74HCT373

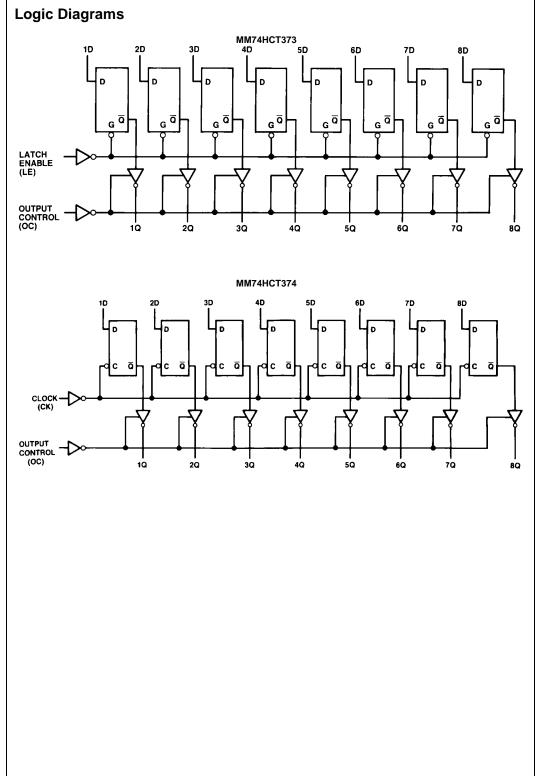
Output	LE	Data	373
Control			Output
L	Н	Н	Н
L	Н	L	L
L	L	X	$Q_0$
Н	Х	Х	Z

- H = HIGH Level
  L = LOW Level
  Q<sub>0</sub> = Level of output before steady-state input conditions were established.
- Z = High Impedance

#### MM74HCT374

Output	Clock	Data	Output
Control			(374)
L	1	Н	Н
L	<b>↑</b>	L	L
L	L	X	$Q_0$
Н	Χ	X	Z

- H = HIGH Level
  L = LOW Level
  X = Don't Care
  ↑ = Transition from LOW-to-HIGH
  Z = High Impedance State
  Q<sub>0</sub> = The level of the output before steady state input conditions were established.



#### **Absolute Maximum Ratings**(Note 1) (Note 2)

Supply Voltage (V<sub>CC</sub>) -0.5 to +7.0V DC Input Voltage (V<sub>IN</sub>) -1.5 to  $V_{CC}$  +1.5V DC Output Voltage (V<sub>OUT</sub>) -0.5 to  $V_{CC}$  +0.5V Clamp Diode Current (I<sub>IK</sub>, I<sub>OK</sub>) ±20 mA DC Output Current, per pin (I<sub>OUT</sub>)  $\pm 35~\text{mA}$ DC  $V_{CC}$  or GND Current, per pin ( $I_{CC}$ ) ±70 mA Storage Temperature Range (T<sub>STG</sub>) -65°C to +150°C

Power Dissipation (P<sub>D</sub>)

600 mW (Note 3) S.O. Package only 500 mW

Lead Temperature (T<sub>L</sub>)

(Soldering 10 seconds) 260°C

#### **Recommended Operating Conditions**

	Min	Max	Units
Supply Voltage (V <sub>CC</sub> )	4.5	5.5	V
DC Input or Output Voltage	0	$V_{CC}$	V
$(V_{IN}, V_{OUT})$ Operating Temperature Range $(T_A)$	-40	+85	°C
Input Rise or Fall Times			
$(t_r, t_f)$		500	ns

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground. Note 3: Power Dissipation temperature derating — plastic "N" package: -12 mW/°C from 65°C to 85°C.

#### **DC Electrical Characteristics**

 $V_{CC} = 5V \pm \, 10\%$  (unless otherwise specified)

Symbol	Parameter	Conditions	T <sub>A</sub> = 25°C		T <sub>A</sub> = -40 to 85°C	T <sub>A</sub> = -55 to 125°C	Units
Syllibol		Conditions	Тур		Guaranteed Limits		
V <sub>IH</sub>	Minimum HIGH Level			2.0	2.0	2.0	V
	Input Voltage			2.0	2.0	2.0	V
V <sub>IL</sub>	Maximum LOW Level			0.8	0.8	0.8	V
	Input Voltage			0.6	0.6	0.6	V
V <sub>OH</sub>	Minimum HIGH Level	$V_{IN} = V_{IH}$ or $V_{IL}$					
	Output Voltage	$ I_{OUT}  = 20 \ \mu A$	$V_{CC}$	V <sub>CC</sub> - 0.1	V <sub>CC</sub> - 0.1	V <sub>CC</sub> - 0.1	V
		$ I_{OUT}  = 6.0 \text{ mA}, V_{CC} = 4.5 \text{V}$	4.2	3.98	3.84	3.7	V
		$ I_{OUT}  = 7.2 \text{ mA}, V_{CC} = 5.5 \text{V}$	5.7	4.98	4.84	4.7	V
V <sub>OL</sub>	Maximum LOW Level	$V_{IN} = V_{IH}$ or $V_{IL}$					
	Voltage	$ I_{OUT}  = 20 \ \mu A$	0	0.1	0.1	0.1	V
		$ I_{OUT}  = 6.0 \text{ mA}, V_{CC} = 4.5 \text{V}$	0.2	0.26	0.33	0.4	V
		$ I_{OUT}  = 7.2 \text{ mA}, V_{CC} = 5.5 \text{V}$	0.2	0.26	0.33	0.4	V
I <sub>IN</sub>	Maximum Input	$V_{IN} = V_{CC}$ or GND,		±0.1	±1.0	±1.0	μА
	Current	$V_{\text{IH}}$ or $V_{\text{IL}}$		±0.1	±1.0	±1.0	μА
l <sub>OZ</sub>	Maximum 3-STATE	V <sub>OUT</sub> = V <sub>CC</sub> or GND					
	Output Leakage	Enable = V <sub>IH</sub> or VIL		±0.5	±5.0	±10	μΑ
	Current						
I <sub>CC</sub>	Maximum Quiescent	$V_{IN} = V_{CC}$ or GND		8.0	80	160	μА
	Supply Current	$I_{OUT} = 0 \mu A$		0.0	50	100	μΑ
		V <sub>IN</sub> = 2.4V or 0.5V (Note 4)		1.0	1.3	1.5	mA

Note 4: Measured per pin. All others tied to V<sub>CC</sub> or ground.

#### **AC Electrical Characteristics**

MM74HCT373: V  $_{CC}$  = 5.0V,  $t_{f}$  =  $t_{f}$  = 6 ns  $T_{A}$  = 25  $^{\circ}C$  (unless otherwise specified)

Symbol	Parameter	Conditions	Тур	Guaranteed Limit	Units
t <sub>PHL</sub> , t <sub>PLH</sub>	Maximum Propagation Delay Data to Output	C <sub>L</sub> = 45 pF	18	25	ns
t <sub>PHL</sub> , t <sub>PLH</sub>	Maximum Propagation Delay  Latch Enable to Output	C <sub>L</sub> = 45 pF	21	30	ns
t <sub>PZH</sub> , t <sub>PZL</sub>	Maximum Enable Propagation Delay Control to Output	$C_L = 45 \text{ pF}$ $R_L = 1 \text{ k}\Omega$	20	28	ns
t <sub>PHZ</sub> , t <sub>PLZ</sub>	Maximum Disable Propagation Delay Control to Output	$C_L = 5 pF$ $R_L = 1 k\Omega$	18	25	ns
t <sub>W</sub>	Minimum Clock Pulse Width			16	ns
t <sub>S</sub>	Minimum Setup Time Data to Clock			5	ns
t <sub>H</sub>	Minimum Hold Time Clock to Data			10	ns

#### **AC Electrical Characteristics**

MM74HCT373: VCC = 5.0V  $\pm$  10%,  $t_{\text{f}}$  =  $t_{\text{f}}$  = 6 ns (unless otherwise specified)

Symbol	Parameter	Conditions	T <sub>A</sub> =25°C		T <sub>A</sub> =-40 to 85°C	T <sub>A</sub> =-55 to 125°C	Units
Cymbol	1 arameter	Conditions	Тур		Guaranteed L	imits	Office
t <sub>PHL</sub> , t <sub>PLH</sub>	Maximum Propagation	C <sub>L</sub> = 50 pF	22	30	37	45	ns
	Delay Data to Output	C <sub>L</sub> = 150 pF	30	40	50	60	ns
t <sub>PHL</sub> , t <sub>PLH</sub>	Maximum Propagation Delay	C <sub>L</sub> = 50 pF	25	35	44	53	ns
	Latch Enable to Output	C <sub>L</sub> = 150 pF	32	45	56	68	ns
t <sub>PZH</sub> , t <sub>PZL</sub>	Maximum Enable Propagation	C <sub>L</sub> = 50 pF	21	30	37	45	ns
	Delay Control to Output	C <sub>L</sub> = 150 pF	30	40	50	60	ns
		$R_L = 1 k\Omega$					
t <sub>PHZ</sub> , t <sub>PLZ</sub>	Maximum Disable Propagation	C <sub>L</sub> = 50 pF	21	30	37	45	ns
	Delay Control to Output	$R_L = 1 k\Omega$					
$t_{THL}, t_{TLH}$	Maximum Output Rise	C <sub>L</sub> = 50 pF	8	12	15	18	ns
	and Fall Time						
t <sub>W</sub>	Minimum Clock Pulse Width			16	20	24	ns
t <sub>S</sub>	Minimum Setup Time Data to Clock			5	6	8	ns
t <sub>H</sub>	Minimum Hold Time Clock to Data			10	13	20	ns
C <sub>IN</sub>	Maximum Input Capacitance			10	10	10	pF
C <sub>OUT</sub>	Maximum Output Capacitance			20	20	20	pF
C <sub>PD</sub>	Power Dissipation Capacitance	$OC = V_{CC}$		5			pF
	(Note 5)	OC = GND		52			pF

Note 5:  $C_{PD}$  determines the no load dynamic power consumption,  $P_D = C_{PD} \ V_{CC} 2 \ f + I_{CC} \ V_{CC}$ , and the no load dynamic current consumption,  $I_S = C_{PD} \ V_{CC} 2 \ f + I_{CC} \ V_{CC}$ , and the no load dynamic current consumption,  $I_S = C_{PD} \ V_{CC} 2 \ f + I_{CC} \ V_{CC} 2 \ f + I_{CC}$ 

#### **AC Electrical Characteristics**

MM74HCT374: V\_CC = 5.0V,  $t_{f}$  =  $t_{f}$  = 6 ns  $T_{A}$  = 25°C (unless otherwise specified)

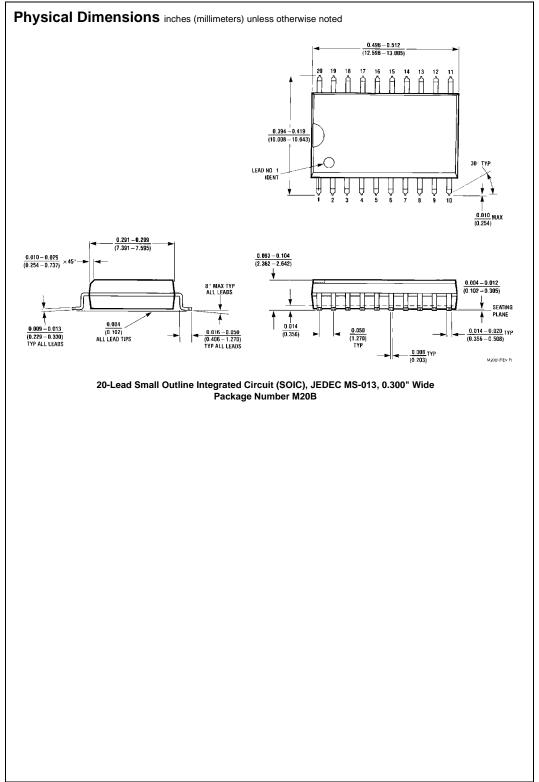
Symbol	Parameter	Conditions	Тур	Guaranteed	Units
- Cymbol	T drameter	Conditions	1,75	Limit	Offics
f <sub>MAX</sub>	Maximum Clock Frequency		50	30	MHz
t <sub>PHL</sub> , t <sub>PLH</sub>	Maximum Propagation Delay	C <sub>L</sub> = 45 pF	20	32	ns
	to Output				
t <sub>PZH</sub> , t <sub>PZL</sub>	Maximum Enable Propagation Delay	C <sub>L</sub> = 45 pF	19	28	ns
	Control to Output	$R_L = 1 k\Omega$			
t <sub>PHZ</sub> , t <sub>PLZ</sub>	Maximum Disable Propagation Delay	C <sub>L</sub> = 5 pF	17	25	ns
	Control to Output	$R_L = 1 k\Omega$			
t <sub>W</sub>	Minimum Clock Pulse Width			20	ns
t <sub>S</sub>	Minimum Setup Time Data to Clock			5	ns
t <sub>H</sub>	Minimum Hold Time Clock to Data			16	ns

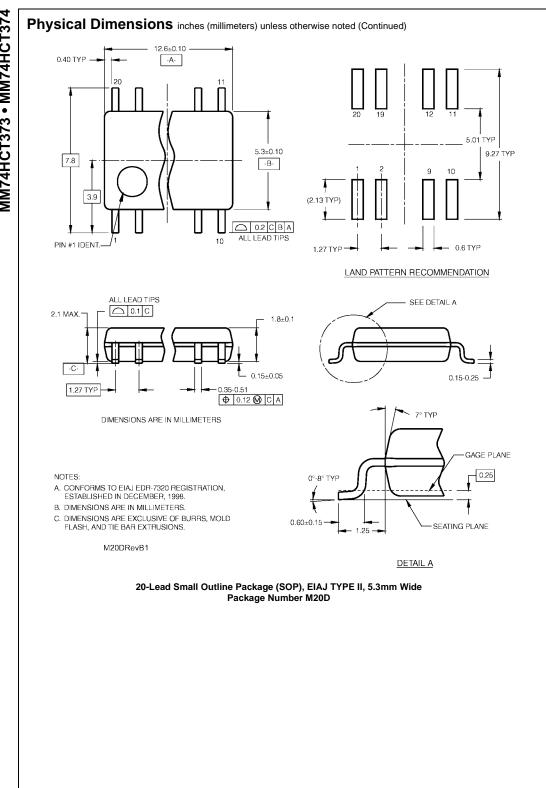
#### **AC Electrical Characteristics**

MM74HCT374:  $\text{V}_{CC} = 5.0 \text{V} \, \pm \, 10\%, \; t_\text{f} = t_\text{f} = 6 \; \text{ns} \; \text{(unless otherwise specified)}$ 

Symbol	Parameter	Conditions	T <sub>A</sub> = 25°C		$T_A = -40 \text{ to } 85^{\circ}\text{C}$ $T_A = -55 \text{ to } 125^{\circ}\text{C}$		Units
Symbol		Conditions	Тур		Guaranteed L	imits	Onits
f <sub>MAX</sub>	Maximum Clock Frequency			30	24	20	MHz
t <sub>PHL</sub> , t <sub>PLH</sub>	Maximum Propagation Delay	C <sub>L</sub> = 50 pF	22	36	45	48	ns
	to Output	C <sub>L</sub> = 150 pF	30	46	57	69	ns
t <sub>PZH</sub> , t <sub>PZL</sub>	Maximum Enable Propagation	C <sub>L</sub> = 50 pF	21	30	37	45	ns
	Delay Control to Output	C <sub>L</sub> = 150 pF	30	40	50	60	ns
		$R_L = 1 k\Omega$					
t <sub>PHZ</sub> , t <sub>PLZ</sub>	Maximum Disable Propagation	C <sub>L</sub> = 50 pF	21	30	37	45	ns
	Delay Control to Output	$R_L = 1 k\Omega$					
t <sub>THL</sub> , t <sub>TLH</sub>	Maximum Output Rise	C <sub>L</sub> = 50 pF	8	12	15	18	ns
	and Fall Time						
t <sub>W</sub>	Minimum Clock Pulse Width			16	20	24	ns
t <sub>S</sub>	Minimum Setup Time Data to Clock			20	25	30	ns
t <sub>H</sub>	Minimum Hold Time Clock to Data			5	5	5	ns
C <sub>IN</sub>	Maximum Input Capacitance			10	10	10	pF
C <sub>OUT</sub>	Maximum Output Capacitance			20	20	20	pF
C <sub>PD</sub>	Power Dissipation Capacitance	OC = V <sub>CC</sub>		5			pF
	(Note 6)	OC = GND		58			pF

Note 6:  $C_{PD}$  determines the no load power consumption,  $P_D = C_{PD} V_{CC} 2 f + I_{CC} V_{CC}$ , and the no load dynamic current consumption,  $I_S = C_{PD} V_{CC} f + I_{CC} V_{CC}$ , and the no load dynamic current consumption,  $I_S = C_{PD} V_{CC} f + I_{CC} V_{CC}$ .

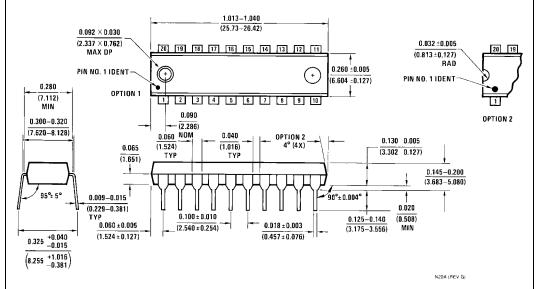




#### Physical Dimensions inches (millimeters) unless otherwise noted (Continued) -0.20 7.72 64 4.4±0.1 -B-0.65 PIN #1 IDENT. LAND PATTERN RECOMMENDATION O.1 C ALL LEAD TIPS SEE DETAIL A -0.90<sup>+0.15</sup> 0.09-0.20 0.65 0.19-0.30 | \$\dag{0.10\dag{A} R\$ 0\$ R0.09mir GAGE PLANE DIMENSIONS ARE IN MILLIMETERS NOTES: A. CONFORMS TO JEDEC REGISTRATION MD-153, VARIATION AC, REF NOTE 6, DATE 7/93. 0.6±0.1 R0.09min -1.00 B. DIMENSIONS ARE IN MILLIMETERS. C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLDS FLASH, AND THE BAR EXTRUSIONS. DETAIL A D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982. MTC20REVD1 20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide Package Number MTC20

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#### Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N20A

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