ST4300

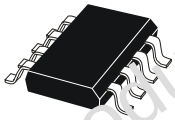
Hot swappable 2-wire bidirectional bus buffer

Features

- Bidirectional I^2C buffer
- Live board insertion and removal without SCL and SDA corruption
- Compatible with I^2C^{TM} and SMBus (up to 400 kHz)
- Low current consumption in disabled mode: $I_{CC} < 1$ µA
- 1 V precharge on SDA and SCL lines
- Supports clock stretching, arbitration and synchronization
- Power down protection, SDA and SCL line goes to high impedance when $V_{CC} = 0$ V
- Available in a small MSOP-8L package

Applications

- Hot board insertion
- Buffer/bus extenders
- Desktop computers
- Servers



MSOP-8L

Description

The ST4300 hot swappable 2-wire bus buffer provides bidirectional buffering for 2-wire open drain systems such as I^2C and SMBus, which isolates the capacitance of input and output side.

When connected, a one-shot circuit in the ST4300 accelerates the rise time allowing the use of a weaker pull-up while still meeting the rise-time requirements.

During live insertion, the ST4300 I/O is precharged to 1 V through a 100 kΩ resistor. When a Stop or Idle bus is detected, the I/O are connected to the buffer circuit, this procedure prevents data corruption in the bus. The V_{CC2} enables the device to become a level translator, both V_{CC} and V_{CC2} can be supplied by voltage ranging from 2.7 V to 5.5 V with no constraint which supply is higher.

The ST4300 includes a digital ENABLE input pin which forces the device to shutdown completely and put the I/O into Hi-Z mode.

Table 1. Device summary

Order code	Package	Packaging
ST4300TTR	MSOP-8L	Tape and reel

1 Pin configuration

Figure 1. Pin description

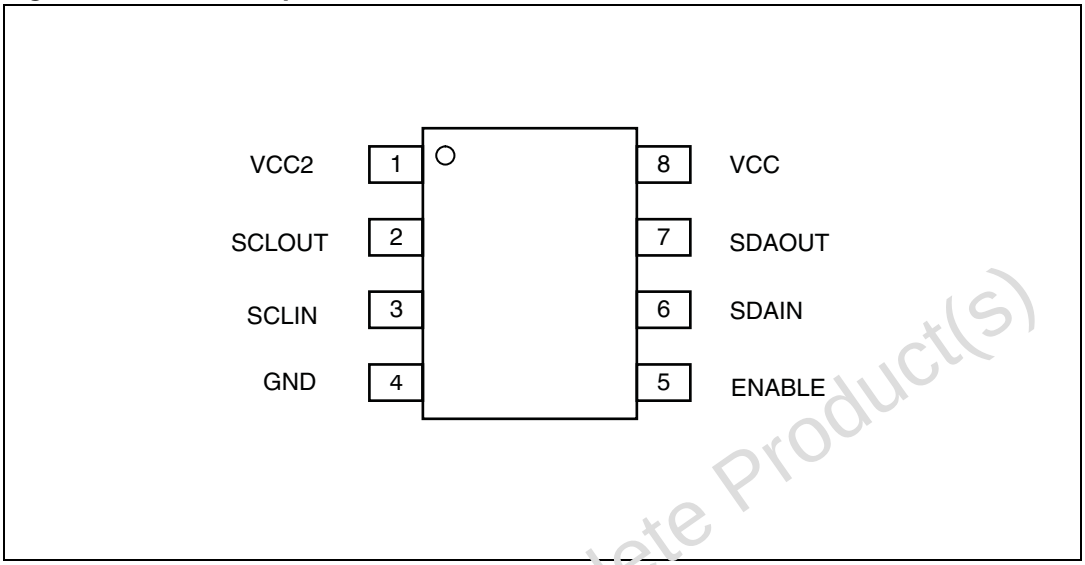
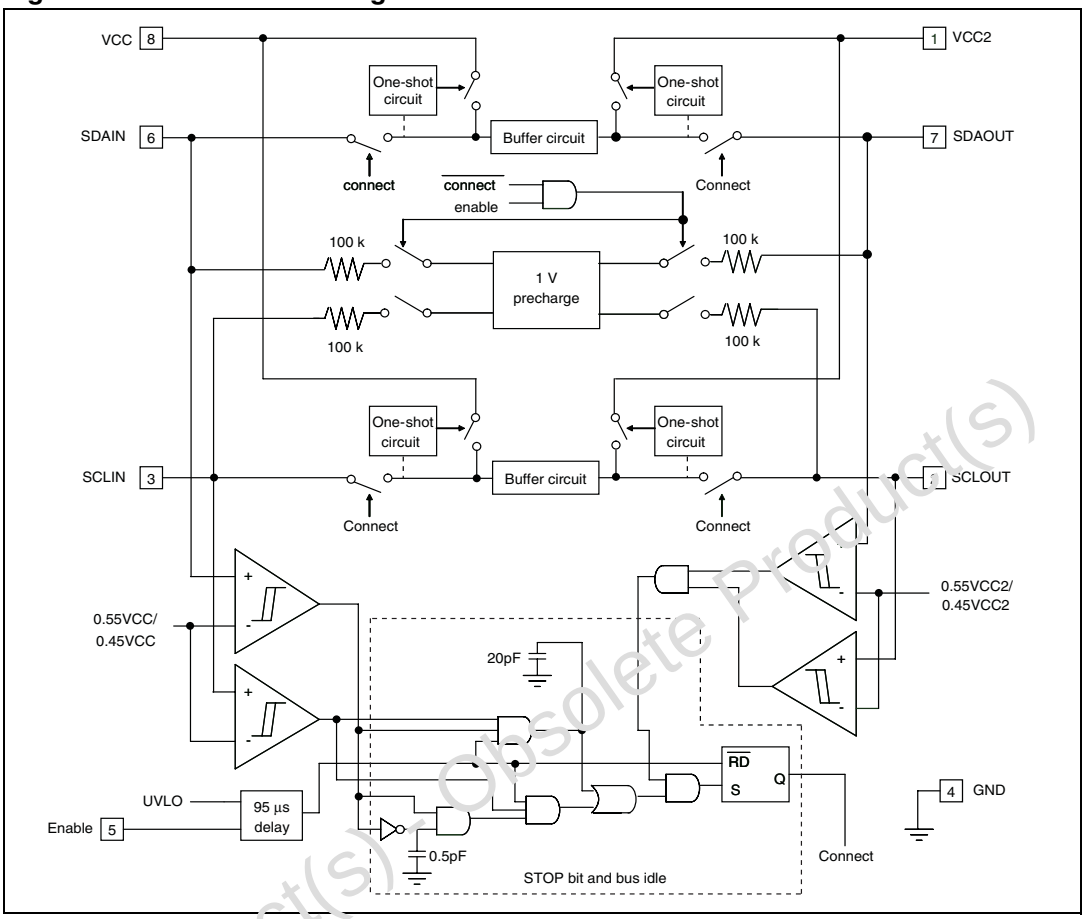


Table 2. Pin assignment

Pin	Name	Function
1	V_{CC2}	This pin provides power to the output signal. Connecting a different voltage to this pin (compared to V_{CC}) results in a level translating function between the input and output. Pull-up resistors for I^2C OUTPUT should be pulled to this supply level.
2	SCLOUT	Serial clock output
3	SCLIN	Serial clock input
4	GND	Ground
5	ENABLE	'0' set the device into low current mode. Input is isolated from output '1' set the device into normal operation
6	SDAIN	Serial data input
7	SDAOUT	Serial data output
8	V_{CC}	Main power supply

Figure 2. ST4300 block diagram



2 Operation

2.1 Start up

When the ST4300 receives power on its power supply pin V_{CC}, the under voltage lockout (UVLO) circuit starts to work and detects whether the supply voltage is enough for the device's safe operation. In UVLO state, any activity on the SDA or SCL (I/O pins) is ignored. At the same time, the precharge circuit is charging the I/O lines to 1 V through a 100 kΩ resistor, to minimize any worst-case voltage difference during the connection, hence reducing disturbance in the active line.

Once the ST4300 exits from the UVLO state, it scans the SDA and SCL buses for either a Stop bit or bus Idle state, and also ensures that the SDA and SCL lines are HIGH, before it connects the buffer circuits to the I/O lines.

2.2 Buffer circuit

The buffer circuit provides bidirectional buffering which separate the capacitance of input and output. If any of the pins, input or output, is pulled LOW, both pins are pulled LOW.

Only when both input and output are HIGH then the buffer circuit releases the line allowing the pull-up resistor to pull up the line HIGH. This feature allows to separate the input and output capacitance and at the same time support clock stretching, clock arbitration and the acknowledgement protocol to work.

2.3 Input/output offset

When the SDA or SCL input/output pins are driven low (V_{LOW1}), the ST4300 regulates the voltage at the other side (V_{LOW2}) to a slightly higher voltage.

This is described in the following expression:

$$V_{LOW2} = V_{LOW1} + 75mV + (V_{CC}/R) \times 100$$

where R is the bus pull-up resistor value in ohms.

2.4 Pull-up resistor selection

As mentioned above, the offset between input and output is affected by the pull-up resistor chosen. The pull-up resistor must be chosen so that the output is still in valid range of LOW state or lower than V_{IL} specification. Based on the I^2C specification version 2.1 (*Table 3*), the V_{OL} of I^2C device must be able to provide 0.4 V maximum low level voltage with 3 mA pull-up current, and V_{IL} of I^2C device must be at least 0.3 V_{CC}. The V_{IL} of ST4300 is 0.6 V which is above the V_{OL} of I^2C device, it guarantees that the ST4300 is compatible with I^2C low level signal.

Table 3. I^2C specification

Parameter	Symbol	Standard mode		Fast mode	
		Min	Max	Min	Max
Low input voltage	V_{IL}	–	$0.3V_{CC}$	–	$0.3V_{CC}$
High input voltage	V_{IH}	$0.7V_{CC}$	–	$0.7V_{CC}$	–
Low output voltage, at 3 mA pull-up current	V_{OL}	0	0.4 V	0	0.4 V

At the input of ST4300 (which is output of the I^2C device host or slave), a pull-up resistor must be chosen so that the pull-up current is not exceeding 3 mA. This is to ensure that the level LOW state voltage level is not higher than 0.4 mV. The minimum value of the pull-up resistor is 1000 Ω at 2.7 V V_{CC}, and 1900 Ω at 5.5 V V_{CC}.

When the ST4300's input voltage is at the worst case of 0.4 V (V_{OL} of I^2C device), assuming the pull-up resistor (at the output) is 1 kΩ and V_{CC} = 2.7 V, the output voltage will be 745 mV which is lower than the V_{IL} of I^2C device (0.3 V_{CC} = 810 mV).

For the correct ST4300's operation and to increase the noise margin, the minimum value of 6.8 kΩ pull-up resistor at input/output is recommended.

2.5 SMBus

The same rule applies for the SMBus system, minimum value of 15 kΩ and 6.8 kΩ pull-up resistor is recommended for low power and high power SMBus system respectively.

In order to activate the one-shot circuit, the pull-up resistor must be able to provide a slew rate of 1.25 V/µs. The formula below can be used to determine the maximum value of pull-up resistor:

$$R \leq (V_{CC(MIN)} - 0.6) \times (800{,}000)/C$$

But, the start-up circuitry needs high voltage at SDA and SCL pins and the pull-up resistor must be able to override the pre-charge voltage. So, regardless of the capacitive load, a pull-up resistor must be chosen as shown below respectively for V_{CC} = 5.5 V:

$$R \leq 16\,k\Omega$$

and for V_{CC} = 3.6 V:

$$R \leq 24\,k\Omega$$

Table 4. SMBus specification

Parameter	Symbol	Low power		High power	
		Min	Max	Min	Max
Low input voltage	V_{IL}	–	0.8 V	–	0.8 V
High input voltage	V_{IH}	2.1 V	–	2.1 V	–
Low output voltage at max 350 µA pull-up current	V_{OL}	0	0.4 V	–	–
Low output voltage, at min 4 mA pull-up current	V_{OL}	–	–	0	0.4V

2.6 One-shot circuit

This circuit will provide a low resistance path from I/O to V_{CC} during the transition from LOW to HIGH to help pulling the SCL/SDA bus HIGH. It allows user to use weak pull-up resistance while still meeting rise time requirements.

The one-shot circuit is designed to be triggered only when both input and output are released by external driver, this is to ensure clock synchronization and acknowledgement procedure work properly. Once the one-shot is triggered, it pulls both input and output to V_{CC}/V_{CC2} fast, and it will be turned OFF when the input/output reach voltage near V_{CC}/V_{CC2}. But, in the event where one-shot is turned ON and at the same time external driver is pulling LOW (which might cause the voltage level stuck in the middle of GND and V_{CC}), one-shot circuit will be automatically turned OFF after 400 ns. This feature is to prevent high current flows for long period.

2.7 ENABLE pin

Setting the ENABLE pin LOW will put ST4300 in low current state where the buffer circuit is disconnected, one-shot circuit is disabled, the pre-charge circuit is turned OFF. If the ENABLE pin is set HIGH after LOW, the start-up sequence as mentioned in *Section 2.1*is executed.

3 Maximum rating

Stressing the device above the rating listed in the “Absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only, and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 5. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	-0.3 to 6	V
V_{CC2}	Supply voltage	-0.3 to 6.0	V
I/O	Input/output voltage	-0.3 to 6.0	V
T_{STG}	Storage temperature range	-65 to +125	°C
ESD	Electrostatic discharge protection (HBM)	±2	kV

3.1 Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply voltage	2.7	–	5.5	V
V_{CC2}	Supply voltage	2.7	–	5.5	V
EN	Device enable pin	0	–	5.5	V
I/O	Input/output pins	0	–	5.5	V
T_{OP}	Operating temperature	-40	–	85	°C

4 Electrical characteristics

Over recommended operating conditions unless otherwise noted.
All typical values are at T_A = 25 °C, V_{CC} = V_{CC2} = 5.5 V

Table 7. Supply specifications

Symbol	Parameter	Test conditions	Value			Unit
			TA = 25 °C			
			Min	Typ	Max	
I_{SD}	Shutdown current	V_{EN} = 0 V	–	0.1	10	µA
I_{CC}	Supply current of V_{CC}	V_{CC} = V_{CC2} = 5.5 V SDAIN = SCLIN = 0 V	–	3.0	4.1	mA
I_{CC2}	Supply current of V_{CC2}		–	2.1	2.9	mA

Table 8. Start-up circuit

Symbol	Parameter	Test conditions	Value			Unit
			TA = 25 °C			
			Min	Typ	Max	
V_{PRE}	Pre-charge voltage	I/O floating	0.8	1.0	1.2	V
T_{IDLE}	Bus idle time		50	95	150	µs
V_{IL-EN}	Low level enable voltage		–	–	0.3V_{CC}	V
V_{IH-EN}	High level enable voltage		0.45V_{CC}	–	–	V
I_{EN}	Input current to EN pin	V_{EN} = 0 V or V_{CC}	–	±0.1	±1.0	µA
T_{P-EN}	Enable delay, on-off		–	10	–	ns
	Enable delay, off-on		–	95	–	µs
UVLO	UVLO threshold of V_{CC}		–	2.5	–	V
	UVLO threshold of V_{CC2}		–	2.0	–	V

Table 9. One-shot circuit

Symbol	Parameter	Test conditions	Value			Unit
			TA = 25 °C			
			Min	Typ	Max	
$I_{ONE-SHOT}$	One-short current	Positive transition, $V_{CC} = V_{CC2} = 2.7$ V guaranteed by design	–	2	–	mA

Table 10. Buffer circuit

Symbol	Parameter	Test conditions	Value			Unit
			TA = 25 °C			
			Min	Typ	Max	
V_{IL}	Low level input voltage	V_{CC} and V_{CC2} range = 2.7 V to 5.5 V	–	–	0.6	V
V_{IH}	High level input voltage	V_{CC} and V_{CC2} range = 2.7 V to 5.5 V	2.1	–	–	V
$V_{OS\_I/O}$	Input-output offset voltage	10 KΩ pull-up V_{CC} = 3.3 V V_{IL} = 0.2 V	–	100	175	mV
$V_{OL\_I/O}$	Output low voltage	SDA, SCL pins, I_{SINK} = 2 mA, $V_{CC} = V_{CC2} = 2.7$ V	0	–	0.4	V
$f_{SCL, SDA}$	Operating frequency	Guaranteed by design	–	400		kHz
C_{IN}	I/O input capacitance	Guaranteed by design	–	–	10	pF
$I_{I/O}$	I/O leakage current	SDA, SCL = V_{CC} = 5.5 V, V_{CC2} = 5.5 V	–	–	±10	µA

Table 11. Timing characteristics

Symbol	Parameter	Test conditions	Value			Unit
			TA = 25 °C			
			Min	Typ	Max	
f_{I2C}	I^2C operating frequency	Guaranteed by design	0	–	400	kHz
t_{BUF}	Bus free time between stop and start condition	Guaranteed by design	1.3	–	–	µs
$t_{hD,STA}$	Hold time after (repeated) start condition	Guaranteed by design	0.6	–	–	µs
$t_{su,STA}$	Repeated start setup time	Guaranteed by design	0.6	–	–	µs
$t_{su,STO}$	Stop condition setup time	Guaranteed by design	0.6	–	–	µs
$t_{hD,DAT}$	Data hold time	Guaranteed by design	300	–	–	µs
$t_{su,DAT}$	Data setup time	Guaranteed by design	100	–	–	µs
t_{LOW}	Clock low period	Guaranteed by design	1.3	–	–	µs
t_{HIGH}	Clock high period	Guaranteed by design	0.6	–	–	µs
t_R	Rise time	10 kΩ pull-up, V_{CC} = 5.5 V	–	–	300	µs
t_F	Fall time	10 kΩ pull-up, V_{CC} = 5.5 V	–	–	300	µs

5 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Figure 3. MSOP-8L package outline

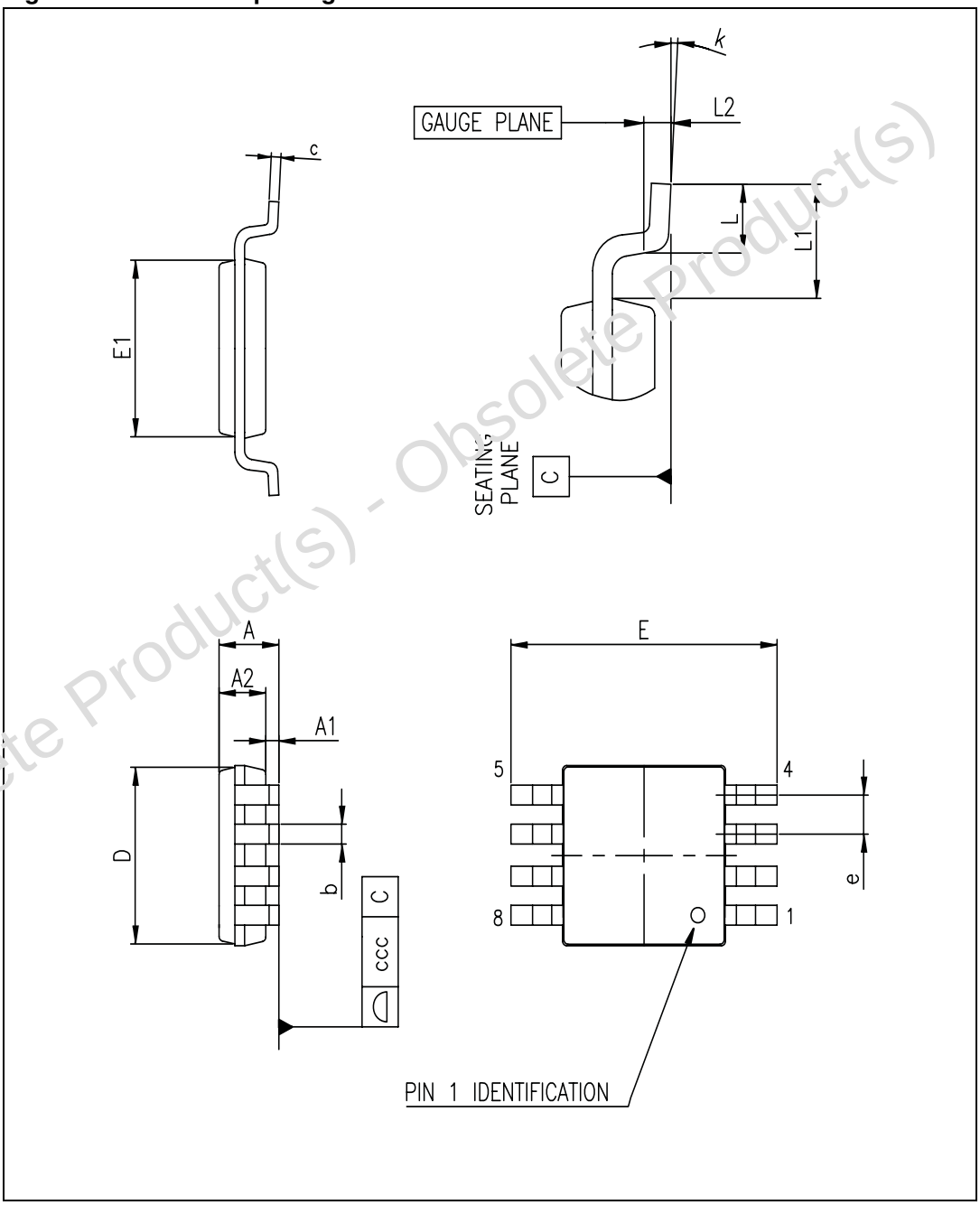


Table 12. MSOP-8L mechanical data

Symbol	Millimeters		
	Min	Typ	Max
A	–	–	1.10
A1	0	–	0.15
A2	0.75	0.85	0.95
b	0.22	–	0.40
c	0.08	–	0.23
D	2.80	3.00	3.20
E	4.65	4.90	5.15
E1	2.80	3.00	3.10
e	–	0.65	–
L	0.40	0.60	0.80
L1	–	0.95	–
L2	–	0.25	–
K	0^o	–	8^o
ccc	–	–	0.10

6 Applications examples

6.1 Live insertion and capacitance buffering

Figure 4 and *Figure 5* show some examples of applications implementing the ST4300 features of hot swap control and capacitance buffer. In a bus where all the cards are connected directly, the backplane must drive the capacitive load of all the cards, which may be quite significant or even higher than the I^2C/SMBUS specification. By placing the ST4300 device on every card, the backplane now can only see the capacitance of the ST4300 I/O, which is less than 10 pF on every card, while the whole capacitive loads at the card side is driven by the ST4300. This method increases the number of cards which can be driven by the backplane.

The ST4300 may be used also for applications as shown in *Figure 4*. V_{CC} and V_{CC2} might have different values and the ST4300 acts as a level translator. Both V_{CC} pins are connected first before SDAIN, SCLIN and ENABLE by a longer connector to ensure SDAIN and SCLIN is biased to 1 V before these are connected to the backplane bus. The ENABLE pin is pulled LOW by a resistor and having a shorter connector to disable the ST4300 until all other pins are connected and the transient is settled.

Figure 4. Card hot-swap into backplane using the ST4300 in "Compact PCI system"

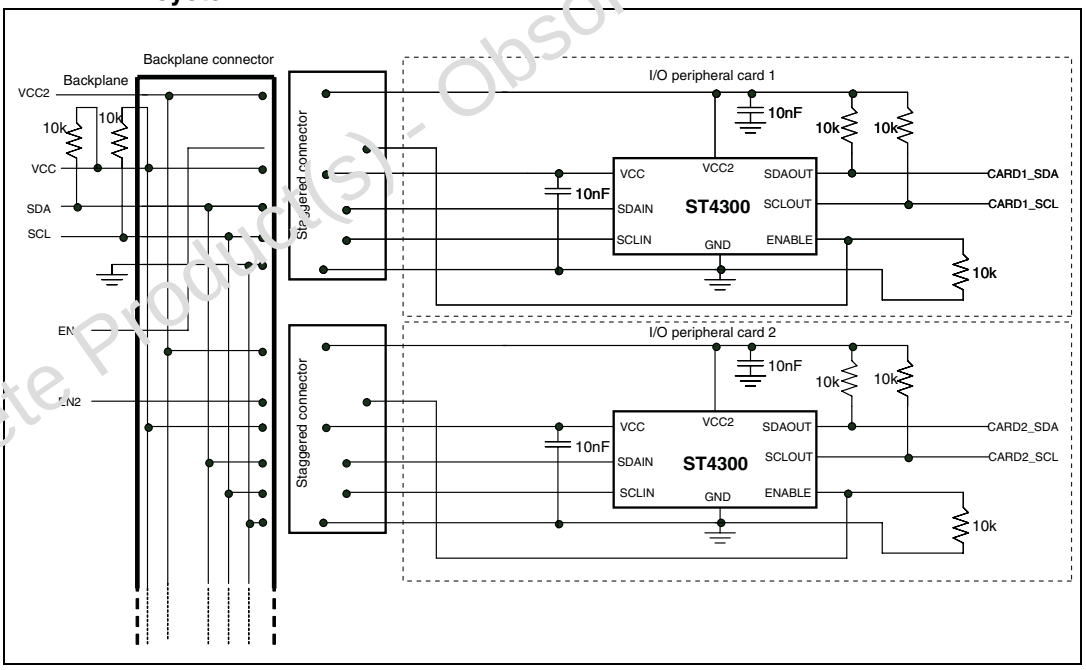
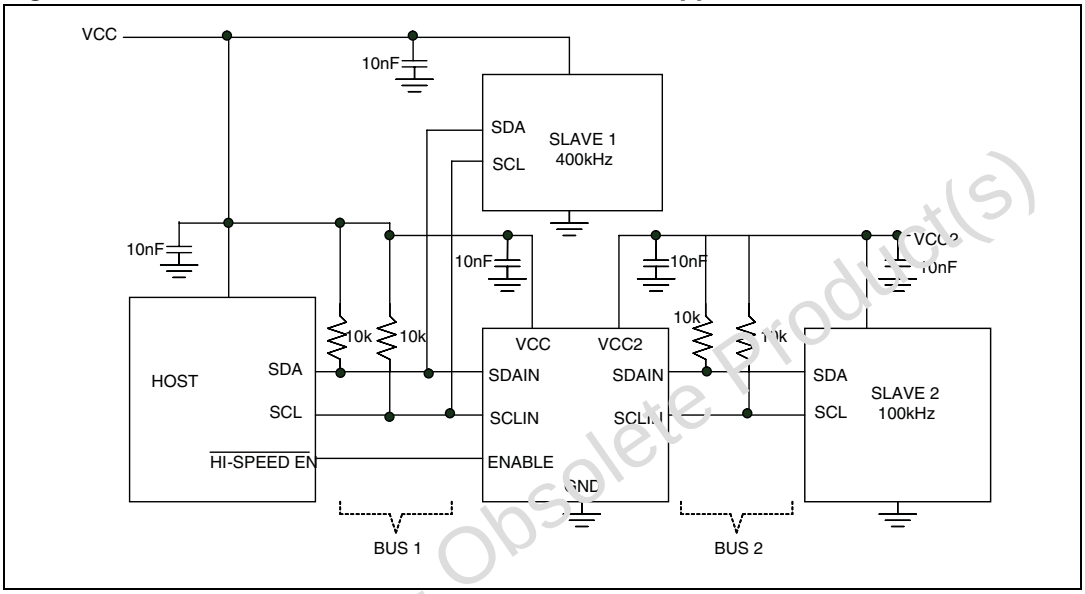


Figure 5 shows a system with two different types of slaves. The first type has higher speed and lower input capacitance while the other type is compatible with lower speed and has higher input capacitance. The ST4300 can be used to isolate the lower speed slave if the host only needs to communicate with the higher speed device and at the same time reduce the capacitance loading at the bus. At the same time, the ST4300 device can operate as a level translator if the power supply to any of the slaves is different from the host.

Figure 5. Buffer/bus extender and level translator application



7 Revision history

Table 13. Document revision history

Date	Revision	Changes
21-May-2008	1	Initial release.
30-Apr-2009	2	Document status promoted from Preliminary data to datasheet. Modified: ECOPACK information.

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