NCP102MBGEVB

NCP102 4 W Motherboard Evaluation Board User's Manual

ON Semiconductor®

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EVAL BOARD USER'S MANUAL

Introduction

The NCP102 low dropout linear regulator controller contains all the control and protection features needed to implement a low voltage regulator. The required external N−Channel MOSFET allows the device to be used in applications across a broad range of voltage and power levels.

The NCP102 is the ideal choice for new generation low voltage supplies in computing motherboard and consumer applications thanks to the following features:

- **A dedicated enable input:** allows the controller to be remotely enabled or sequenced.
- **An extremely accurate 0.8 V (±2.0%) reference:** allows the implementation of sub 1 V voltage supplies.
- **Adjustable soft−start:** allows the system to turn on in a controlled manner eliminating output voltage overshoot.
- **Minimum drive capability of ±5 mA:** provides fast transient response. The drive current is internally limited to protect the controller in case of an external MOSFET failure.
- **Wide voltage supply operation:** allows the controller to be biased directly from existing voltage supplies without the need of external voltage limiting circuits.

Linear Regulators

Linear regulators are a common topology for generating a lower voltage supply from a higher voltage. A linear regulator consists of a voltage reference (V_{REF}), an error amplifier and a pass transistor as shown in Figure 1.

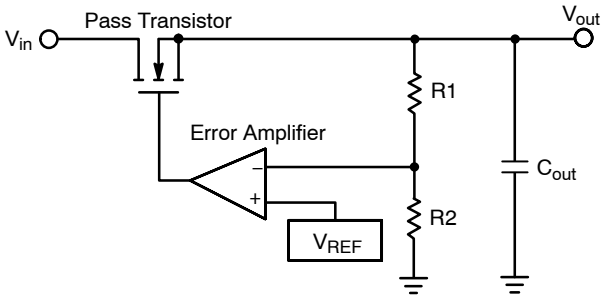

Figure 1. Simplified Linear Regulator Model

A fraction of the output voltage is compared to the internal reference voltage by means of resistor divider R1 and R2. The minimum output voltage is limited by the voltage reference. The pass transistor is selected to achieve the desired input voltage and output current.

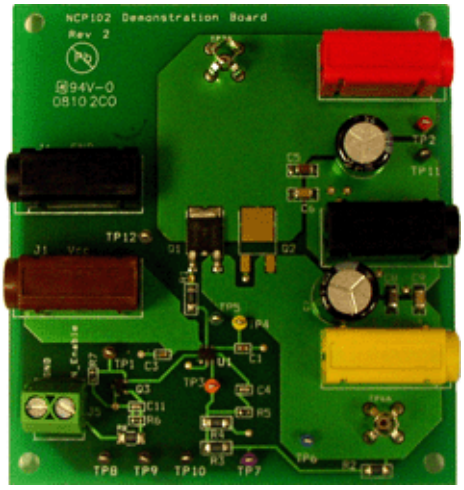

Figure 2. Evaluation Board Photo

Stability of linear regulators is very critical as with any feedback system. The main contributors to the stability of a linear regulator are the error amplifier, the external pass transistor, the output capacitor(s) and load. Figure 3 shows a model of a linear regulator used to evaluate the frequency response of the regulator.

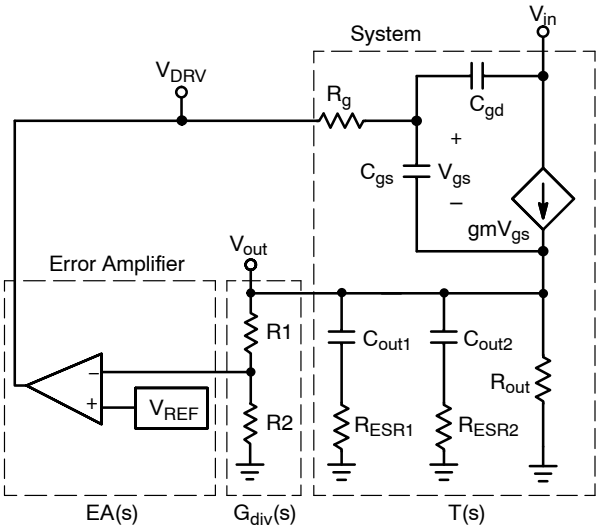

Figure 3. Frequency Model of a Linear Regulator

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The overall system response, H(s), is given by Equation 1.

$$H(s) = EA(s) \cdot G_{div}(s) \cdot T(s) \quad \text{(eq. 1)}$$

The error amplifier (EA(s)) usually has a dominant pole at a low frequency with additional poles or zeros at higher frequencies. Assuming its additional frequency components are above the frequency range of interest, the frequency response can be approximated to a single pole response as given by Equation 2.

$$EA(s) = \frac{K1}{(s + p1)} \quad \text{(eq. 2)}$$

where K1 is the dc gain and p1 is the dominant pole. The resistor divider attenuates the system gain, $G_{div}(s)$, and its magnitude is given by Equation 3.

$$G_{div}(s) = 20 \cdot \log\left(\frac{R2}{R1 + R2}\right) \quad \text{(eq. 3)}$$

The frequency response of the external components from V_{DRV} to V_{out} is a little more complicated. The response is determined by the output capacitors and the external pass transistor. If only one capacitor is considered the transfer response can be simplified as described in ON Semiconductor's application note AND8037.

Each output capacitor contributes a zero due to its equivalent series resistance (ESR). In the case of two types of output capacitors (such as electrolytic and ceramic), zeros at different frequencies are generated. The external pass transistor contributes a zero and affects the poles of the system. The frequency response from V_{DRV} to V_{out} is given by Equation 4.

$$T(s) = \frac{R_{out}(sC_{gs} + 1) \cdot (sR_{ESR1}C_{OUT1} + 1) \cdot (sR_{ESR2}C_{OUT2} + 1)}{D_4s^4 + D_3s^3 + D_2s^2 + D_1s + (1 + g_mR_{out})} \quad \text{(eq. 4)}$$

where:

$D_4 = C_{gs}R_{out}C_{gd}R_gR_X$

$D_3 = C_{gs}R_{out}C_{gd}R_gR_X + R_gR_XC_X + C_XR_{out}R_gR_{ESR2}C_{out2}C_{out1} + R_{out}R_gR_{ESR1}C_{out1}C_{out2}C_X + R_{out}R_X(R_gg_mC_{gd} + C_{gs})$

$D_2 = C_{gs}R_{out}C_{gd}R_g + R_gR_{ESR1}C_{out1}C_X + R_X + R_{ESR2}C_{out2}R_gC_X + C_{out1}R_{out}R_{ESR2}C_{out2} + C_{out1}R_{out}R_gC_X + C_{out2}R_{out}R_{ESR1}C_{out1} + C_{out2}R_{out}R_gC_X + g_mR_{out}R_X + g_mR_{out}R_gC_{gd}R_S + C_{gs}R_{out}R_S$

$D_1 = R_gC_X + R_S + R_{out}\,(C_{out1} + C_{out2} + C_{gs}) + g_mR_{out}(R_S + C_{gd}R_g)$

$R_X = R_{ESR1}C_{out1}R_{ESR2}C_{out2}$

$C_X = C_{gs} + C_{gd}$

$R_S = R_{ESR1}C_{out1} + R_{ESR2}C_{out2}$

and gm is the transconductance of the external transistor.

It is obvious that the overall transfer response is too complex for hand calculations. Even with several simplifications the roots of the transfer function to determine the poles of T(s) are too complex. A design tool is available for the NCP102 allowing the user to evaluate the system response. The design tool can be downloaded at www.onsemi.com.

DESIGN EXAMPLE

The flexibility of the NCP102 is demonstrated by designing a 1.2 V/3.0 A voltage regulator using the NCP102 design tool. The input and supply voltages selected are typically found in computing mother board applications. The regulator specifications are listed in Table 1.

Table 1. Design Specifications

Parameter	Symbol	Min	Max
Input Voltage	V_{in} (V)	1.8 (±2%)	
Output Voltage	V_{out} (V)	1.2 (±2%)	
Output Current	I_{out} (A)	0.3	3.0
Ambient Temperature	T_A (°C)	–	50
Supply Voltage	V_{CC} (V)	5 V (±5%)	
Derating Factor	–	90 %	

DESIGN PROCEDURE

External MOSFET:

The 1st step in the regulator design is to select the external pass transistor. The output and supply voltages as well as MOSFET gate−to−source threshold voltage, V_{th}, need to be considered. The MOSFET threshold voltage, V_{th}, should be less than V_{CC} minus V_{out} as given by Equation 5.

$$V_{th} \le V_{CC} - V_{out} \quad \text{(eq. 5)}$$

Solving 5 using the design specifications, V_{th} should be less than 3.8 V. The next step is to calculate the power dissipation, P_D, of the external MOSFET. The power

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dissipation is calculated using Equation 6 and the maximum junction temperature, T_J, using Equation 7.

$$P_D = (V_{in} - V_{out}) \cdot I_{out} \quad \text{(eq. 6)}$$

$$T_J = P_D \cdot R_{\theta JA} + T_A \quad \text{(eq. 7)}$$

where, $R_{\theta JA}$ is the junction to ambient thermal resistance (in °C/W) of the external MOSFET. The NCP102 design tool automatically calculates the power dissipation and junction temperature.

Using $R_{\theta JA}$ doesn't always result in accurate junction temperature calculations as $R_{\theta JA}$ depends on the board layout. Alternatively, T_J can be calculated using the junction to case thermal resistance, $R_{\theta JC}$, and measuring the case temperature (T_C). Equation 8 relates the T_J to $R_{\theta JC}$.

$$T_J = P_D \cdot R_{\theta JC} + T_C \quad \text{(eq. 8)}$$

ON Semiconductor's NTD40N03 is used in this design. It has a V_{th} of 2.0 V, an $R_{\theta JA}$ of 71.4°C/W and an $R_{\theta JC}$ of 3°C/W. Using $R_{\theta JA}$ and the maximum ambient temperature a T_J of 178°C is calculated. That is slightly higher than the maximum junction temperature of the device and exceeds the derating factor. As $R_{\theta JA}$ provided in the NTD40N03 datasheet is for a specific layout, we will evaluate the board at full load and use $R_{\theta JC}$ to calculate T_J. It will be shown that the junction temperature meets the derating factor. This board provides a place holder for a parallel MOSFET (Q2) allowing the user to spread the power dissipation if needed.

Transconductance is the ratio of output current to the input voltage. In a MOSFET, it is the ratio of drain current (I_D) to gate−to−source voltage (V_{GS}) as given by Equation 9.

$$gm = \frac{\Delta I_D}{\Delta V_{GS}} \quad \text{(eq. 9)}$$

Referring to the NTD40N03R datasheet, the transconductance is calculated using the On−Region Characteristics Curve (Figure 1). Let's calculate the transconductance for a V_{DS} of 0.5 V with a V_{GS} variation from 2.8 V to 3 V. The drain current at 2.8 V is ~1.8 A and at 3 V it is approximately 3.8 A. Using these values a transconductance of 10 is calculated.

The gate−to−source, C_{GS}, and drain−to−source, C_{DS}, capacitances are needed for the frequency response analysis. The capacitances are calculated from the Capacitance Variation curve on the NTD40N03R datasheet. C_{rss} is the gate−to−drain capacitance. C_{iss} is the sum of C_{GS} and C_{GD}. C_{oss} is the sum of C_{DS} and C_{GD}. Referring to the Capacitance Variation curve, C_{rss} is approximately 150 pF, C_{iss} is approximately 700 pF and C_{oss} is approximately 600 pF at a V_{DS} of 0.5 V, resulting in a C_{DS} of 450 pF and a C_{GS} of 550 pF.

Output Capacitor:

The next step is to select the output capacitor. It is very common to use an electrolytic capacitor for bulk storage and a ceramic capacitor for high frequency bypass. However, the capacitors need to be carefully selected as they affect the stability of the system.

An electrolytic capacitor has high capacitance and high ESR resulting in a zero at a low frequency (typically below 1 kHz) and a dominant pole at a higher frequency. The ceramic capacitor has very low ESR placing a zero at a high frequency. If the ceramic capacitor capacitance is large (above 4.7 μF) the resulting zero may be in the crossover frequency range and thus affect the stability of the system.

This design uses a 1000 μF electrolytic capacitor with an ESR of 212 mΩ and a 4.7 μF ceramic in parallel.

Resistor Divider:

The output voltage is sampled by resistor divider R1 and R2. The node between the resistors must equal the reference voltage (0.8 V) at the desired output voltage. Using the design tool, the user arbitrarily selects a value for R2 and the tool suggests a value for R1. The user can override the suggested R1 value. In this design, R2 is set at 20 kΩ and R1 at 10 kΩ.

Frequency Response:

The NCP102 design tool simplifies the frequency response analysis of the regulator. It is a good tool to evaluate the interaction between the components and approximate the cross over frequency. However, it does not take into account 2nd order effects such as transconductance variations with load current. The simulated frequency response of the regulator at minimum load is shown in Figure 4.

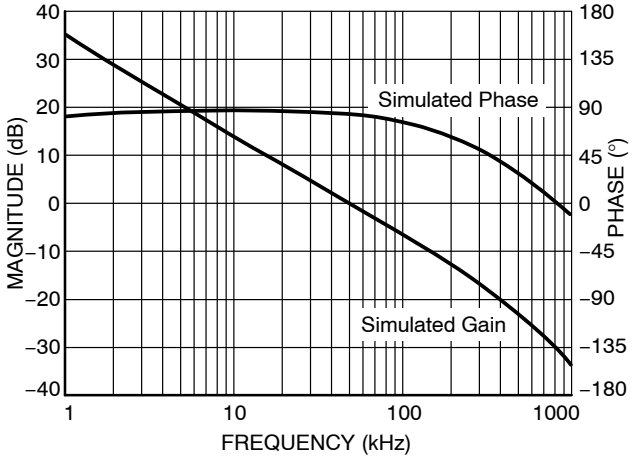

Figure 4. Simulated Frequency Response

The approximate crossover frequency is 50 kHz with a phase margin of 85°.

Soft−Start:

Soft−start slowly increases the regulator output voltage reducing stress during power up. The NCP102 implements soft−start by slowly charging the soft−start capacitor (C_{SOFT-S}) with a fixed current source (I_{SOFT-S}). The soft−start voltage is then used to control the dv−dt of the DRV pin. The soft−start period ends once the soft−start voltage reaches 0.8 V. Equation 10 is used to calculate the soft−start period.

$$t_{SOFT-S} = \frac{C_{SOFT-S} \cdot 0.8\ V}{I_{SOFT-S}} \quad \text{(eq. 10)}$$

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The design tool calculates the soft−start capacitor based on the user provided soft−start period. The user can override the suggested soft−start capacitor value and the tool calculates the soft−start period based on the provided capacitor value. This design uses a 0.1 μF soft−start capacitor for a 16 ms period.

BOARD LAYOUT

The regulator is built to validate the design using a 2 layer FR4 board having 1 oz copper plating. The board size is 3.5 in. x 3.2 in. Test points are provided for the Enable, DRV, Soft−Start, FB, V_{in}, V_{out} signals.

During the layout process care was taken to:

1. Minimize trace length, especially for high current loops.
2. Use wide traces for high current connections.
3. Use a single ground connection.
4. Place decoupling capacitors close to the NCP102 and board terminals.
5. Sense output voltage at the output connector to improve load regulation.

The top layer is shown in Figure 5 and the bottom layer is shown in Figure 6. The top layer shows the component location.

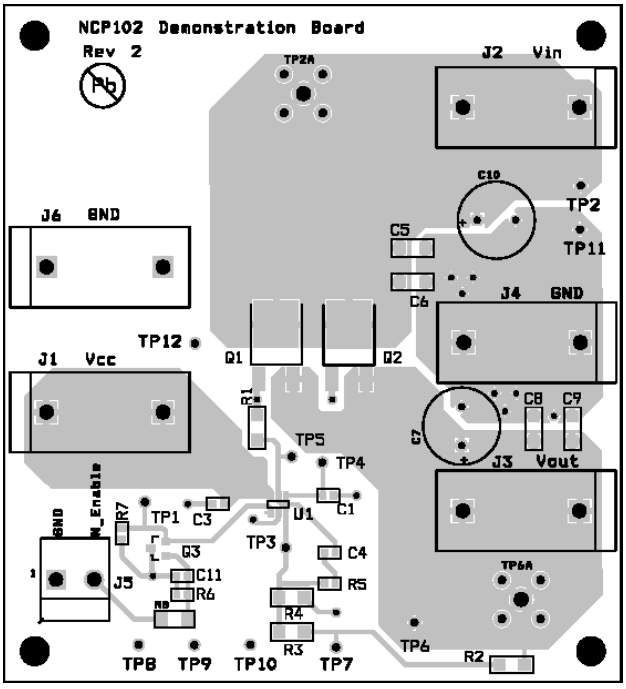

Figure 5. Layer 1 (Top)

The layout files may be available. Please contact your sales representative for availability.

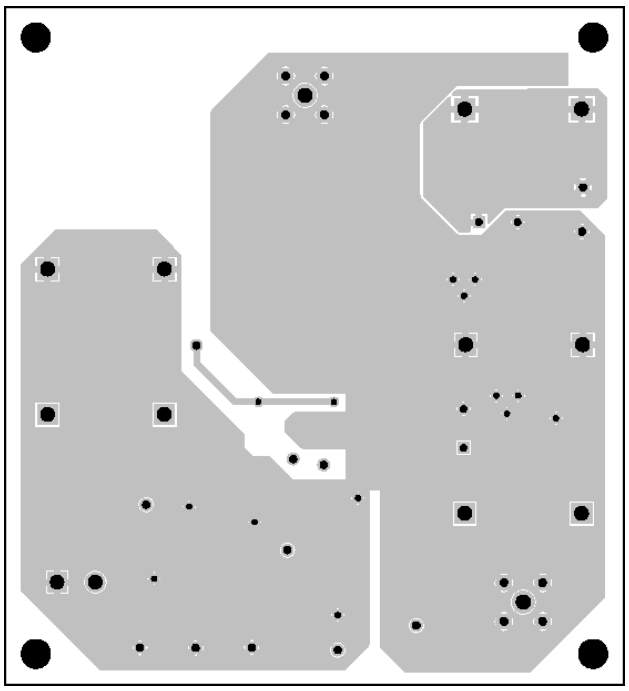

Figure 6. Layer 2 (Bottom)

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DESIGN VALIDATION

The circuit schematic is shown in Figure 7 and the bill of materials is shown in Table 2.

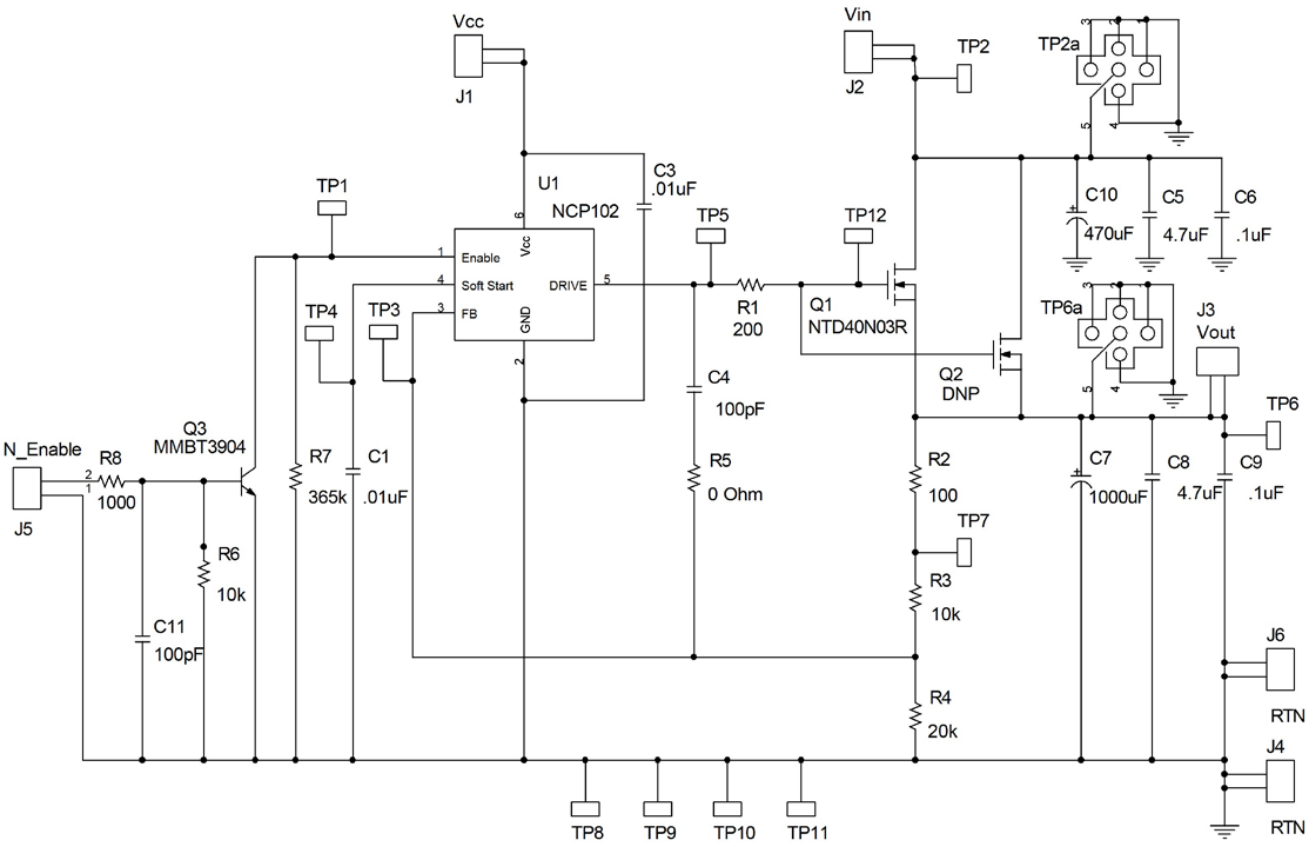

Figure 7. Circuit Schematic

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Table 2. BILL OF MATERIALS

Designator	Qty	Description	Value	Tolerance	Footprint	Manufacturer	Manufacturer Part Number	Substitutions Allowed	Lead Free
C1, C3	2	Capacitor, Ceramic	.01 uF, 25 V (.01 uF, 50 V)	10%	0603	Vishay (TDK)	VJ0603Y103KXXA (C1608X7R1H103K)	Yes	Yes
C4, C11	2	Capacitor, Ceramic	100 pF, 25 V (100 pF, 50 V)	5%	0603	Vishay (TDK)	VJ0603Y101KXXA (C1608C0G1H101J)	Yes	Yes
C5, C8	2	Capacitor, Ceramic	4.7 uF, 16 V	10%	1206	TDK	C3216X5R1C475K	Yes	Yes
C6, C9	2	Capacitor, Ceramic	.1 uF, 25 V	10%	1206	Vishay (TDK)	VJ1206Y104KXXA (C3216CH1E104J)	Yes	Yes
C7	1	Capacitor, Aluminum Electrolytic	1000 uF, 25 V	20%	Radial Lead	United-Chemicon	ESMG250ELL102MJ20S	No	Yes
C10	1	Capacitor, Aluminum Electrolytic	470 uF, 25 V	20%	Radial Lead	United-Chemicon	ESMG250ELL471MJC5S	Yes	Yes
Q1	1	Power MOSFET, N-Channel	45 A, 25 V	n/a	D-Pack	ON Semiconductor	NTD40N03R	No	Yes
Q2		Do Not Place		n/a	D-Pack		Do Not Place	Yes	
Q3	1	Transistor, Sm Signal, NPN	200 mA, 40 V	n/a	SOT-23	ON Semiconductor	MMBT3904LT1G	Yes	Yes
R1	1	Resistor, Thick Film	200 Ω, 0.25 W	1%	1206	Vishay	CRCW1206200RF	Yes	Yes
R2	1	Resistor, Thick Film	100 Ω, 0.25 W	1%	1206	Vishay	CRCW1206100RF	Yes	Yes
R3	1	Resistor, Thick Film	10 kΩ, 0.25 W	1%	1206	Vishay	CRCW12061002F	Yes	Yes
R4	1	Resistor, Thick Film	20 kΩ, 0.25 W	1%	1206	Vishay	CRCW12062002F	Yes	Yes
R5	1	Resistor, Thick Film	0 Ω, 0.1 W		0603	Vishay	CRCW06030R00F, or CRCW06030000Z0	Yes	Yes
R6	1	Resistor, Thick Film	10 kΩ, 0.1 W	1%	0603	Vishay	CRCW06031002F	Yes	Yes
R7	1	Resistor, Thick Film	365 kΩ, 0.1 W	1%	0603	Vishay	CRCW06033653F	Yes	Yes
R8	1	Resistor, Thick Film	1000 Ω, 0.25 W	1%	1206	Vishay	CRCW12061001F	Yes	Yes
U1	1	Controller, Low Dropout Linear Regulator			TSOP-6	ON Semiconductor	NCP102G	No	Yes
C2		Not Used							
Hardware									
H1	1	Printed Circuit Board			3.5” x 3.2” x 0.062”	Circuit Express, Inc.	NCP102_DEMOBD	Yes	Yes
J1	1	Banana Jack, 4 mm Socket, Brown, Horizontal Mt.	10 ADC	n/a	10.5mm x 23.5mm x 12.4mm; 15.3mm lead pitch	Deltron Emcon	571-0300	Yes	Yes
J2	1	Banana Jack, 4 mm Socket, Red, Horizontal Mt.	10 ADC	n/a	10.5mm x 23.5mm x 12.4mm; 15.3mm lead pitch	Deltron Emcon	571-0500	Yes	Yes
J3	1	Banana Jack, 4 mm Socket, Yellow, Horizontal Mt.	10 ADC	n/a	10.5mm x 23.5mm x 12.4mm; 15.3mm lead pitch	Deltron Emcon	571-0700	Yes	Yes
J4, J6	2	Banana Jack, 4 mm Socket, Black, Horizontal Mt.	10 ADC	n/a	10.5mm x 23.5mm x 12.4mm; 15.3mm lead pitch	Deltron Emcon	571-0100	Yes	Yes

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Table 2. BILL OF MATERIALS

Desig-nator	Qty	Description	Value	Toler-ance	Footprint	Manufacturer	Manufacturer Part Number	Substi-tutions Allowed	Lead Free
J5	1	Terminal Block, 2 Pole, Side Entry	300 V, 16 A	n/a	10mm x 10mm x 13.5mm; 5mm lead pitch		DigiKey ED1930-ND, or equiv	Yes	Yes
TP1	1	Test Point, Brown			.18”ht x .05”dia eyelet	Components Corporation	TP-015-01-01	Yes	Yes
TP2	1	Test Point, Red			.18”ht x .05”dia eyelet	Components Corporation	TP-015-01-02	Yes	Yes
TP3	1	Test Point, Orange			.18”ht x .05”dia eyelet	Components Corporation	TP-015-01-03	Yes	Yes
TP4	1	Test Point, Yellow			.18”ht x .05”dia eyelet	Components Corporation	TP-015-01-04	Yes	Yes
TP5	1	Test Point, Green			.18”ht x .05”dia eyelet	Components Corporation	TP-015-01-05	Yes	Yes
TP6	1	Test Point, Blue			.18”ht x .05”dia eyelet	Components Corporation	TP-015-01-06	Yes	Yes
TP7	1	Test Point, Violet			.18”ht x .05”dia eyelet	Components Corporation	TP-015-01-07	Yes	Yes
TP8, TP9, TP10, TP11	4	Test Point, Black			.18”ht x .05”dia eyelet	Components Corporation	TP-015-01-00	Yes	Yes
TP12	1	Test Point, Gray			.18”ht x .05”dia eyelet	Components Corporation	TP-015-01-08	Yes	Yes
TP6a, TP2a	2	3.5 mm dia Probe Adapter				Tektronix	131-5031-00 (pkg of 25)	Yes	Yes

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The final step is to verify the board performance. The evaluation criteria include step load and power up responses, load regulation, stability and power dissipation.

Dynamic Response:

The dynamic response of the regulator is evaluated stepping the load current from 10% to 100% and from 100% to 10% of the rated output current. The step load responses are shown in Figure 8.

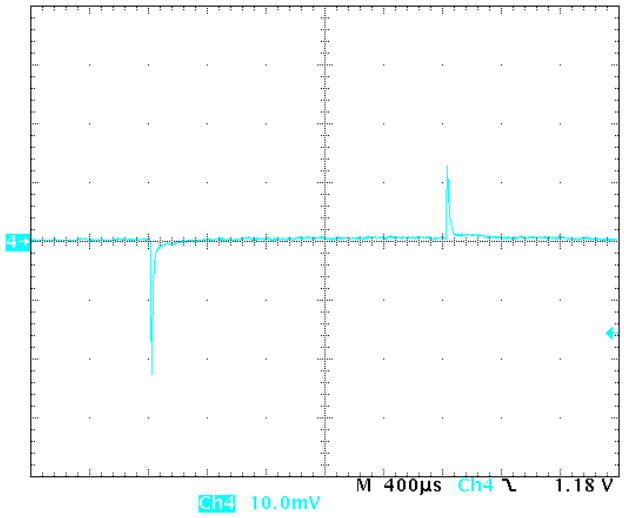

Figure 8. Output Voltage Response to a Step Load from 0.3 A to 3.0 A to 0.3 A

The output voltage stays within the 2% tolerance limit. The initial drop on the output voltage as a higher load is applied is mostly dependent on the output capacitor and not on the loop response of the system. No ringing is observed, indicating an adequate phase margin.

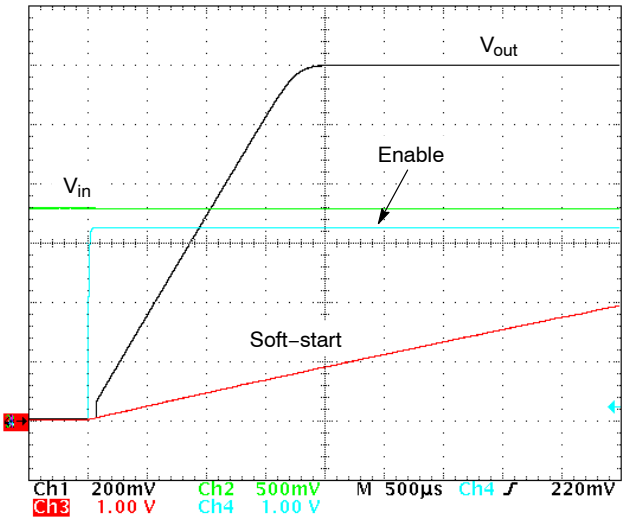

Figure 9. Output Voltage During Power Up at Minimum Load

Startup:

The startup behavior of the regulator is evaluated at minimum and maximum load enabling the controller using the enable pin while V_{in} and V_{CC} are already high. The startup waveforms at minimum and maximum load are shown in Figure 9 and 10, respectively.

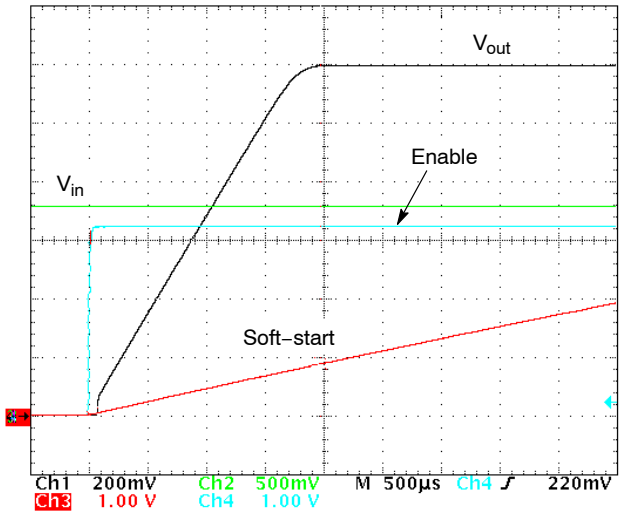

Figure 10. Output Voltage During Power Up at Maximum Load

Line and Load Regulation:

Line and load regulation are calculated using Equations 11 and 12, respectively. Line regulation is measured at 0.1% and load regulation is measured at 0.067%. The output voltage vs. input voltage and output load is shown in Figure 11.

$$Reg_{(line)} = \frac{\Delta V_{out}}{\Delta V_{in}} \quad \text{(eq. 11)}$$

$$Reg_{(load)} = \frac{V_{out(no\ load)} - V_{out(full\ load)}}{V_{out(no\ load)}} \quad \text{(eq. 12)}$$

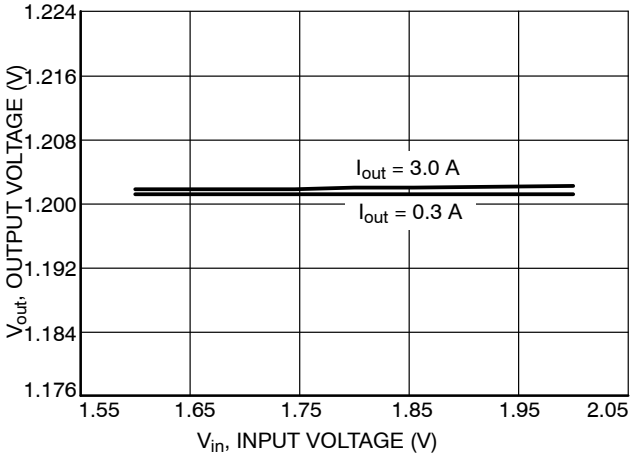

Figure 11. Output Voltage Response to Input Voltage and Output Load Variations

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Frequency Response:

The open loop response is measured by injecting an AC signal across R2 using a network analyzer and an isolation transformer. The measured and calculated open loop responses at minimum load are shown in Figure 12. The measured crossover frequency is 58 kHz with a phase margin of 70°. A good correlation is observed between simulated and calculated responses up to around 200 kHz.

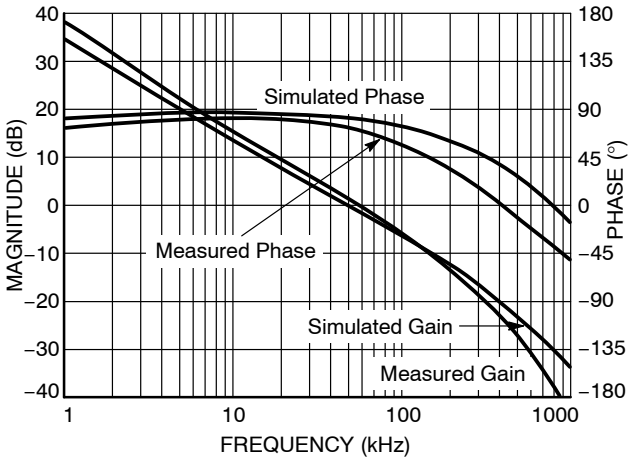

Figure 12. Measured and Calculated Open Loop Frequency Responses

Power Dissipation:

This demo board is designed to operate with no airflow. However, in most desktop computing applications airflow will be present. The thermal performance of the board is evaluated using an infrared camera. Figure 13 shows the thermal image of the board at maximum output load.

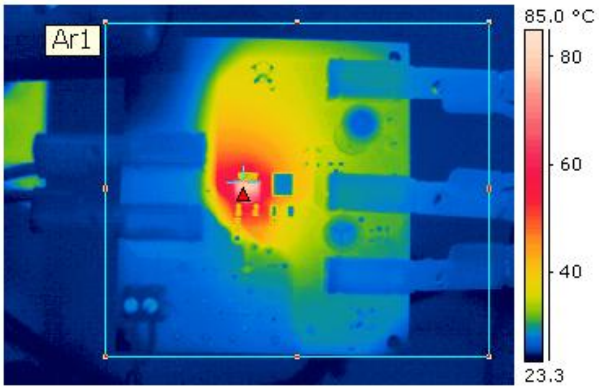

Figure 13. Thermal Image of the Board at Maximum Load

As expected, the hottest component on the board is the external pass transistor. The case temperature is measured at 78.4°C at room temperature. Using Equation 8, the junction temperature is calculated at 84°C. The maximum junction temperature is calculated at 109°C assuming a 25°C temperature delta between room and maximum ambient temperatures. A junction temperature of 109°C meets our derating guidelines.

The thermal performance of the board can be optimized by using a heatsink, increasing the number of external pass transistors (Q1 & Q2) pad area, increasing the copper weight of the board or using an additional pass transistor.

SUMMARY

A 1.2 V regulator is designed and built using the NCP102. The regulator has excellent line and load regulation with better than ±2% output voltage regulation.

The regulator provides excellent transient response. Phase margin and crossover frequency are measured at 70° and 58 kHz, respectively.

REFERENCES

1. Tod Schiff, “Stability in High Speed Linear LDO Regulator,” AND8037/D, www.onsemi.com.

2. Low Dropout Linear Regulator Controller Datasheet NCP102, www.onsemi.com.

3. Power MOSFET 45 A, 25 V Datasheet NTD40N03R, www.onsemi.com

TEST PROCEDURE FOR THE NCP102 EVALUATION BOARD

Required Equipment

- 3 DC Power Supplies:
  - “Vin supply” possessing a minimum voltage rating of 5 VDC and minimum current rating of 4 ADC; for example, HP 6282A.
  - “Vcc supply” possessing a minimum voltage rating of 15 VDC and minimum current rating of 1 ADC; for example, 1/2 Agilent e3649A dual supply.
  - “N_Enable supply” possessing a minimum voltage rating of 5.5 VDC and minimum current rating of 0.1 ADC; for example, 1/2 Agilent e3649A dual supply.
- 3 Auto-ranging Digital Multimeters (DMMs): each possessing a minimum voltage rating of 20 VDC and minimum current rating of 2ADC; for example, Keithley 175.
- 1 Electronic Load: possessing a current display and minimum current capability of 4 ADC; for example, Kikusui PLZ303W.

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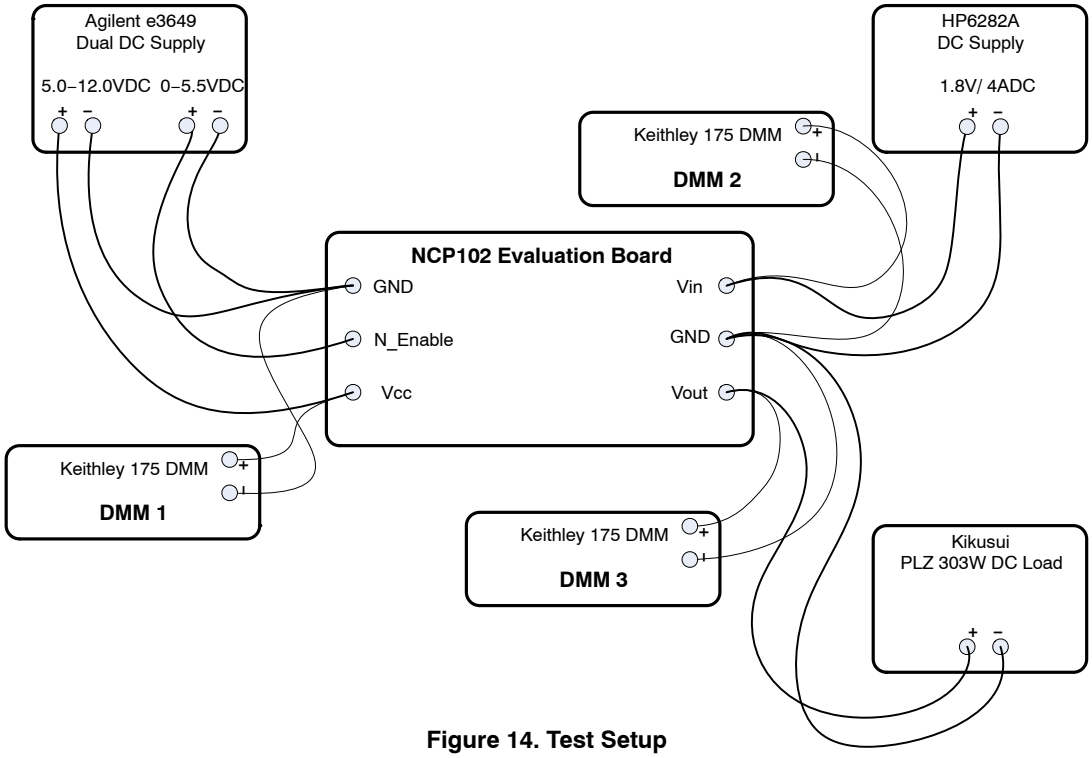

Figure 14. Test Setup

Test Procedure

- Establish Setup
  1. Connect the NCP102 Evaluation Board as shown in Figure 14.
  2. Adjust the N_Enable supply to 4.5 VDC while observing the indicator on the supply.

NOTE: for measurement accuracy, the DMMs must be connected to the Evaluation Board terminals and not the DC supply or load terminals. This is particularly true for DMM 2 and DMM 3.

  3. Connect DMM 1 to Vcc and configure as a voltmeter. Set DMM 1for auto-range.
  4. Connect DMM 2 to Vin and configure as a voltmeter. Set DMM 2 for auto-range.
  5. Connect DMM 3 to Vout and configure as a voltmeter. Set DMM 3 for auto-range.
  6. Adjust the Vcc supply to 5.0 VDC while observing DMM 1 (not the indicator on the DC supply).
  7. Adjust the Vin supply to 1.800 VDC while observing DMM 2 (not the indicator on the DC supply).
  8. Disable the electronic load so that it is neither sinking nor sourcing current.

- No-Load Regulation and Enable Function
  1. Verify that Vout (DMM 3) equals zero VDC.
  2. Temporarily disconnect the banana cable connected to “N_Enable”, or reduce the “N_Enable” supply to zero Volts.
  3. Verify that Vin (DMM 2) equals 1.800 VDC, ±2% (1.764 VDC to 1.836 VDC).
  4. Readjust the Vin supply if necessary.
  5. Verify that Vout (DMM 3) equals 1.200 VDC, ±2% (1.176 VDC to 1.224 VDC).
  6. Reconnect the banana cable to “N_Enable”, or adjust the “N_Enable” supply output to 4.5 VDC.
  7. If Vcc= 12.0 VDC (DMM 1), go to *Full-Load Regulation and Enable Function*, below.
  8. Adjust the Vcc supply to 12.0 VDC, as indicated on DMM 1.
  9. Repeat steps 1 through 7 of this section.

- Full-Load Regulation and Enable Function
  1. While observing the front panel indicator on the electronic load, adjust it to sink 3.5 ADC from the demonstration board Vout terminal.
  2. Enable the electronic load.
  3. Verify that Vout (DMM 3) equals zero VDC.
  4. Temporarily disconnect the banana cable connected to “N_Enable”, or reduce the “N_Enable” supply to zero Volts.
  5. Verify that Vin (DMM 2) equals 1.800 VDC, ±2% (1.764 VDC to 1.836 VDC).
  6. Readjust the Vin supply if necessary.
  7. Verify that Vout (DMM 3) equals 1.200VDC, ±2% (1.176 VDC to 1.224 VDC).
  8. Reconnect the banana cable to “N_Enable”, or adjust the “N_Enable” supply output to 4.5 VDC.
  9. If Vcc= 5.0 VDC (DMM 1), go to Step 12.
  10. Adjust the Vcc supply to 5.0VDC, as indicated on DMM 1.
  11. Repeat steps 1 through 9 of this section.
  12. Verify that Vout (DMM 3) equals zero VDC.
  13. Test complete.

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