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# 3-State Octal D-Type Edge-Triggered Flip-Flop

The MM74HC574 high speed octal D-type flip-flops utilize advanced silicon-gate P-well CMOS technology. They possess the high noise immunity and low power consumption of standard CMOS integrated circuits, as well as the ability to drive 15 LS-TTL loads. Due to the large output drive capability and the 3-STATE feature, these devices are ideally suited for interfacing with bus lines in a bus organized system.

These devices are positive edge triggered flip—flops. Data at the D inputs, meeting the set—up and hold time requirements, are transferred to the Q outputs on positive going transitions of the CLOCK (CK) input. When a high logic level is applied to the OUTPUT CONTROL (OC) input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

The 74HC logic family is speed, function, and pinout compatible with the standard 74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

#### **Features**

• Typical Propagation Delay: 18 ns

• Wide Operating Voltage Range: 2 V – 6 V

• Low Input Current: 1 μA Maximum

• Low Quiescent Current: 80 µA Maximum

• Compatible with Bus-oriented Systems

• Output Drive Capability: 15 LS-TTL Loads

#### MAXIMUM RATINGS (Note 1)

Rating	Symbol	Value	Unit
Supply Voltage	V <sub>CC</sub>	-0.5 to + 7.0 V	V
DC Input Voltage	V <sub>IN</sub>	–1.5 to V <sub>CC</sub> + 1.5 V	V
DC Output Voltage	V <sub>OUT</sub>	–0.5 to V <sub>CC</sub> + 0.5 V	V
Clamp Diode Current	$I_{IK}$ , $I_{OK}$	±20	mA
DC Output Current, per pin	I <sub>OUT</sub>	±35	mA
DC V <sub>CC</sub> or GND Current, per pin	I <sub>CC</sub>	±70	mA
Storage Temperature Range	T <sub>STG</sub>	-65 to +150	°C
Power Dissipation (Note 2) S.O. Package only	P <sub>D</sub>	600 500	mW
Lead Temperature (Soldering 10 s)	TL	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Unless otherwise specified all voltages are referenced to ground.

 Power Dissipation temperature derating — plastic "N" package: – 12 mW/°C from 65°C to 85°C.



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SOP20 SJ SUFFIX CASE 565BG



TSSOP20 MTC SUFFIX CASE 948AQ



PDIP20 N SUFFIX CASE 646AC



SOIC20 WM SUFFIX CASE 751BJ

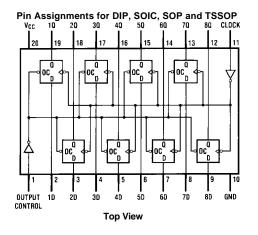
#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

## **ORDERING CODE**

Order Number	Package Number	Package Description
MM74HC574WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
MM74HC574SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3 mm Wide
MM74HC574MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4 mm Wide
MM74HC574N	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

# **Connection Diagram**



# **Truth Table**

Output Control	Clock	Data	Output
L	1	Н	Н
L	1	L	L
L	L	Х	$Q_0$
Н	X	Х	Z

H = HIGH Level

L = LOW Level

X = Don't Care

↑ = Transition from Low-to-HIGH

Z = High Impedance State

Q0 = The level of the output before steady state input conditions were established

## **RECOMMENDED OPERATING CONDITIONS**

Symbol	Characteristic	Min	Тур	Max	Units
V <sub>CC</sub>	Supply Voltage	2		6	V
V <sub>IN</sub> , V <sub>OUT</sub>	DC Input or Output Voltage	0		V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature Range	<b>-</b> 55		+125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise or Fall Times $ \begin{array}{c} V_{CC} = 2.0 \ V \\ V_{CC} = 4.5 \ V \\ V_{CC} = 6.0 \ V \\ \end{array} $			1000 500 400	ns

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

## DC ELECTRICAL CHARACTERISTICS (Note 3)

				T <sub>A</sub> =	25°C	T <sub>A</sub> = -40 to 85°C	T <sub>A</sub> = -55 to 125°C	
Symbol	Parameter	Conditions	V <sub>CC</sub>	Тур		Guaranteed L	imits	Units
V <sub>IH</sub>	Minimum HIGH Lev- el Input Voltage		2.0 V 4.5 V 6.0 V		1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V <sub>IL</sub>	Maximum LOW Lev- el Input Voltage		2.0 V 4.5 V 6.0 V		0.5 1.35 1.8	0.5 1.35 1.8	0.5 1.35 1.8	V
V <sub>OH</sub>	Minimum HIGH Lev- el Output Voltage	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $ I_{OUT}  \le 20 \mu\text{A}$	2.0 V 4.5 V 6.0 V	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{IN} = V_{IH} \text{ or } V_{IL}$ $\begin{vmatrix} I_{OUT} \end{vmatrix} \le 6.0 \text{ mA}$ $\begin{vmatrix} I_{OUT} \end{vmatrix} \le 7.8 \text{ mA}$	4.5 V 6.0 V	4.2 5.7	3.98 5.48	3.84 5.34	3.7 5.2	V
V <sub>OL</sub>	Maximum LOW Lev- el Output Voltage	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $ I_{OUT}  \le 20  \mu\text{A}$	2.0 V 4.5 V 6.0 V	0 0 0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{IN} = V_{IH} \text{ or } V_{IL}$ $\begin{vmatrix} I_{OUT} \end{vmatrix} \le 6.0 \text{ mA}$ $\begin{vmatrix} I_{OUT} \end{vmatrix} \le 7.8 \text{ mA}$	4.5 V 6.0 V	0.2 0.2	0.26 0.26	0.33 0.33	0.4 0.4	V
I <sub>IN</sub>	Maximum Input Cur- rent	$V_{IN} = V_{CC}$ or GND	6.0 V		±0.1	±1.0	±1.0	μΑ
loz	Maximum 3-STATE Output Leakage Current	V <sub>OUT</sub> = V <sub>CC</sub> or GND OC = V <sub>IH</sub>	6.0 V		±0.5	±5.0	±10	μΑ
I <sub>CC</sub>	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND $I_{OUT} = 0 \mu A$	6.0 V		8.0	80	160	μΑ
$\Delta I_{CC}$	Quiescent Supply	V <sub>CC</sub> = 5.5 V	OE	1.0	1.5	1.8	2.0	mA
	Current per Input Pin	V <sub>IN</sub> = 2.4 V or 0.4 V (Note 3)	CLK	0.6	0.8	1.0	1.1	
			DATA	0.4	0.5	0.6	0.7	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product

# AC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C, $t_f$ = $t_f$ = 6 ns)

Symbol	Parameter	Conditions	Тур	Guaranteed Limit	Units
f <sub>MAX</sub>	Maximum Operating Frequency		60	33	MHz
t <sub>PHL</sub> , t <sub>PLH</sub>	Maximum Propagation Delay, Clock to Q	C <sub>L</sub> = 45 pF	17	27	ns
t <sub>PZH</sub> , t <sub>PZL</sub>	Maximum Output Enable Time	$R_L = 1 \text{ k}\Omega, C_L = 45 \text{ pF}$	19	28	ns
t <sub>PHZ</sub> , t <sub>PLZ</sub>	Maximum Output Disable Time	$R_L = 1 \text{ k}\Omega, C_L = 5 \text{ pF}$	14	25	ns
t <sub>S</sub>	Minimum Setup Time, Data to Clock		10	12	ns
t <sub>H</sub>	Minimum Hold Time, Clock to Data		-3	5	ns
t <sub>W</sub>	Minimum Pulse Clock Width		8	15	ns

performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. For a power supply of 5 V ±10% the worst–case output voltages (V<sub>OH</sub>, and V<sub>OL</sub>) occur for HC at 4.5 V. Thus the 4.5 V values should be used when designing with this supply. Worst–case V<sub>IH</sub> and V<sub>IL</sub> occur at V<sub>CC</sub> = 5.5 V and 4.5 V respectively. (The V<sub>IH</sub> value at 5.5 V is 3.85 V.) The worst–case leakage current (I<sub>IN</sub>, I<sub>CC</sub>, and I<sub>OZ</sub>) occur for CMOS at the higher voltage and so the 6.0 V values should be used.

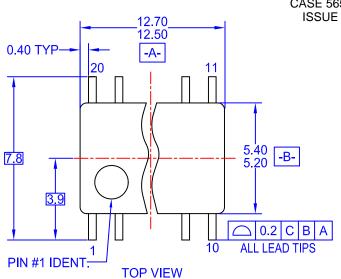
# $\textbf{AC ELECTRICAL CHARACTERISTICS} \ (\text{V}_{CC} = 2.0 - 6.0 \ \text{V}, \ C_L = 50 \ \text{pF}, \ t_f = t_f = 6 \ \text{ns} \ \text{unless otherwise specified})$

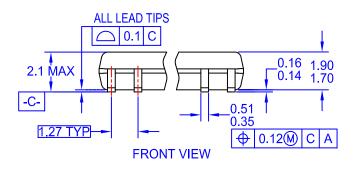
				T <sub>A</sub> =	25°C	$T_A = -40 \text{ to } 85^{\circ}\text{C}$	T <sub>A</sub> = -55 to 125°C	
Symbol	Parameter	Conditions	V <sub>CC</sub>	Тур		Guaranteed L	imits	Units
f <sub>MAX</sub>	Maximum Operating Frequency	C <sub>L</sub> = 50 pF	2.0 V 4.5 V 6.0 V		33 30 35	28 24 28	23 20 23	MHz
t <sub>PHL</sub> , t <sub>PLH</sub>	Maximum Propagation Delay, Clock to Q	C <sub>L</sub> = 50 pF C <sub>L</sub> = 150 pF	2.0 V 2.0 V	18 51	30 155	38 194	45 233	ns
	Clock to Q	C <sub>L</sub> = 50 pF C <sub>L</sub> = 150 pF	4.5 V 4.5 V	13 19	23 31	29 47	35 47	ns
		C <sub>L</sub> = 50 pF C <sub>L</sub> = 150 pF	6.0 V 6.0 V	12 18	20 27	25 34	30 41	ns
t <sub>PZH</sub> , t <sub>PZL</sub>	Maximum Output Enable Time	$R_L = 1 \text{ k}\Omega$ $C_L = 50 \text{ pF}$ $C_L = 150 \text{ pF}$	2.0 V 2.0 V	22 59	30 180	38 225	45 270	ns
		C <sub>L</sub> = 50 pF C <sub>L</sub> = 150 pF	4.5 V 4.5 V	14 20	28 36	35 45	42 54	ns
		C <sub>L</sub> = 50 pF C <sub>L</sub> = 150 pF	6.0 V 6.0 V	12 18	24 31	30 39	36 47	ns
t <sub>PHZ</sub> , t <sub>PLZ</sub>	Maximum Output Disable Time	$R_L = 1 \text{ k}\Omega$ $C_L = 50 \text{ pF}$	2.0 V 4.5 V 6.0 V	15 12 10	30 25 21	38 31 27	45 38 32	ns
t <sub>S</sub>	Minimum Setup Time Data to Clock		2.0 V 4.5 V 6.0 V	6	12 20 17	15 25 21	18 30 25	ns
t <sub>H</sub>	Minimum Hold Time Clock to Data		2.0 V 4.5 V 6.0 V	-1	5 0 0	6 0 0	8 0 0	ns
t <sub>THL</sub> , t <sub>TLH</sub>	Maximum Output Rise and Fall Time	C <sub>L</sub> = 50 pF	2.0 V 4.5 V 6.0 V	6 7 6	12 12 10	15 15 13	18 18 15	ns
t <sub>W</sub>	Minimum Clock Pulse Width		2.0 V 4.5 V 6.0 V	30 9 8	15 16 14	20 20 18	24 24 20	ns
t <sub>r</sub> , t <sub>f</sub>	Maximum Clock Input Rise and Fall Time		2.0 V 4.5 V 6.0 V		1000 500 400	1000 500 400	1000 500 400	ns
C <sub>PD</sub>		OC = V <sub>CC</sub> OC = GND		5 58				pF
C <sub>IN</sub>	Maximum Input Capacitance			5	10	10	10	pF
C <sub>OUT</sub>	Maximum Output Capacitance			15	20	20	20	pF

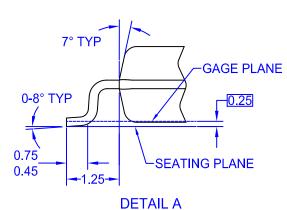
<sup>4.</sup> C<sub>PD</sub> determines the no load dynamic power consumption, P<sub>D</sub> = C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f + I<sub>CC</sub> V<sub>CC</sub>, and the no load dynamic current consumption, I<sub>S</sub> = C<sub>PD</sub> V<sub>CC</sub> f + I<sub>CC</sub>.

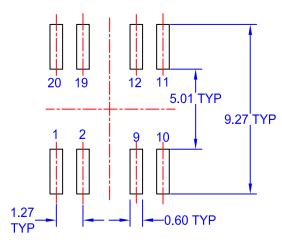
#### PACKAGE DIMENSIONS

### SOP20 CASE 565BG **ISSUE O**

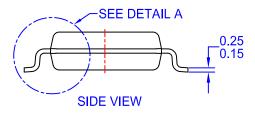








# LAND PATTERN RECOMMENDATION

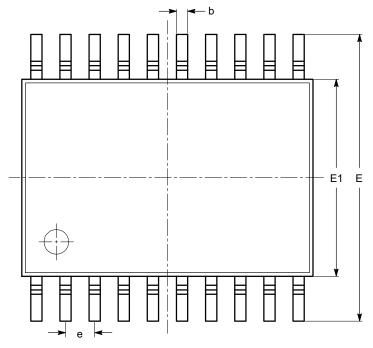


#### **NOTES:**

- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
  B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

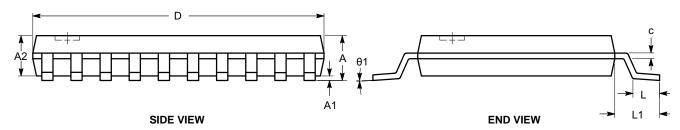
# **PACKAGE DIMENSIONS**

# TSSOP20, 4.4x6.5 CASE 948AQ-01 ISSUE A



SYMBOL	MIN	NOM	MAX		
А			1.20		
A1	0.05		0.15		
A2	0.80		1.05		
b	0.19		0.30		
С	0.09		0.20		
D	6.40	6.50	6.60		
Е	6.30	6.40	6.50		
E1	4.30	4.40	4.50		
е	0.65 BSC				
L	0.45	0.60	0.75		
L1	1.00 REF				
θ	0°		8°		

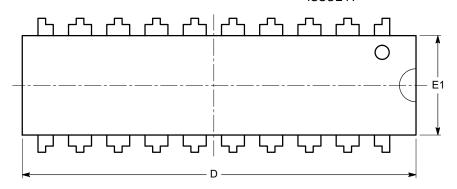
**TOP VIEW** 



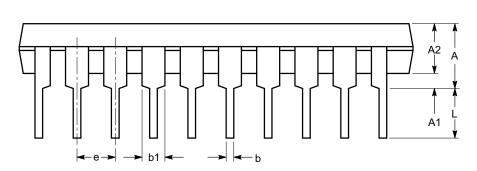
- (1) All dimensions are in millimeters. Angles in degrees.(2) Complies with JEDEC MO-153.

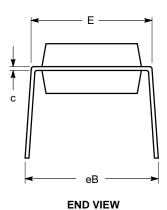
# **PACKAGE DIMENSIONS**

# PDIP-20, 300 mils CASE 646AC-01 ISSUE A



**TOP VIEW** 





SIDE VIEW

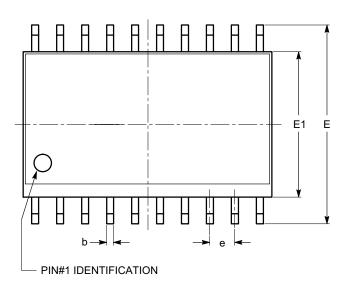
SYMBOL	MIN	NOM	MAX		
Α	3.56		5.33		
A1	0.38				
A2	2.92	3.30	4.95		
b	0.36	0.45	0.55		
b1	1.15	1.52	1.77		
С	0.21	0.26	0.35		
D	24.89	26.16	26.92		
Е	7.62	7.87	8.25		
E1	6.10	6.35	7.11		
е	2.54 BSC				
eB	7.88		10.92		
L	2.99	3.30	3.81		

### Notes:

- (1) All dimensions are in millimeters.
- (2) Complies with JEDEC MS-001.

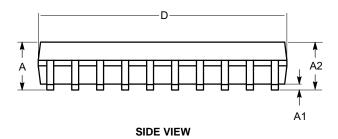
#### PACKAGE DIMENSIONS

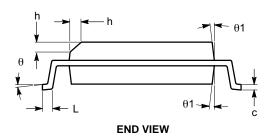
SOIC-20, 300 mils CASE 751BJ-01 ISSUE O



SYMBOL	MIN NOM		MAX		
А	2.36	2.49	2.64		
A1	0.10		0.30		
A2	2.05		2.55		
b	0.31	0.41	0.51		
С	0.20	0.27	0.33		
D	12.60	12.80	13.00		
Е	10.01	10.30	10.64		
E1	7.40	7.50	7.60		
е	1.27 BSC				
h	0.25		0.75		
L	0.40	0.81	1.27		
θ	0°		8°		
θ1	5°		15°		

#### **TOP VIEW**





#### Notes:

- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Complies with JEDEC MS-013.

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