ISP1302UK

USB On-The-Go transceiver

Rev. 03 — 29 September 2009 Product data sheet

1. General description

The ISP1302UK is a Universal Serial Bus (USB) On-The-Go (OTG) transceiver device. It is fully compliant with *Universal Serial Bus Specification Rev. 2.0* and *On-The-Go Supplement to the USB 2.0 Specification Rev. 1.3*. The ISP1302UK can transmit and receive serial data at full-speed (12 Mbit/s) and low-speed (1.5 Mbit/s) data rates.

The ISP1302UK is available in WLCSP25 package.

2. Features

- Fully complies with:
  - *Universal Serial Bus Specification Rev. 2.0*
  - *On-The-Go Supplement to the USB 2.0 Specification Rev. 1.3*
  - *On-The-Go Transceiver Specification (CEA-2011)*
- Can transmit and receive serial data at full-speed (12 Mbit/s) and low-speed (1.5 Mbit/s) data rates
- Supports OTG Host Negotiation Protocol (HNP) and Session Request Protocol (SRP)
- Supports I^2C-bus (up to 400 kHz) serial interface to access control and status registers
- Supports Universal Asynchronous Receiver-Transmitter (UART) pass-through on the DP and DM lines
- Supports service mode with 2.8 V UART signaling on the DP and DM lines
- Built-in charge pump regulator outputs 5 V at current up to 50 mA
- 3.0 V to 4.5 V power supply input range (V_{CC})
- Supports wide range digital interfacing I/O voltage ($V_{CC(I/O)}$) 1.4 V to 3.6 V
- Full industrial grade operation from –40 °C to +85 °C
- Available in small WLCSP25 halogen-free and lead-free package

3. Applications

- Mobile phones
- Digital camera
- Personal digital assistant

4. Ordering information

Table 1. Ordering information

Commercial product code	Package description	Packing	Minimum sellable quantity
ISP1302UKTS	WLCSP25; 25 bumps; 2.5 × 2.5 × 0.6 mm	7 inch tape and reel non-dry pack	3000 pieces

5. Block diagram

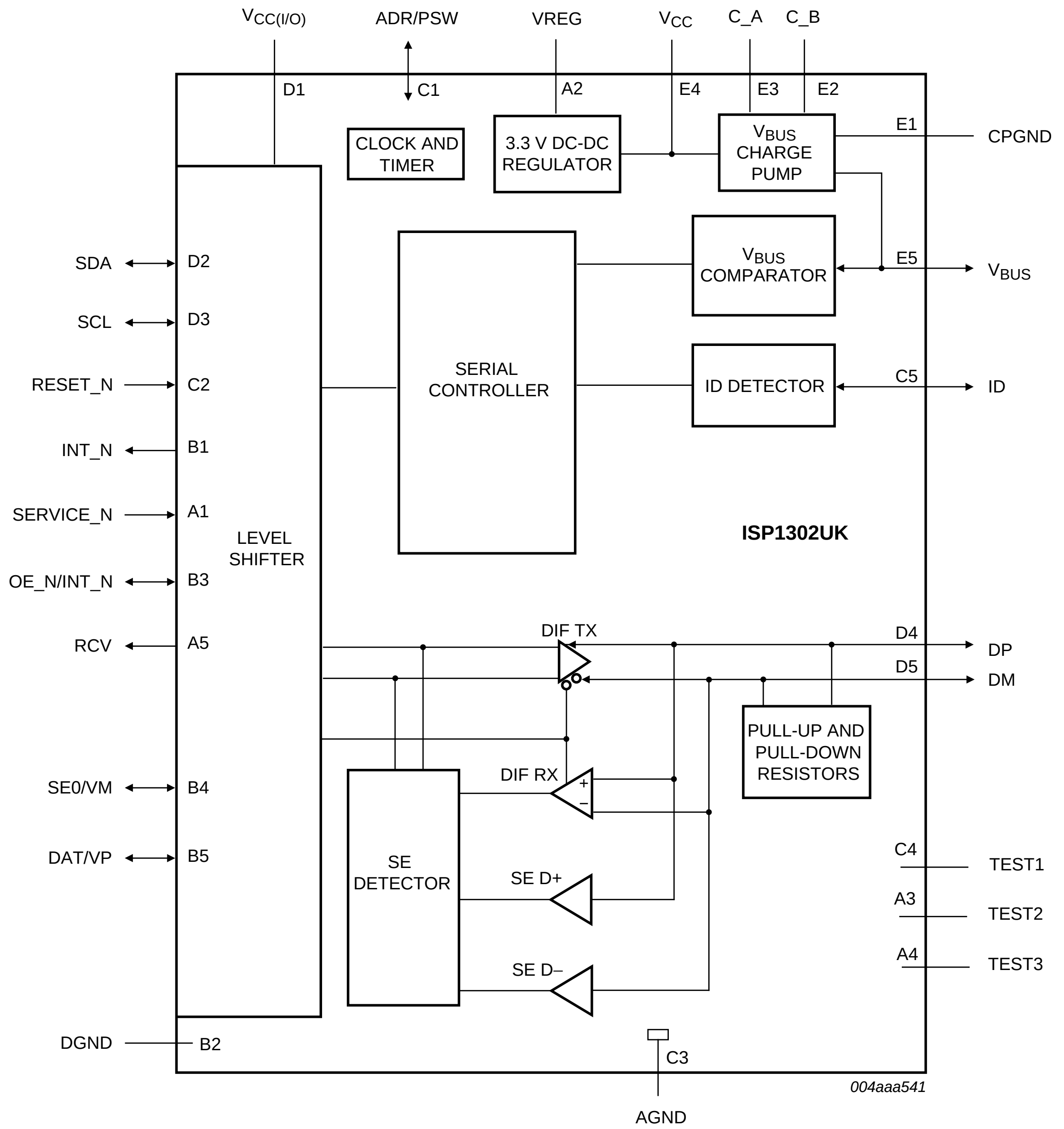


Fig 1. Block diagram

6. Pinning information

6.1 Pinning

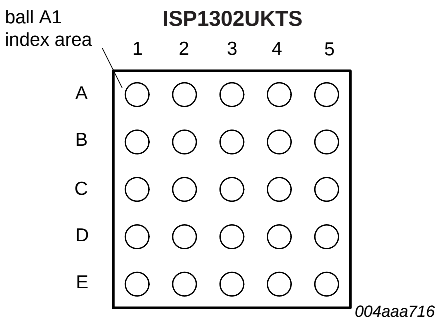


Fig 2. Pin configuration WLCSP25 (top view)

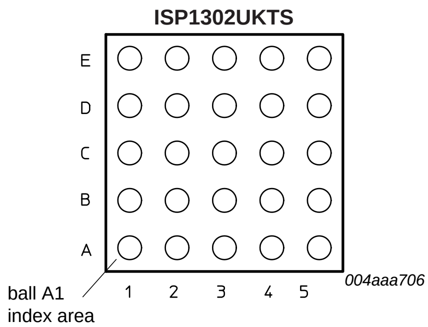


Fig 3. Pin configuration WLCSP25 (bottom view)

6.2 Pin description

Table 2. Pin description

Symbol[1]	Pin	Type[2]	Reset value	Description
SERVICE_N	A1	I	-	input; sets default operation mode of the ISP1302UK: • If a LOW is latched on reset (including power-on reset), default mode is UART with 2.8 V signaling. • If a HIGH is latched on reset (including power-on reset), default mode is USB with 3.3 V signaling. Operation mode can be changed after reset by changing the value of the Mode register bits.
VREG	A2	P	-	output of the voltage regulator; place a 0.1 μF capacitor between this pin and ground
TEST2	A3	AI	-	must be connected to ground
TEST3	A4	AI/O	-	must be connected to ground
RCV	A5	O	0	differential receiver output; reflects the differential value of DP and DM push-pull output

Table 2. Pin description *…continued*

Symbol[1]	Pin	Type[2]	Reset value	Description
INT_N	B1	OD	high-Z	interrupt output; active LOW open-drain output
DGND	B2	P	-	digital ground
OE_N/INT_N	B3	I/O	high-Z	this pin can be programmed as: **OE_N input —** Enables driving DP and DM when in USB mode **INT_N output —** Indicates interrupt when bit OE_INT_EN = 1 and SUSPEND_REG = 1 bidirectional; push-pull input; 3-state output
SE0/VM	B4	I/O	high-Z	**SE0 input and output —** SE0 functions in DAT_SE0 USB mode **VM input and output —** VM functions in VP_VM USB mode **TxD input —** UART mode bidirectional; push-pull input; 3-state output
DAT/VP	B5	I/O	high-Z	**DAT input and output —** DAT functions in DAT_SE0 USB mode **VP input and output —** VP functions in VP_VM USB mode **RxD output —** UART mode bidirectional; push-pull input; 3-state output
ADR/PSW	C1	I/O	high-Z	**ADR input —** Sets the least-significant I^2C-bus address bit of the ISP1302UK; latched on the rising edge of the RESET_N pin **PSW output —** Enables or disables the external charge pump after reset An internal series resistor is implemented for this pin. If the PSW (output) function is not used, then this pin can be directly connected to DGND or VREG. This pin will output 3.3 V when driven HIGH. For details, see Section 7.10. bidirectional; push-pull input; 3-state output
RESET_N	C2	I	-	asynchronous reset input, active LOW
AGND	C3	P	-	analog ground
TEST1	C4	AI	-	must be connected to ground
ID	C5	AI/O	-	identification detector input and output; connected to the ID pin of the USB micro receptacle; internal 100 kΩ pull-up resistor
$V_{CC(I/O)}$	D1	P	-	supply voltage for the I/O interface logic signals (1.4 V to 3.6 V)
SDA	D2	I/OD	high-Z	serial I^2C-bus data input and output bidirectional; push-pull input; open-drain output
SCL	D3	I/OD	high-Z	serial I^2C-bus clock input and output bidirectional; push-pull input; open-drain output
DP	D4	AI/O	high-Z	this pin can be programmed as: • USB D+ (data plus pin) or • transparent UART RxD
DM	D5	AI/O	high-Z	this pin can be programmed as: • USB D− (data minus pin) or • transparent UART TxD
CPGND	E1	P	-	ground for the charge pump

Table 2. Pin description *…continued*

Symbol[1]	Pin	Type[2]	Reset value	Description
C_B	E2	AI/O	-	charge pump flying capacitor pin 1; connect a 220 nF capacitor between C_B and C_A for 50 mA output current
C_A	E3	AI/O	-	charge pump flying capacitor pin 2; connect a 220 nF capacitor between C_B and C_A for 50 mA output current
V_{CC}	E4	P	-	supply voltage (3.0 V to 4.5 V)
V_{BUS}	E5	AI/O	high-Z	V_{BUS} line input and output of the USB interface; charge pump output; place an external decoupling capacitor of 0.1 μF close to this pin

[1] Symbol names ending with underscore N (for example, NAME_N) indicate active LOW signals.

[2] AI = analog input; AI/O = analog input/output; I = input; O = output; I/O = digital input/output; I/OD = input/open-drain output; OD = open-drain output; P = power or ground.

7. Functional description

7.1 Serial controller

The serial controller includes the following functions:

- Serial controller interface
- Device identification registers
- Control registers
- Interrupt registers
- Interrupt generator

The serial controller acts as an I^2C-bus slave, and uses the SCL and SDA pins to communicate with the OTG Controller.

For details on the serial controller, see Section 9.

7.2 V_{BUS} charge pump

The charge pump supplies current to the V_{BUS} line. It can operate in any of the following modes:

- Output 5 V at current above 50 mA
- Pull-up V_{BUS} to 3.3 V through a resistor ($R_{UP(VBUS)}$) to initiate V_{BUS} pulsing SRP
- Pull-down V_{BUS} to ground through a resistor ($R_{DN(VBUS)}$) to discharge V_{BUS}

7.3 V_{BUS} comparators

V_{BUS} comparators provide indications regarding the voltage level on V_{BUS}.

7.3.1 V_{BUS} valid comparator

This comparator is used by an A-device to determine whether the voltage on V_{BUS} is at a valid level for operation. The minimum threshold for the V_{BUS} valid comparator is 4.4 V. Any voltage on V_{BUS} below this threshold is considered a fault. A hardware debounce timer ($t_{d(VA\_VBUS\_VLD)}$) is implemented for the V_{BUS} valid comparator. This timer is enabled when the internal charge pump is turned on (bit VBUS_DRV = 1) and is disabled when the internal charge pump is turned off (bit VBUS_DRV = 0). During power-up, it is expected that the comparator output will be ignored.

7.3.2 Session valid comparator

The session valid comparator is used to determines when V_{BUS} is high enough for a session to start. Both the A-device and the B-device use this comparator to detect when a session is started. These devices also use this comparator to indicate when a session is completed. The session valid threshold is between 0.8 V to 2.0 V for A-device, and between 0.8 V to 4.0 V for B-device.

7.3.3 Session end comparator

The session end comparator determines when V_{BUS} is below the B-device session end threshold of 0.2 V to 0.8 V.

7.4 ID detector

In normal power mode (when both V_{CC} and $V_{CC(I/O)}$ are present), the ID detector senses the condition of the ID line and can differentiate between the following conditions:

- The ID pin is floating (bit ID_FLOAT = 1)
- The ID pin is shorted to ground (bit ID_GND = 1)

In power-down mode, only the ID_FLOAT detector is active and can wake up the chip. The ID_GND detector is turned off.

The recommended procedure to detect the ID status using software is:

1. When nothing is connected, ID is in the ID_FLOAT state. Enable the ID_FLOAT interrupt (falling edge).
2. If an interrupt occurs, read the Interrupt Latch register. If ID changes, bit ID_FLOAT_INT is set.
3. The software waits for some time, for example, 100 ms, to allow mechanical debounce.
4. The software reads the Interrupt Source register, and checks bits ID_FLOAT and ID_GND.

The ID detector has a switch that can be used to ground pin ID. This switch is controlled by bit ID_PULLDN of the OTG Control register.

7.5 Pull-up and pull-down resistors

Figure 4 shows the switchable pull-up and pull-down resistors that are internally connected to the DP and DM lines. The DP pull-up resistor (SW1) is controlled by bit DP_PULLUP of the OTG Control register.

The pull-up resistor is context variable as described in document *ECN_27%_Resistor*. The pull-up resistor value depends on the USB bus condition:

- When the bus is idle, the resistor is 900 Ω to 1575 Ω (SW2 = on).
- When the bus is transmitting or receiving, the resistor is 1425 Ω to 3090 Ω (SW2 = off).

DP also implements a weak pull-up resistor ($R_{weakUP(DP)}$) that is controlled using bit DP_WKPU_EN of the Misc Control register.

The DP pull-down resistor ($R_{DN(DP)}$) is connected to the DP line, if bit DP_PULLDOWN in the OTG Control register is set.

The DM pull-down resistor ($R_{DN(DM)}$) is connected to the DM line, if bit DM_PULLDOWN in the OTG Control register is set.

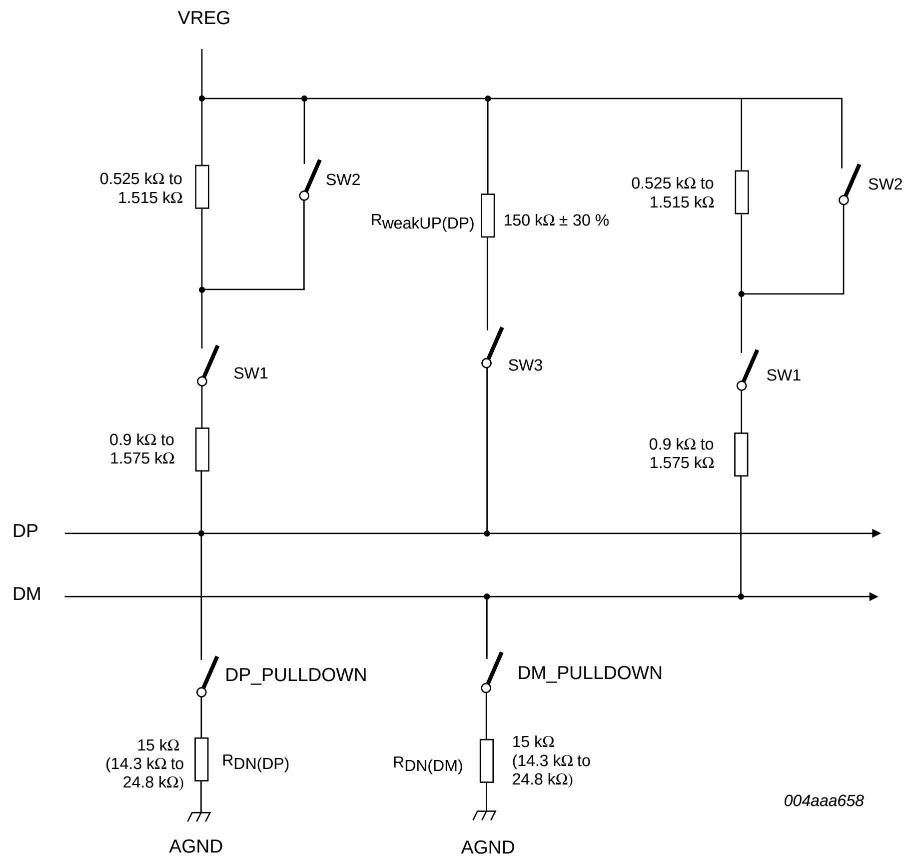


Fig 4. DP and DM pull-up and pull-down resistors

7.6 3.3 V DC-DC regulator

The built-in DC-DC regulator conditions the input power supply (V_{CC}) for use in the core of the ISP1302UK.

When V_{CC} is greater than 3.6 V, the regulator will output 3.3 V ± 10 %.

When V_{CC} is less than 3.6 V and bit REG_BYPASS_DIS = 0, the regulator will be automatically bypassed so that pin VREG will be shorted to pin V_{CC}.

When V_{CC} is less than 3.6 V and bit REG_BYPASS_DIS = 1, the regulator will output a voltage between V_{CC} and V_{CC} – 0.2 V.

The output of the regulator can be monitored on pin VREG. A capacitor (0.1 μF) must be connected between pin VREG and ground.

7.7 Autoconnect and AutoSE0

The HNP in the OTG supplement specifies the following sequence of events to transfer the role of the host from the A-device to the B-device:

1. The A-device sets the bus in the suspend state.
2. The B-device simulates a disconnect by deasserting its DP pull-up.

3. The A-device detects SE0 on the bus and asserts its DP pull-up.
4. The B-device detects that the DP line is HIGH, drives SE0 to DP/DM lines and assumes the role of the host.

The OTG supplement specifies that the time between the B-device deasserting its DP pull-up and the A-device asserting its pull-up must be less than 3 ms. For an A-device with a slow interrupt response time, 3 ms may not be enough to write an I^2C-bus command to the ISP1302UK to assert DP pull-up. An alternative method is for the A-device transceiver to automatically assert DP pull-up after detecting an SE0 from the B-device.

The sequence of events is as follows: After finishing data transfers between the A-device and the B-device and before suspending the bus, the A-device sends SOFs. The B-device receives these SOFs, and does not transmit any packet back to the A-device. During this time, the A-device sets the BDIS_ACON_EN bit in the ISP1302UK. This enables the ISP1302UK to look for SE0 whenever the A-device is not transmitting (that is, whenever the OE_N/INT_N pin of the ISP1302UK is not asserted). After the BDIS_ACON_EN bit is set, the A-device stops transmitting SOFs and allows the bus to go to the idle state. If the B-device disconnects, the bus goes to SE0, and the ISP1302UK logic automatically turns on the A-device pull-up. To disable the DP pull-up resistor, clear bit BDIS_ACON_EN.

The OTG supplement specifies that the time between the A-device asserting its DP pull-up and the B-device driving SE0 must be less than 1 ms. For a B-device with a slow interrupt response time, 1 ms may not be enough for the OTG controller to detect a remote connection and drive the bus reset (SE0) to USB data lines. An alternative method is for the B-device transceiver to automatically drive SE0 after detecting that DP is pulled HIGH by the A-device.

The sequence of events is as follows:

1. The B-device is in b_peripheral state, with DP_PULLUP enabled. The B-device is ready to transit to b_wait_acon state.
2. Set ACON_BSE0_EN (BDIS_ACON_EN) bit in Mode Control 1 register to 1.
3. Set BDIS_ACON_IEH bit in Interrupt Enable High register to 1 (alternatively, set DP_HI_IEH bit to 1).
4. Set FORCE_DP_LOW bit in Misc Control register to 1.
5. Disable DP_PULLUP.
6. Set FORCE_DP_LOW bit in Misc Control register to 0.
7. The B-device goes to b_wait_acon state.
8. The remote A-device will enable PU on D+ within 3 ms.
9. Wait for interrupt BDIS_ACON_INT in Interrupt Latch register (alternatively, detect DP_HI_INT interrupt).
10. The B-device waits for 50 ms, clears the ACON_BSE0_EN bit, goes to b_host state and enables SOFs.

The software needs to make sure the actual time spent on items 4 to 6 (inclusive) is less than 1 ms. A typical I^2C one-byte write operation takes about 75 μs (I^2C clock = 400 kHz).

7.8 USB transceiver

7.8.1 Differential driver

The operation of the driver is described in Table 3.

Table 3. Transceiver driver operating setting

Pin		Bit		Differential driver
RESET_N[1]	OE_N/INT_N	SUSPEND	DAT_SE0	
HIGH	LOW	0	0	output value from DAT/VP to DP and SE0/VM to DM
HIGH	LOW	0	1	output value from DAT/VP to DP and DM if SE0/VM is LOW; otherwise drive both DP and DM to LOW
HIGH	LOW	1	X	output value from DAT/VP to DP and DM
HIGH	HIGH	X	X	high-Z
LOW	X	X	X	high-Z

[1] Include the internal power-on-reset pulse (active HIGH).

Table 4 shows the behavior of the transmit operation in detail.

Table 4. USB functional mode: transmit operation

USB mode	Inputs		Outputs	
	DAT/VP	SE0/VM	DP	DM
DAT_SE0	LOW	LOW	LOW	HIGH
DAT_SE0	HIGH	LOW	HIGH	LOW
DAT_SE0	LOW	HIGH	LOW	LOW
DAT_SE0	HIGH	HIGH	LOW	LOW
VP_VM	LOW	LOW	LOW	LOW
VP_VM	HIGH	LOW	HIGH	LOW
VP_VM	LOW	HIGH	LOW	HIGH
VP_VM	HIGH	HIGH	HIGH	HIGH

7.8.2 Differential receiver

The operation of the differential receiver is described in Table 5.

Table 5. Differential receiver operation settings

Pin	Bit		Differential receiver
OE_N/INT_N	SUSPEND	DAT_SE0	
HIGH	0	1	output differential value from DP and DM to DAT/VP and RCV
HIGH	0	0	output differential value from DP and DM to RCV

The detailed behavior of the receive transceiver operation is shown in Table 6.

Table 6. USB functional mode: receive operation

USB mode	Bit SUSPEND	Inputs		Outputs		
		DP	DM	DAT/VP	SE0/VM	RCV
DAT_SE0	0	LOW	LOW	RCV	HIGH	last value of RCV
DAT_SE0	0	HIGH	LOW	HIGH	LOW	HIGH
DAT_SE0	0	LOW	HIGH	LOW	LOW	LOW
DAT_SE0	0	HIGH	HIGH	RCV	LOW	last value of RCV
DAT_SE0	1	LOW	LOW	LOW	HIGH	X
DAT_SE0	1	HIGH	LOW	HIGH	LOW	X
DAT_SE0	1	LOW	HIGH	LOW	LOW	X
DAT_SE0	1	HIGH	HIGH	HIGH	LOW	X
VP_VM	0	LOW	LOW	LOW	LOW	last value of RCV
VP_VM	0	HIGH	LOW	HIGH	LOW	HIGH
VP_VM	0	LOW	HIGH	LOW	HIGH	LOW
VP_VM	0	HIGH	HIGH	HIGH	HIGH	last value of RCV
VP_VM	1	LOW	LOW	LOW	LOW	X
VP_VM	1	HIGH	LOW	HIGH	LOW	X
VP_VM	1	LOW	HIGH	LOW	HIGH	X
VP_VM	1	HIGH	HIGH	HIGH	HIGH	X

7.9 Power-On Reset (POR)

When V_{CC} is powered on, an internal POR is generated. The internal POR pulse width (t_{PORP}) will typically be 200 ns. The pulse is started when V_{CC} rises above $V_{POR(trip)}$.

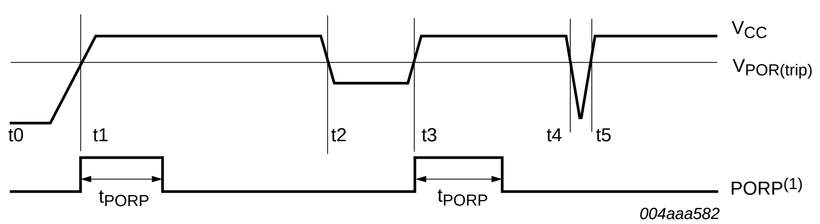
The power-on reset function can be explained by viewing the dips at t2 to t3 and t4 to t5 on the V_{CC} curve (see Figure 5).

t0 — The internal POR starts with a LOW level.

t1 — The detector will see the passing of the trip level and a delay element will add another t_{PORP} before it drops to LOW.

t2 to t3 — The internal POR pulse will be generated whenever V_{CC} drops below $V_{POR(trip)}$ for more than 11 μs.

t4 to t5 — The dip is too short (< 11 μs) and the internal POR pulse will not react and will remain LOW.



(1) PORP = Power-On Reset Pulse.

Fig 5. Internal power-on reset timing

7.10 I²C-bus device address and external charge pump control

The ADR/PSW pin has two functions. Both functions are described as follows.

The first function of the ADR/PSW pin is to set the I²C-bus address. On the rising edge of the RESET_N pin, the level on ADR/PSW is latched and stored in ADR_REG, which represents the Least Significant Bit (LSB) of the I²C-bus address. If ADR_REG = 0, the I²C-bus address for the ISP1302UK is 010 1100 (2Ch); if ADR_REG = 1, the I²C-bus address for the ISP1302UK is 010 1101 (2Dh). The power-on reset value of ADR_REG = 0.

The second function of the ADR/PSW pin is to control an external charge pump. The ADR/PSW pin can be programmed as an active HIGH or active LOW PSW output. The polarity of the PSW output is determined by ADR_REG. If ADR_REG = 0, then PSW will be active HIGH; if ADR_REG = 1, then PSW will be active LOW. The PSW output will be enabled only when Mode Control 2 register bit PSW_OE = 1. By default, PSW can only drive HIGH if the hardware reset pulse is not issued on RESET_N.

The combinations of I²C-bus address and the PSW polarity are limited, as shown in Table 7.

Table 7. Possible combinations of I²C-bus address and the PSW polarity

ADR/PSW level on the rising edge of RESET_N	I²C-bus address	PSW polarity
LOW	2Ch	active HIGH
HIGH	2Dh	active LOW

The ISP1302UK built-in charge pump supports V_{BUS} current at 50 mA. If the application needs more current support, an external charge pump may be needed. In this case, the ADR/PSW pin can act as a power switch for the external charge pump. Figure 6 shows an example of using an external charge pump.

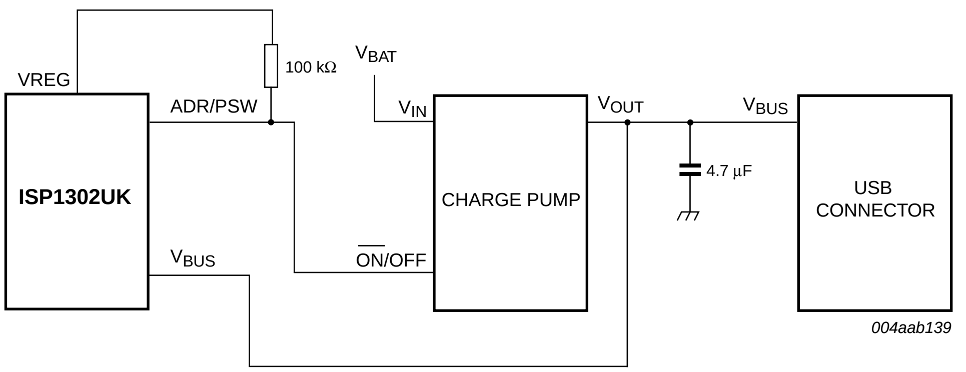


Fig 6. Using an external charge pump

8. Modes of operation

The ISP1302UK supports three types of modes:

- Power modes
- USB modes
- Transparent modes

8.1 Power modes

8.1.1 Normal mode

In this mode, both V_{CC} and $V_{CC(I/O)}$ are connected and their voltage levels are within the operation range.

There are three levels of power saving schemes in the ISP1302UK:

- Active-power mode: power is on; all circuits are active.
- USB suspend mode: to reduce power consumption, the USB differential receiver is powered down.
- Power-down mode: set by writing logic 1 to bit PWR_DN of the Mode Control 2 register. The clock generator and all biasing circuits are turned off to reduce power consumption to the minimum possible. For details on waking up the clock, see Section 10.

8.1.2 Disable mode

In disable mode, $V_{CC(I/O)}$ is cut-off and V_{CC} is powered. In this mode, the ISP1302UK is in the power-down state.

The USB differential driver will be 3-stated as long as $V_{CC(I/O)}$ is not present.

8.1.3 Isolate mode

In isolate mode, V_{CC} is cut-off and $V_{CC(I/O)}$ is powered. In this mode, the ISP1302UK will drive a stable level to all digital output pins, and all bidirectional digital pins will be set in 3-state.

Table 8 shows a summary of power modes.

Table 8. ISP1302UK power modes summary

V_{CC}	$V_{CC(I/O)}$	PWR_DN (bit)	$I_{CC} = I_{CC(pd)}$	Comment
Off	off	X	yes	power off
Off	on	X	yes	isolate mode
On	off	X	yes	disable mode (power-down)
On	on	0	no	normal mode (full operation)
On	on	1	yes	normal mode (power-down)

Table 9 shows the pin states in disable and isolate modes.

Table 9. ISP1302UK pin states in disable and isolate modes

Pin name	Disable mode (V_{CC} = on, $V_{CC(I/O)}$ = off)	Isolate mode (V_{CC} = off, $V_{CC(I/O)}$ = on)
V_{CC}, VREG	powered	not present
$V_{CC(I/O)}$	not present	powered
DP	15 kΩ pull-down resistor enabled	high-Z
DM	15 kΩ pull-down resistor enabled	high-Z
RCV	high-Z	drive LOW
RESET_N, SDA, SCL, ADR/PSW, SE0/VM, DAT/VP, INT_N, OE_N/INT_N, SERVICE_N	high-Z	high-Z
ID, V_{BUS}, C_A, C_B	high-Z	high-Z

8.2 USB modes

The two USB modes of the ISP1302UK are:

- VP_VM bidirectional mode
- DAT_SE0 bidirectional mode

In VP_VM USB mode, pin DAT/VP is used for the VP function, pin SE0/VM is used for the VM function, and pin RCV is used for the RCV function.

In DAT_SE0 USB mode, pin DAT/VP is used for the DAT function, pin SE0/VM is used for the SE0 function, and pin RCV is not used.

Table 10 specifies the functionality of the device during the two USB modes.

Table 10. USB functional modes: I/O values

USB mode[1]	Bit	Pin			
	DAT_SE0	OE_N/INT_N	DAT/VP	SE0/VM	RCV
VP_VM	0	LOW	TxD+[2]	TxD–[2]	RxD[6]
		HIGH	RxD+[3]	RxD–[3]	RxD[6]
DAT_SE0	1	LOW	TxD[4]	FSE0[5]	RxD[6]
		HIGH	RxD[6]	RSE0[7]	RxD[6]

[1] Some of the modes and signals are provided to achieve backward compatibility with IP cores.

[2] TxD+ and TxD– are single-ended inputs to drive the DP and DM outputs, respectively, in single-ended mode.

[3] RxD+ and RxD– are the outputs of the single-ended receivers connected to DP and DM, respectively.

[4] TxD is the input to drive DP and DM in DAT_SE0 mode.

[5] FSE0 is to force an SE0 on the DP and DM lines in DAT_SE0 mode.

[6] RxD is the output of the differential receiver.

[7] RSE0 is an output, indicating that an SE0 is received on the DP and DM lines.

8.3 Transparent modes

8.3.1 Transparent UART mode

When in transparent UART mode, an SoC (with the UART controller) communicates through the ISP1302UK to another UART device that is connected to its DP and DM lines. The ISP1302UK operates as a logic level translator between the following pins:

- For the TxD signal: from SE0/VM ($V_{CC(I/O)}$ level) to DM (VREG level).
- For the RxD signal: from DP (VREG level) to DAT/VP ($V_{CC(I/O)}$ level).

The ISP1302UK is in transparent UART mode, if bit UART_EN of the Mode Control 1 register is set.

8.3.2 Transparent general-purpose buffer mode

In transparent general-purpose buffer mode, the DAT/VP and SE0/VM pins are connected to the DP and DM pins, respectively. The direction of the data transfer can be controlled using bits TRANSP_BDIR1 and TRANSP_BDIR0 of the Mode Control 2 register as specified in Table 12.

The ISP1302UK is in transparent general-purpose buffer mode, if bit UART_EN = 0, bit DAT_SE0 = 1 and bit TRANSP_EN = 1.

Table 11 provides a summary of device operating modes.

Table 11. Summary of device operating modes

Mode	Bit			Description
	UART_EN	TRANSP_EN	DAT_SE0	
USB mode	0	0	X	USB ATX enabled
Transparent general-purpose buffer mode	0	1	1	USB ATX disabled. SE0/VM ↔ DM DAT/VP ↔ DP see Table 12
Transparent UART mode	1	X	X	USB ATX disabled. SE0/VM → DM DAT/VP ← DP

Table 12. Transparent general-purpose buffer mode

Bit TRANSP_BDIR[1:0]	Direction of the data flow	
00	DAT/VP → DP	SE0/VM → DM
01	DAT/VP → DP	SE0/VM ← DM
10	DAT/VP ← DP	SE0/VM → DM
11	DAT/VP ← DP	SE0/VM ← DM

9. Serial controller

9.1 Register map

Table 13 provides an overview of serial controller registers.

Remark: Reserved registers must never be written or undefined behavior will result.

Table 13. Register overview

Register	Width (bits)	Access	Memory address[1]	Functionality	Reference
Vendor ID	16	R	00h to 01h	device identification registers	Section 9.1.1 on page 17
Product ID	16	R	02h to 03h		
Version ID	16	R	14h to 15h		
Mode Control 1	8	R/S/C	**Set** — 04h **Clear** — 05h	control and status registers	Section 9.1.2 on page 18
Mode Control 2	8	R/S/C	**Set** — 12h **Clear** — 13h		
Reserved	-	-	16h to 17h		
OTG Control	8	R/S/C	**Set** — 06h **Clear** — 07h		
Misc Control	8	R/S/C	**Set** — 18h **Clear** — 19h		
Reserved	-	-	1Ah to FFh		
OTG Status	8	R	10h		
Interrupt Source	8	R	08h	interrupt registers	Section 9.1.3 on page 22
Interrupt Latch	8	R/S/C	**Set** — 0Ah **Clear** — 0Bh		
Interrupt Enable Low	8	R/S/C	**Set** — 0Ch **Clear** — 0Dh		
Interrupt Enable High	8	R/S/C	**Set** — 0Eh **Clear** — 0Fh		

[1] The R/W/S/C access type represents a field that can be read, written, set or cleared (set to 0). A register can be read from either of the set or clear addresses. Writing to a write address indicates that values will be directly written to the register. Writing logic 1 to a set address sets the associated bit. Writing logic 1 to a clear address clears the associated bit. Writing logic 0 to either a set or clear address has no effect.

9.1.1 Device identification registers

9.1.1.1 Vendor ID register

Table 14 provides the bit description of the Vendor ID register.

Table 14. Vendor ID register (address R = 00h to 01h) bit description

Bit	Symbol	Access	Value	Description
15 to 0	VENDORID[15:0]	R	04CCh	ST-Ericsson' Vendor ID

9.1.1.2 Product ID register

The bit description of the Product ID register is given in Table 15.

Table 15. Product ID register (address R = 02h to 03h) bit description

Bit	Symbol	Access	Value	Description
15 to 0	PRODUCTID[15:0]	R	1302h	Product ID of the ISP1302UK

9.1.1.3 Version ID register

Table 16 shows the bit allocation of the register.

Table 16. Version ID register (address R = 14h to 15h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	PACKAGEID[3:0]				LEGACYID[3:0]			
Reset	X[1]							
Access	R	R	R	R	R	R	R	R
Bit	7	6	5	4	3	2	1	0
Symbol	MAJORID[3:0]				MINORID[3:0]			
Reset	X[1]							
Access	R	R	R	R	R	R	R	R

[1] The reset value depends on the version number of the chip.

Table 17. Version ID register (address R = 14h to 15h) bit description

Bit	Symbol	Description
15 to 12	PACKAGEID[3:0]	Package information: **1 —** WLCSP25
11 to 8	LEGACYID[3:0]	Legacy version ID: **0 —** New method of defining the version ID **1 to 15 —** Legacy method of defining the version ID
7 to 4	MAJORID[3:0]	Version ID, major number; this number starts with 1 and increments by 1 if there is a major update to the chip.
3 to 0	MINORID[3:0]	Version ID, minor number; this number starts with 0 and increments by 1 if there is a minor update to the chip.

9.1.2 Control registers

9.1.2.1 Mode Control 1 register

The bit allocation of the Mode Control 1 register is given in Table 18.

Table 18. Mode Control 1 register (address S = 04h, C = 05h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved	UART_EN	OE_INT_EN	BDIS_ACON_EN	TRANSP_EN	DAT_SE0	SUSPEND	SPEED
Reset	0	0/1	0	0	0	0	0	0
Access	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C

Table 19. Mode Control 1 register (address S = 04h, C = 05h) bit description

Bit	Symbol	Description
7	-	reserved
6	UART_EN	When set, the ATX is in transparent UART mode. The default value of this bit depends on the SERVICE_N pin. On reset, if SERVICE_N = HIGH, the reset value of UART_EN = 0; if SERVICE_N = LOW, the reset value of UART_EN = 1.
5	OE_INT_EN	When set and when in suspend mode, pin OE_N/INT_N becomes an output and is asserted when an interrupt occurs.
4	BDIS_ACON_EN	This bit has two functions (see Section 7.7): For an A-device, this bit works as BDIS_ACON_EN. It enables the A-device to connect if the B-device disconnect is detected. **0 —** DP pull-up resistor is controlled by the DP_PULLUP bit in the OTG Control register. **1 —** DP pull-up resistor will connect on the B-device disconnect. For a B-device, this bit works as ACON_BSE0_EN. It enables the B-device to drive SE0 on DP and DM, if the A-device connect is detected. **0 —** B-device will stop driving SE0. **1 —** B-device will start to drive SE0, if the A-device connect is detected.
3	TRANSP_EN	When set, the ATX is in transparent general-purpose buffer mode.
2	DAT_SE0	**0 —** VP_VM mode **1 —** DAT_SE0 mode
1	SUSPEND	Sets the transceiver in low-power mode. **0 —** Active-power mode **1 —** Low-power mode (differential receiver is disabled if SPEED = 1)
0	SPEED	Set the rise time and the fall time of the transmit driver in USB modes. **0 —** Low-speed mode **1 —** Full-speed mode

9.1.2.2 Mode Control 2 register

For the bit allocation of this register, see Table 20.

Table 20. Mode Control 2 register (address S = 12h, C = 13h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved	PSW_OE	reserved	TRANSP_BDIR1	TRANSP_BDIR0	reserved		PWR_DN
Reset	0	0	0	0	0	1	0	0
Access	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C

Table 21. Mode Control 2 register (address S = 12h, C = 13h) bit description

Bit	Symbol	Description
7	-	reserved
6	PSW_OE	**0 —** ADR/PSW pin acts as an input. **1 —** ADR/PSW pin is driven.

Table 21. Mode Control 2 register (address S = 12h, C = 13h) bit description *...continued*

Bit	Symbol	Description
5	-	reserved
4 to 3	TRANSP_BDIR [1:0]	Controls the direction of data transfer in transparent general-purpose buffer mode; see Table 12
2 to 1	-	reserved
0	PWR_DN	Set to power-down mode; activities on pin SCL or the interrupt event can wake-up the chip; see Section 10

9.1.2.3 OTG Control register

Table 22 shows the bit allocation of the OTG Control register.

Table 22. OTG Control register (address S = 06h, C = 07h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	VBUS_ CHRG	VBUS_ DISCHRG	VBUS_ DRV	ID_PULL DN	DM_PULL DOWN	DP_PULL DOWN	DM_PULL UP	DP_PULL UP
Reset	0	0	0	0	1	1	0	0
Access	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C

Table 23. OTG Control register (address S = 06h, C = 07h) bit description

Bit	Symbol	Description
7	VBUS_CHRG	Charge V_{BUS} through a pull-up resistor ($R_{UP(VBUS)}$), which is connected to VREG. **0** — Disconnect the resistor **1** — Connect the resistor
6	VBUS_DISCHRG	Discharge V_{BUS} through a pull-down resistor ($R_{DN(VBUS)}$). **0** — Disconnect the resistor **1** — Connect the resistor
5	VBUS_DRV	Drive V_{BUS} to 5 V through the charge pump. **0** — Charge pump is disabled **1** — Charge pump is enabled
4	ID_PULLDN	Connect pin ID to ground. See Table 3. **0** — Disconnected **1** — Connected
3	DM_PULLDOWN	Connect the DM pull-down resistor ($R_{DN(DM)}$). **0** — DM pull-down resistor is disconnected **1** — DM pull-down resistor is connected

Table 23. OTG Control register (address S = 06h, C = 07h) bit description *...continued*

Bit	Symbol	Description
2	DP_PULLDOWN	Connect the DP pull-down resistor ($R_{DN(DP)}$). **0 —** DP pull-down resistor is disconnected **1 —** DP pull-down resistor is connected
1	DM_PULLUP	Connect the DM pull-up resistor ($R_{UP(DM)}$). **0 —** DM pull-up resistor is disconnected **1 —** DM pull-up resistor is connected
0	DP_PULLUP	Connect the DP pull-up resistor ($R_{UP(DP)}$). **0 —** DP pull-up resistor is disconnected (assuming that bit BDIS_ACON_EN is logic 0) **1 —** DP pull-up resistor is connected

9.1.2.4 Misc Control register

Table 24 shows the bit allocation of the register.

Table 24. Misc Control register (address S = 18h, C = 19h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	FORCE_ DP_HIGH	FORCE_ DP_LOW	reserved	UART_2V8 _EN	IDPU_DIS	DP_WKPU _EN	SRP_INIT	REG_BY PASS_DIS
Reset	0	0	0	1	0	0	0	0
Access	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C

Table 25. Misc Control register (address S = 18h, C = 19h) bit description

Bit	Symbol	Description
7	FORCE_DP_HIGH	Forces the DP pin to be driven to HIGH
6	FORCE_DP_LOW	Forces the DP pin to be driven to LOW
5	-	reserved
4	UART_2V8_EN	This bit indicates the output voltage level of the internal regulator. This bit is only valid when bit UART_EN is logic 1. When this bit and bit UART_EN are logic 1, the internal regulator bypass switch will always be disabled, ignoring the value of bit REG_BYPASS_DIS. This is to ensure that the internal regulator outputs +2.8 V, when V_{CC} is 3.0 V to 4.5 V. **0 —** Internal regulator outputs 3.3 V **1 —** Internal regulator outputs 2.8 V
3	IDPU_DIS	**0 —** Internal ID pin pull-up resistor is enabled **1 —** Internal ID pin pull-up resistor is disabled

Table 25. Misc Control register (address S = 18h, C = 19h) bit description *…continued*

Bit	Symbol	Description
2	DP_WKPU_EN	This bit will enable $R_{weakUP(DP)}$ on the DP line if V_{BUS} is powered and the SESS_VLD bit is also set. It is provided to support the detection of external accessory devices. **0 —** Disconnect the DP weak pull-up resistor ($R_{weakUP(DP)}$) **1 —** Connect the DP weak pull-up resistor ($R_{weakUP(DP)}$)
1	SRP_INIT	**0 —** No event **1 —** Initialize SRP, if this bit is set, the following events occur in sequence: enable DP pull-up for 7.5 ms, enable the VBUS_CHRG resistor for 32 ms, enable the VBUS_DISCHRG resistor for 13 ms. This bit will autoclear when the sequence is complete.
0	REG_BYPASS_DIS	**0 —** Internal regulator bypass switch is turned on, when V_{CC} < 3.6 V **1 —** Internal regulator bypass switch is turned off

9.1.2.5 OTG Status register

Table 26 shows the bit allocation of the OTG Status register.

Table 26. OTG Status register (address R = 10h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved	B_SESS_END	reserved					
Reset	0	-[1]	0	0	-	-	-	0
Access	R	R	R	R	R	R	R	R

[1] The reset value depends on the status of the respective pin.

Table 27. OTG Status register (address R = 10h) bit description

Bit	Symbol	Description
7	-	reserved
6	B_SESS_END	Set when the V_{BUS} voltage is below the B-device session end threshold (0.2 V to 0.8 V). In power-down mode, this bit is fixed as logic 0.
5 to 0	-	reserved

9.1.3 Interrupt registers

9.1.3.1 Interrupt Source register

Table 28 shows the bit allocation of this register that indicates the current state of the signals that can generate an interrupt.

Table 28. Interrupt Source register (address R = 08h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved	BDIS_ACON	ID_FLOAT	DM_HI	ID_GND	DP_HI	SESS_VLD	VBUS_VLD
Reset	-	0	-[1]	-[1]	-[1]	-[1]	-[1]	-[1]
Access	R	R	R	R	R	R	R	R

[1] The reset value depends on the status of the respective pin.

Table 29. Interrupt Source register (address R = 08h) bit description

Bit	Symbol	Description
7	-	reserved
6	BDIS_ACON	Set when bit BDIS_ACON_EN is set, and the ISP1302UK enables the DP pull-up resistor after detecting the B-device disconnect (SE0). **0** — No event **1** — BDIS_ACON is detected.
5	ID_FLOAT	Indicates the status of pin ID. **0** — ID pin is not floating. **1** — ID pin is floating.
4	DM_HI	DM single-ended receiver output. **0** — LOW **1** — HIGH
3	ID_GND	Indicates the status of pin ID: **0** — ID pin is not grounded. **1** — ID pin is grounded. In power-down mode, this bit is fixed as logic 0.
2	DP_HI	DP single-ended receiver output. **0** — LOW **1** — HIGH
1	SESS_VLD	V_{BUS} session valid detector. **0** — V_{BUS} is lower than $V_{A\_SESS\_VLD}$ (bit ID_GND = 1) or $V_{B\_SESS\_VLD}$ (bit ID_GND = 0). **1** — V_{BUS} is higher than $V_{A\_SESS\_VLD}$ (bit ID_GND = 1) or $V_{B\_SESS\_VLD}$ (bit ID_GND = 0).
0	VBUS_VLD	This bit has two functions: For the A-device (bit ID_GND = 1), it acts as the V_{BUS} valid detector. **0** — V_{BUS} is lower than the V_{BUS} valid threshold. **1** — V_{BUS} is higher than the V_{BUS} valid threshold. For the B-device (bit ID_GND = 0), it acts as B_SESS_END (B-device session end detector). **0** — V_{BUS} is above the B-device session end threshold (0.2 V to 0.8 V). **1** — V_{BUS} is below the B-device session end threshold (0.2 V to 0.8 V). In power-down mode, this bit is fixed as logic 0.

9.1.3.2 Interrupt Latch register

This register indicates the source that generates an interrupt. For the bit allocation, see Table 30.

Table 30. Interrupt Latch register (address S = 0Ah, C = 0Bh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved	BDIS_ ACON_INT	ID_FLOAT _INT	DM_HI_ INT	ID_GND_ INT	DP_HI_INT	SESS_VLD _INT	VBUS_ VLD_INT
Reset	0	0	0	0	0	0	0	0
Access	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C

Table 31. Interrupt Latch register (address S = 0Ah, C = 0Bh) bit description

Bit	Symbol	Description
7	-	reserved
6	BDIS_ACON_INT	**0** — No interrupt **1** — Interrupt on the BDIS_ACON status change
5	ID_FLOAT_INT	**0** — No interrupt **1** — Interrupt on the ID_FLOAT status change
4	DM_HI_INT	**0** — No interrupt **1** — Interrupt on the DM_HI status change
3	ID_GND_INT	**0** — No interrupt **1** — Interrupt on the ID_GND status change
2	DP_HI_INT	**0** — No interrupt **1** — Interrupt on the DP_HI status change
1	SESS_VLD_INT	**0** — No interrupt **1** — Interrupt on the SESS_VLD status change
0	VBUS_VLD_INT	**0** — No interrupt **1** — Interrupt on the VBUS_VLD status change

9.1.3.3 Interrupt Enable Low register

The bits in this register enable interrupts when the corresponding bits in the Interrupt Source register change from logic 1 to logic 0. Table 32 shows the bit allocation of the register.

Table 32. Interrupt Enable Low register (address S = 0Ch, C = 0Dh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved		ID_FLOAT_IEL	DM_HI_IEL	ID_GND_IEL	DP_HI_IEL	SESS_VLD_IEL	VBUS_VLD_IEL
Reset	0	0	0	0	0	0	0	0
Access	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C

Table 33. Interrupt Enable Low register (address S = 0Ch, C = 0Dh) bit description

Bit	Symbol	Description
7 to 6	-	reserved
5	ID_FLOAT_IEL	**0** — Disable **1** — Enable
4	DM_HI_IEL	**0** — Disable **1** — Enable
3	ID_GND_IEL	**0** — Disable **1** — Enable
2	DP_HI_IEL	**0** — Disable **1** — Enable
1	SESS_VLD_IEL	**0** — Disable **1** — Enable
0	VBUS_VLD_IEL	**0** — Disable **1** — Enable

9.1.3.4 Interrupt Enable High register

The bits in this register enable interrupts when the corresponding bits in the Interrupt Source register change from logic 0 to logic 1. For the bit allocation, see Table 34.

Table 34. Interrupt Enable High register (address S = 0Eh, C = 0Fh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved	BDIS_ ACON_IEH	ID_FLOAT _IEH	DM_HI_ IEH	ID_GND_ IEH	DP_HI_IEH	SESS_VLD _IEH	VBUS_ VLD_IEH
Reset	0	0	0	0	0	0	0	0
Access	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C

Table 35. Interrupt Enable High register (address S = 0Eh, C = 0Fh) bit description

Bit	Symbol	Description
7	-	reserved
6	BDIS_ACON_IEH	**0** — Disable **1** — Enable
5	ID_FLOAT_IEH	**0** — Disable **1** — Enable
4	DM_HI_IEH	**0** — Disable **1** — Enable
3	ID_GND_IEH	**0** — Disable **1** — Enable
2	DP_HI_IEH	**0** — Disable **1** — Enable
1	SESS_VLD_IEH	**0** — Disable **1** — Enable
0	VBUS_VLD_IEH	**0** — Disable **1** — Enable

9.2 Interrupts

Any of the Interrupt Source register signals given in Table 28 can generate an interrupt, when the signal becomes either LOW or HIGH. After an interrupt is generated, the SoC should be able to read the status of each signal and the bit that indicates whether that signal generated the interrupt. A bit in the Interrupt Latch register is set when any of the following events occurs:

- Writing logic 1 to a set address sets the corresponding bit.
- The corresponding bit in the Interrupt Enable High register is set, and the associated signal changes from LOW to HIGH.
- The corresponding bit in the Interrupt Enable Low register is set, and the associated signal changes from HIGH to LOW.
- The INT_N pin will be asserted if one or more bits in the Interrupt Latch register are set. The INT_N pin will be deasserted if all the bits in the Interrupt Latch register are cleared by software.

When entering power-down mode, the Interrupt Source register bit of the corresponding wake-up event must be cleared for an interrupt to occur. For the clock wake-up event, see Section 10.2.

9.3 I²C-bus protocol

For detailed information, refer to *The I²C-bus specification; ver. 2.1*.

9.3.1 I²C-bus byte transfer format

Table 36. I²C-bus byte transfer format

S[1]	Byte 1	A[2]	Byte 2	A[2]	Byte 3	A[2]	..	A[2]	P[3]
	8 bits		8 bits		8 bits		..		

[1] S = Start.

[2] A = Acknowledge.

[3] P = Stop.

9.3.2 I²C-bus device address

Table 37. I²C-bus slave address bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	A6	A5	A4	A3	A2	A1	A0	R/W
Value	0	1	0	1	1	0	[1]	X

[1] Determined by the status of the ADR/PSW pin on the rising edge of RESET_N. If ADR/PSW = HIGH, bit A0 = 1; if ADR/PSW = LOW, bit A0 = 0. Bit A0 will be zero if there is no hardware reset pulse on the RESET_N pin after power on.

Table 38. I²C-bus slave address bit description

Bit	Symbol	Description
7 to 1	A[6:0]	**Device Address**: The device address of the ISP1302UK is 01 0110 (A0), where A0 is determined by pin ADR/PSW.
0	R/W	Read or write command. **0 —** Write **1 —** Read

9.3.3 Write format

A write operation can be performed as:

- One-byte write to the specified register address.
- Multiple-byte write to N consecutive registers, starting from the specified start address. N defines the number of registers to write. If N = 1, only the start register is written.

9.3.3.1 One-byte write

Table 39 describes the transfer format for a one-byte write.

Table 39. Transfer format description for a one-byte write

Byte	Description
S	master starts with a START condition
Device select	master transmits the device address and write command bit R/W = 0
ACK	slave generates an acknowledgment
Register address K	master transmits the address of register K
ACK	slave generates an acknowledgment
Write data K	master writes data to register K
ACK	slave generates an acknowledgment
P	master generates a STOP condition

9.3.3.2 Multiple-byte write

Table 40 describes the transfer format for multiple-byte write.

Table 40. Transfer format description for a multiple-byte write

Byte	Description
S	master starts with a START condition
Device select	master transmits the device address and write command bit R/W = 0
ACK	slave generates an acknowledgment
Register address K	master transmits the address of register K. This is the start address for writing multiple data bytes to consecutive registers. After a byte is written, the register address is automatically incremented by 1. **Remark:** If the master writes to a nonexistent register, the slave must send a 'not ACK' and also must not increment the index address.
ACK	slave generates an acknowledgment
Write data K	master writes data to register K
ACK	slave generates an acknowledgment
Write data K + 1	master writes data to register K + 1
ACK	slave generates an acknowledgment
:	:
Write data K + N – 1	master writes data to register K + N – 1. When the incremented address K + N – 1 becomes > 255, the register address rolls over to 0. Therefore, it is possible that some registers may be overwritten, if the transfer is not stopped before the rollover.
ACK	slave generates an acknowledgment
P	master generates a STOP condition

Figure 7 illustrates the write format for a one-byte write and a multiple-byte write.

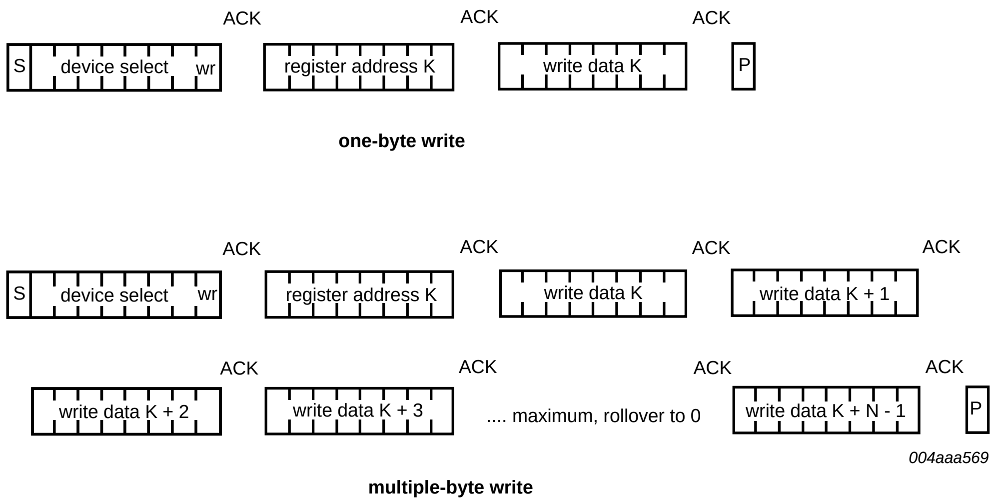


Fig 7. Writing data to the ISP1302UK registers

9.3.4 Read format

A read operation can be performed in two ways:

- Current address read: To read the register at the current address.
  - Single register read
- Random address read: To read N registers starting at a specified address. N defines the number of registers to be read. If N = 1, only the start register is read.
  - Single register read
  - Multiple register read

9.3.4.1 Current address read

The transfer format description for a current address read is given in Table 41. For the illustration, see Figure 8.

Table 41. Transfer format description for current address read

Byte	Description
S	master starts with a START condition
Device select	master transmits the device address and read command bit R/W = 1
ACK	slave generates an acknowledgment
Read data K	slave transmits and master reads data from register K. If the start address is not specified, the read operation starts from where the index register is pointing to because of a previous read or write operation.
No ACK	master terminates the read operation by generating a no acknowledgement
P	master generates a stop condition

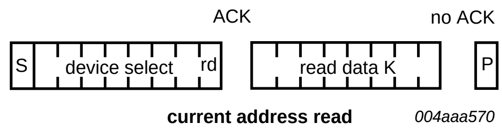


Fig 8. Current address read

9.3.4.2 Random address read: single read

Table 42 describes the transfer format for a single-byte read. Figure 9 illustrates the byte sequence.

Table 42. Transfer format description for a single-byte read

SDA line	Description
S	master starts with a START condition
Device select	master transmits the device address and write command bit R/W = 0
ACK	slave generates an acknowledgment
Register address K	master transmits (start) address of register K from which to be read
ACK	slave generates an acknowledgment
S	master restarts with a START condition
Device select	master transmits the device address and read command bit R/W = 1
ACK	slave generates an acknowledgment
Read data K	slave transmits and master reads data from register K
No ACK	master terminates the read operation by generating a no acknowledgement
P	master generates a STOP condition

9.3.4.3 Random address read: multiple read

The transfer format description for a multiple-byte read is given in Table 43. Figure 9 illustrates the byte sequence.

Table 43. Transfer format description for a multiple-byte read

SDA line	Description
S	master starts with a START condition
Device select	master transmits the device address and write command bit R/W = 0
ACK	slave generates an acknowledgment
Register address K	master transmits (start) address of register K from which to be read
ACK	slave generates an acknowledgment
S	master restarts with a START condition
Device select	master transmits the device address and read command bit R/W = 1
ACK	slave generates an acknowledgment
Read data K	slave transmits and master reads data from register K. After a byte is read, the address is automatically incremented by 1.
ACK	master generates an acknowledgment
Read data K + 1	slave transmits and master reads data from register K + 1
ACK	master generates an acknowledgment
:	:

Table 43. Transfer format description for a multiple-byte read *...continued*

SDA line	Description
Read data K + N – 1	slave transmits and master reads data register K + N – 1. This is the last register to read. After incrementing, the address rolls over to 0. Here, N represents the number of addresses available in the slave.
No ACK	master terminates the read operation by generating a no acknowledgement
P	master generates a STOP condition

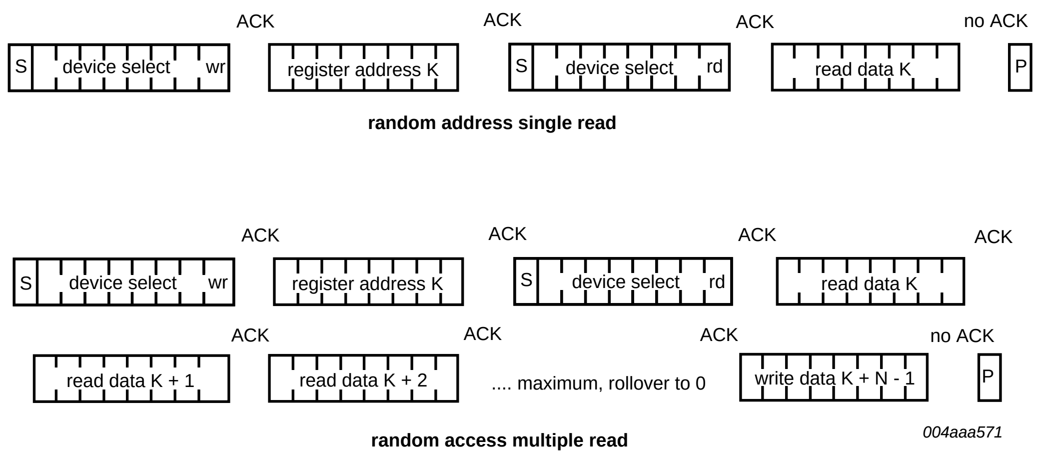


Fig 9. Random address read

10. Clock wake-up scheme

The following subsections explain the ISP1302UK clock stop timing, events triggering the clock to wake up, and the timing of the clock wake-up.

10.1 Power-down event

The internal clock (LazyClock and/or I^{2}C-bus clock) is stopped when bit PWR_DN is set. It takes $t_{d(clkstp)}$ for the clock to stop from the time the power-down condition is detected. The clock always stops at its falling edge.

The internal clock must be woken up first before any register read or write operation.

10.2 Clock wake-up event

The clock wakes up when any of the following events occurs on the ISP1302UK pins:

- Pin SCL goes LOW.
- Pin V_{BUS} goes above the session valid threshold, provided bit SESS_VLD_IEH of the Interrupt Enable High register is set.
- Status bit ID_FLOAT changes from logic 1 to logic 0, provided bit ID_FLOAT_IEL of the Interrupt Enable Low register is set.
- Status bit ID_FLOAT changes from logic 0 to logic 1, provided bit ID_FLOAT_IEH of the Interrupt Enable High register is set.

- DP goes HIGH provided the DP_HI_IEH bit in the Interrupt Enable High register is set.
- DM goes HIGH provided the DM_HI_IEH bit in the Interrupt Enable High register is set.

The event triggers the clock to start. The clock start-up time is $t_{startup(lclk)}$. A stable clock is guaranteed after six clock cycles. The clock will always start at its rising edge.

When an event is triggered and the clock is started, the clock will remain active for $t_{d(clkstp)}$. If bit PWR_DN is not cleared within this period, the clock will stop. If the clock wakes up because of any event other than SCL going LOW, an interrupt will be generated once the clock is active.

11. Limiting values

Table 44. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
Voltage						
V_{CC}	supply voltage			–0.5	+5.5[1]	V
$V_{CC(I/O)}$	input/output supply voltage			–0.5	+4.6	V
V_I	input voltage	on digital pins ADR/PSW, SERVICE_N and RESET_N		–0.5	+4.6	V
		on all other digital pins		–0.5	$V_{CC(I/O)}$ + 0.5	V
		on analog pins DP and DM		–0.5	+4.6[2]	V
$V_{I(VBUS)}$	input voltage on pin V_{BUS}			–0.5	+7.0[3]	V
$V_{I(ID)}$	input voltage on pin ID			–0.5	+5.5	V
V_{ESD}	electrostatic discharge voltage					
		Human Body Model (JESD22-A114D)	[4]	–2	+2	kV
		Machine Model (JESD22-A115-A)		–200	+200	V
		Charge Device Model (JESD22-C101-C)		–500	+500	V
Current						
I_{lu}	latch-up current			-	100	mA
Temperature						
T_{stg}	storage temperature			–60	+125	°C
T_j	junction temperature			–40	+125	°C

[1] When the charge pump is enabled, +5.5 V is only allowed for short period of time ≤ 1 second.

[2] The ISP1302UK has been tested according to *Universal Serial Bus Specification Rev. 2.0, Section 7.1.1*. The DP and DM lines were shorted to V_{BUS}/GND for 24 hours with 50 % transmit/receive duty cycle. The ISP1302UK operated normally after this test and is therefore compliant to the requirement.

[3] When an external series resistor is added to the V_{BUS} pin, it can withstand higher voltages for longer periods of time because the resistor limits the current flowing into the V_{BUS} pad. For example, with an external 1 kΩ resistor, V_{BUS} can tolerate 10 V for at least 5 seconds. If an external resistor is used, the internal charge pump must never be used, and other OTG functions must be verified in the customer application.

[4] Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ resistor (Human Body Model).

12. Recommended operating conditions

Table 45. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Voltage						
V_{CC}	supply voltage		3.0	-	4.5	V
$V_{CC(I/O)}$	input/output supply voltage		1.4	-	3.6[1]	V
V_I	input voltage	digital pins ADR/PSW, SERVICE_N and RESET_N	0	-	3.6	V
		on all other digital pins	0	-	$V_{CC(I/O)}$	V
		on analog pins DP and DM	0	-	3.6	V

Table 45. Recommended operating conditions *...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(pu)OD}$	open-drain pull-up voltage		1.4	-	3.6	V
Temperature						
T_{amb}	ambient temperature		–40	-	+85	°C

[1] $V_{CC(I/O)}$ should be less than or equal to V_{CC}.

13. Static characteristics

Table 46. Static characteristics: supply pins
V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 1.4 V to 3.6 V; T_{amb} = –40 °C to +85 °C; unless otherwise specified.
Typical values are at V_{CC} = 3.3 V; $V_{CC(I/O)}$ = 3.3 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Voltage							
$V_{O(VREG)}$	output voltage on pin VREG	bit UART_2V8_EN = 0; I_{load} ≤ 300 µA[1]		3.0[2]	-	3.6	V
		bit UART_2V8_EN = 1 and bit UART_EN = 1; I_{load} ≤ 10 mA		2.35	-	2.85	V
$V_{POR(trip)}$	power-on reset trip voltage			1.5	-	2.5	V
Current							
I_{CC}	supply current	transmitting and receiving at 12 Mbit/s; C_L = 50 pF on pins DP and DM	[3]	-	5	8	mA
$I_{CC(I/O)}$	supply current on pin $V_{CC(I/O)}$	transmitting and receiving at 12 Mbit/s	[3]	-	1	2	mA
$I_{CC(I/O)(isol)}$	isolate mode supply current on pin $V_{CC(I/O)}$	V_{CC} not connected		-	-	10	µA
$I_{CC(idle)}$	idle and SE0 supply current	idle: V_{DP} > 2.7 V, V_{DM} < 0.3 V; SE0: V_{DP} < 0.3 V, V_{DM} < 0.3 V	[4]	-	0.5	1	mA
$I_{CC(I/O)(stat)}$	static supply current on pin $V_{CC(I/O)}$	idle, SE0 or suspend		-	-	20	µA
$I_{CC(stat)}$	static supply current	(bit PWR_DN = 1 and bit SUSPEND = 1 and bit SPEED = 1) or $V_{CC(I/O)}$ = 0 V	[4]	-	12	25	µA

[1] I_{load} includes the DP pull-up resistor current.

[2] In power-down mode, the minimum voltage is 2.7 V.

[3] Maximum value characterized only, not tested in production.

[4] Excluding any load current to the 1.5 kΩ and 15 kΩ pull-up and pull-down resistors (200 µA typical).

Table 47. Static characteristics: digital pins
V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 1.4 V to 3.6 V; T_{amb} = –40 °C to +85 °C; unless otherwise specified.
Typical values are at V_{CC} = 3.3 V; $V_{CC(I/O)}$ = 3.3 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Input level voltage						
V_{IL}	LOW-level input voltage		-	-	$0.3V_{CC(I/O)}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{CC(I/O)}$	-	-	V

Table 47. Static characteristics: digital pins *…continued*

V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 1.4 V to 3.6 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.
Typical values are at V_{CC} = 3.3 V; $V_{CC(I/O)}$ = 3.3 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Output level voltage							
V_{OL}	LOW-level output voltage	I_{OL} = 2 mA		-	-	0.4	V
		I_{OL} = 100 μA		-	-	0.15	V
V_{OH}	HIGH-level output voltage	I_{OH} = 2 mA	[1]	$V_{CC(I/O)}$ − 0.4	-	-	V
		I_{OH} = 100 μA		$V_{CC(I/O)}$ − 0.15	-	-	V
Leakage current							
I_{LI}	input leakage current			−1	-	+1	μA
Open-drain output current							
I_{OZ}	off-state output current			−5	-	+5	μA
Capacitance							
C_{in}	input capacitance	pin to ground		-	-	10	pF

[1] Not applicable for open-drain outputs.

Table 48. Static characteristics: analog I/O pins DP and DM

V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 1.4 V to 3.6 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.
Typical values are at V_{CC} = 3.3 V; $V_{CC(I/O)}$ = 3.3 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Input level voltage							
V_{DI}	differential input sensitivity	$\|V_{DP} - V_{DM}\|$		0.2	-	-	V
V_{CM}	differential common mode voltage range	includes V_{DI} range		0.8	-	2.35	V
V_{IL}	LOW-level input voltage			-	-	0.8	V
V_{IH}	HIGH-level input voltage			2.0	-	-	V
Output level voltage							
V_{OL}	LOW-level output voltage	R_L of 1.5 kΩ to +3.6 V		-	-	0.3	V
V_{OH}	HIGH-level output voltage	R_L of 15 kΩ to ground		2.8	-	3.6	V
Voltage							
V_{TERM}	termination voltage		[1]	3.0	-	3.6	V
Leakage current							
I_{LZ}	off-state leakage current			−1	-	+1	μA
Capacitance							
C_{in}	input capacitance	pin to AGND		-	-	10	pF
Resistance							
$R_{DN(DP)}$	pull-down resistance on pin DP			14.25	-	24.8	kΩ
$R_{DN(DM)}$	pull-down resistance on pin DM			14.25	-	24.8	kΩ
$R_{UP(DP)}$	pull-up resistance on pin DP	bus idle		900	-	1575	Ω
		bus driven		1425	-	3090	Ω
$R_{weakUP(DP)}$	weak pull-up resistance on pin DP			105	-	195	kΩ
Z_{DRV}	driver output impedance	steady-state drive	[2]	34	-	44	Ω

Table 48. Static characteristics: analog I/O pins DP and DM *...continued*

V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 1.4 V to 3.6 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.
Typical values are at V_{CC} = 3.3 V; $V_{CC(I/O)}$ = 3.3 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Z_{INP}	input impedance		1	-	-	MΩ

[1] For the upstream port pull-up resistance (R_{PU}).

[2] Includes external series resistances of 33 Ω ± 5 % each on DP and DM.

Table 49. Static characteristics: analog I/O pin ID

V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 1.4 V to 3.6 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.
Typical values are at V_{CC} = 3.3 V; $V_{CC(I/O)}$ = 3.3 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Resistance						
$R_{UP(int)(ID)}$	internal pull-up resistance on pin ID		70	-	130	kΩ
$R_{DN(ID)}$	pull-down resistance on pin ID	bit ID_PULLDOWN = 1; output pull-down resistance	-	-	120	Ω
$R_{DN(ext)(ID)}$	external pull-down resistance on pin ID	bit ID_FLOAT = 0	-	-	180	kΩ
		bit ID_FLOAT = 1	440	-	-	kΩ
		bit ID_GND = 0	23	-	-	kΩ
		bit ID_GND = 1	-	-	15	kΩ
$V_{(th)(det)(ID\_FLOAT)}$	ID_FLOAT detector threshold		1.8	-	2.5	V
$V_{(th)(det)(ID\_GND)}$	ID_GND detector threshold		0.3	-	0.7	V

Table 50. Static characteristics: charge pump

V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 1.4 V to 3.6 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.
Typical values are at V_{CC} = 3.3 V; $V_{CC(I/O)}$ = 3.3 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Current						
I_{load}	load current	C_{ext} = 220 nF; V_{BUS} > $V_{A\_VBUS\_VLD}$	50	-	-	mA
Voltage						
$V_{O(VBUS)}$	output voltage on pin V_{BUS}	I_{load} = 50 mA; C_{ext} = 220 nF	4.4	5	5.25	V
$V_{L(VBUS)}$	leakage voltage on pin V_{BUS}	charge pump disabled	-	-	0.2	V
$V_{A\_VBUS\_VLD}$	A-device V_{BUS} valid voltage		4.4	-	4.7	V
$V_{B\_SESS\_END}$	B-device session end voltage		0.2	-	0.8	V
$V_{A\_SESS\_VLD}$	A-device session valid voltage	bit ID_GND = 1	0.8	-	2.0	V
$V_{B\_SESS\_VLD}$	B-device session valid voltage	bit ID_GND = 0	0.8	-	4.0	V
$V_{hys(A\_SESS\_VLD)}$	A-device session valid hysteresis voltage		-	80	-	mV

Table 50. Static characteristics: charge pump *...continued*
V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 1.4 V to 3.6 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.
Typical values are at V_{CC} = 3.3 V; $V_{CC(I/O)}$ = 3.3 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{hys(B\_SESS\_VLD)}$	B-device session valid hysteresis voltage		-	80	-	mV
η_{cp}	charge pump efficiency	I_{load} = 50 mA; V_{CC} = 3 V [1]	-	75	-	%
Resistance						
$R_{UP(VBUS)}$	pull-up resistance on pin V_{BUS}	connect to VREG when bit VBUS_CHRG = 1	460	-	1000	Ω
$R_{DN(VBUS)}$	pull-down resistance on pin V_{BUS}	connect to ground when bit VBUS_DISCHRG = 1	660	-	1200	Ω
$R_{I(idle)(VBUS)}$	idle input resistance on pin V_{BUS}	bit VBUS_DRV = 0	52.5	-	100	kΩ
		bit VBUS_DRV = 1 or V_{CC} is not powered	250	-	500	kΩ
Capacitance						
C_{ext}	external capacitance	I_{load} = 8 mA	20	-	-	nF
		I_{load} = 20 mA	61	-	-	nF
		I_{load} = 25 mA	90	-	-	nF
		I_{load} = 50 mA	198	-	-	nF

[1] Efficiency when loaded.

14. Dynamic characteristics

Table 51. Dynamic characteristics: reset and clock

V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 1.4 V to 3.6 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.
Typical values are at V_{CC} = 3.3 V; $V_{CC(I/O)}$ = 3.3 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Reset							
$t_{W(RESET\_N)}$	external RESET_N pulse width			10	-	-	µs
Internal clock							
f_{clk}	clock frequency	bit PWR_DN = 0	[1]	50	-	150	kHz
f_{clk_I2C}	I^2C-bus clock frequency			3.5	-	8.0	MHz
$t_{startup(lclk)}$	LazyClock start-up time			7	-	13	µs
$t_{d(clkstp)}$	clock stop delay time			5	-	10	ms

[1] LazyClock for interrupts, registers, and power-down and wake-up timer.

Table 52. Dynamic characteristics: V_{BUS} comparator timing

V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 1.4 V to 3.6 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.
Typical values are at V_{CC} = 3.3 V; $V_{CC(I/O)}$ = 3.3 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{d(VA\_VBUS\_VLD)}$	$V_{A\_VBUS\_VLD}$ delay time		20	-	300	µs

Table 53. Dynamic characteristics: bus turnaround timing (USB bidirectional mode)

V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 1.4 V to 3.6 V; C_L = 50 pF; R_{PU} = 1.5 kΩ on DP to V_{TERM}; T_{amb} = −40 °C to +85 °C; unless otherwise specified.
Typical values are at V_{CC} = 3.3 V; $V_{CC(I/O)}$ = 3.3 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{TOI}	bus turnaround time (O/I)	OE_N/INT_N to DAT/VP and SE0/VM; see Figure 14	0	-	5	ns
t_{TIO}	bus turnaround time (I/O)	OE_N/INT_N to DAT/VP and SE0/VM; see Figure 14	0	-	5	ns

Table 54. Dynamic characteristics: analog I/O pins DP and DM

V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 1.4 V to 3.6 V; C_L = 50 pF; R_{PU} = 1.5 kΩ on DP to V_{TERM}; T_{amb} = −40 °C to +85 °C; unless otherwise specified.
Typical values are at V_{CC} = 3.3 V; $V_{CC(I/O)}$ = 3.3 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Driver characteristics (low-speed)							
t_{LR}	transition time: rise time	C_L = 200 pF to 600 pF; 1.5 kΩ pull-up on pin DM enabled; 10 % to 90 % of $\lvert V_{OH} - V_{OL}\rvert$; see Figure 10		75	-	300	ns
t_{LF}	transition time: fall time	C_L = 200 pF to 600 pF; 1.5 kΩ pull-up on pin DM enabled; 90 % to 10 % of $\lvert V_{OH} - V_{OL}\rvert$; see Figure 10		75	-	300	ns
FRFM	differential rise time/fall time matching	excluding the first transition from idle state	[1]	80	-	125	%

Table 54. Dynamic characteristics: analog I/O pins DP and DM *...continued*

V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 1.4 V to 3.6 V; C_L = 50 pF; R_{PU} = 1.5 kΩ on DP to V_{TERM}; T_{amb} = −40 °C to +85 °C; unless otherwise specified.
Typical values are at V_{CC} = 3.3 V; $V_{CC(I/O)}$ = 3.3 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{CRS}	output signal crossover voltage	excluding the first transition from idle state; see Figure 11		1.3	-	2.0	V
Driver characteristics (full-speed)							
t_{FR}	rise time	C_L = 50 pF; 10 % to 90 % of $\|V_{OH} - V_{OL}\|$; see Figure 10		4	-	20	ns
t_{FF}	fall time	C_L = 50 pF; 90 % to 10 % of $\|V_{OH} - V_{OL}\|$; see Figure 10		4	-	20	ns
FRFM	differential rise time/fall time matching	excluding the first transition from idle state	[1]	90	-	111.1	%
V_{CRS}	output signal crossover voltage	excluding the first transition from idle state; see Figure 11		1.3	-	2.0	V
Driver timing							
$t_{PLH(drv)}$	driver propagation delay (LOW to HIGH)	DAT/VP, SE0/VM to DP, DM; see Figure 11 and Figure 15		-	-	18	ns
$t_{PHL(drv)}$	driver propagation delay (HIGH to LOW)	DAT/VP, SE0/VM to DP, DM; see Figure 11 and Figure 15		-	-	18	ns
t_{PHZ}	HIGH to OFF-state propagation delay	OE_N/INT_N to DP, DM; see Figure 12 and Figure 16		-	-	15	ns
t_{PLZ}	LOW to OFF-state propagation delay	OE_N/INT_N to DP, DM; see Figure 12 and Figure 16		-	-	15	ns
t_{PZH}	OFF-state to HIGH propagation delay	OE_N/INT_N to DP, DM; see Figure 12 and Figure 16		-	-	15	ns
t_{PZL}	OFF-state to LOW propagation delay	OE_N/INT_N to DP, DM; see Figure 12 and Figure 16		-	-	15	ns
Receiver timing							
Differential receiver							
$t_{PLH(rcv)}$	receiver propagation delay (LOW to HIGH)	DP, DM to RCV; see Figure 13 and Figure 17		-	-	15	ns
$t_{PHL(rcv)}$	receiver propagation delay (HIGH to LOW)	DP, DM to RCV; see Figure 13 and Figure 17		-	-	15	ns
Single-ended receiver							
$t_{PLH(se)}$	single-ended propagation delay (LOW to HIGH)	DP, DM to DAT/VP, SE0/VM; see Figure 13 and Figure 17		-	-	18	ns
$t_{PHL(se)}$	single-ended propagation delay (HIGH to LOW)	DP, DM to DAT/VP, SE0/VM; see Figure 13 and Figure 17		-	-	18	ns

[1] t_{FR}/t_{FF}.

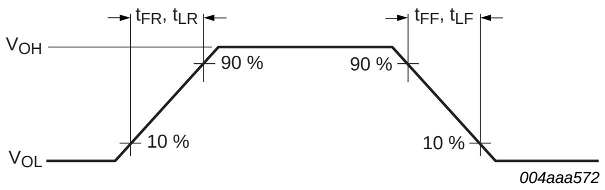


Fig 10. Rise time and fall time

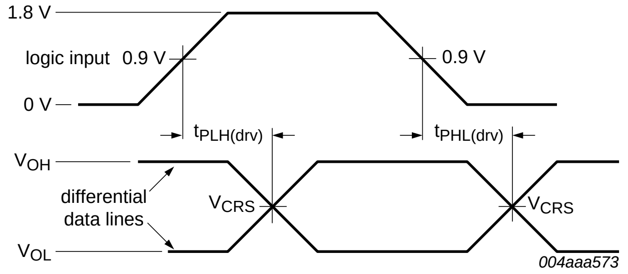


Fig 11. Timing of DAT/VP and SE0/VM to DP and DM

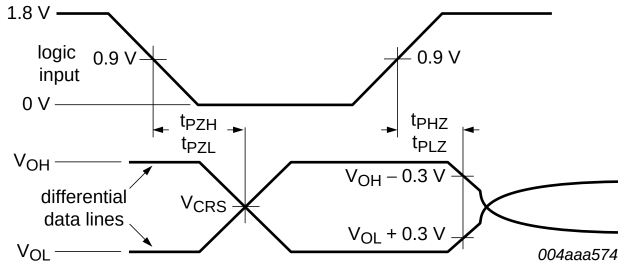


Fig 12. Timing of OE_N/INT_N to DP and DM

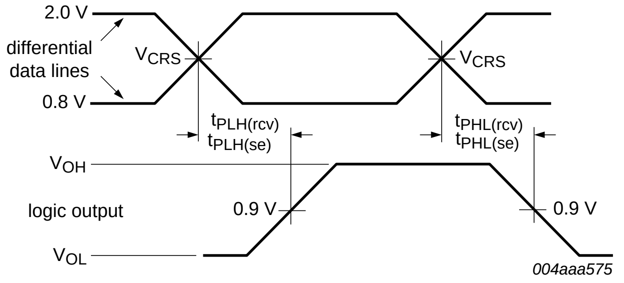


Fig 13. Timing of DP and DM to RCV, DAT/VP and SE0/VM

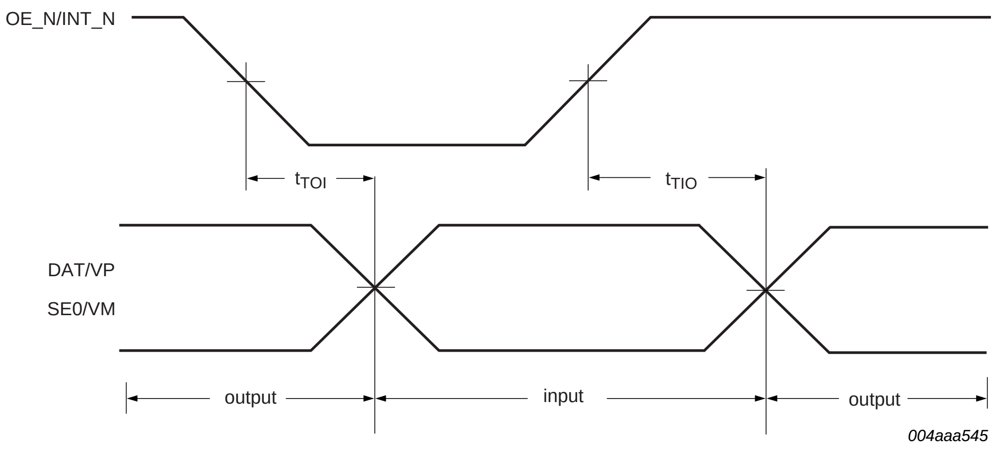
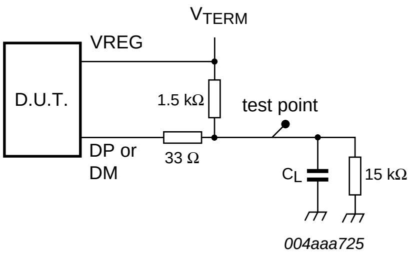
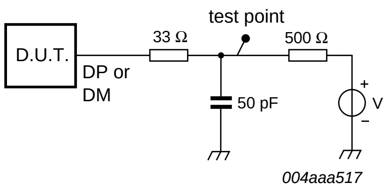


Fig 14. SIE interface bus turnaround timing



Load capacitance C_L = 50 pF (minimum or maximum timing).

Fig 15. Load on pins DP and DM



V = 0 V for t_{PZH} and t_{PHZ}.

V = VREG for t_{PZL} and t_{PLZ}.

Fig 16. Load on pins DP and DM for enable time and disable time

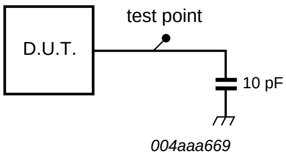


Fig 17. Load on pins SE0/VM, DAT/VP and RCV

14.1 I²C-bus characteristics

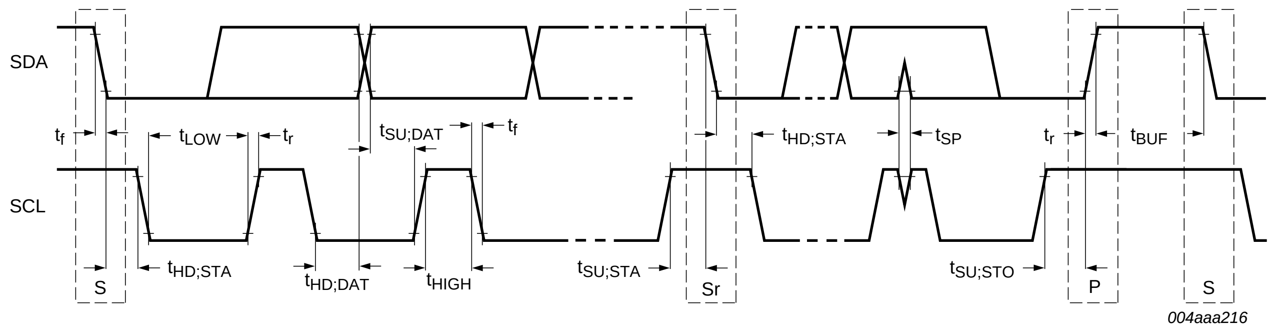


Fig 18. Definition of timing for standard mode or fast mode devices on the I²C-bus

Table 55. Characteristics of I/O stages of I²C-bus lines (SDA, SCL)

Symbol	Parameter	Conditions	Standard mode		Fast mode		Unit
			Min	Max	Min	Max	
f_{SCL}	SCL clock frequency		0	100	0	400	kHz
$t_{HD;STA}$	hold time (repeated) START condition		4.0	-	0.6	-	μs
t_{LOW}	LOW period of the SCL clock		4.7	-	1.3	-	μs
t_{HIGH}	HIGH period of the SCL clock		4.0	-	0.6	-	μs
$t_{SU;STA}$	set-up time for a repeated START condition		4.7	-	0.6	-	μs
$t_{SU;DAT}$	data set-up time		250	-	100	-	ns
$t_{HD;DAT}$	data hold time		0	-	0	0.9	μs
t_r	rise time of both SDA and SCL signals		-	1000	20 + 0.1C_b[1]	300	ns
t_f	fall time of both SDA and SCL signals		-	300	20 + 0.1C_b[1]	300	ns
$t_{SU;STO}$	set-up time for STOP condition		4.0	-	0.6	-	μs
t_{BUF}	bus free time between a STOP and START condition		4.7	-	1.3	-	μs
t_{SP}	pulse width of spikes that must be suppressed by the input filter		not applicable	not applicable	0	50	ns

[1] C_b is the capacitance load for each bus line in pF. If mixed with high-speed mode devices, faster fall times are allowed.

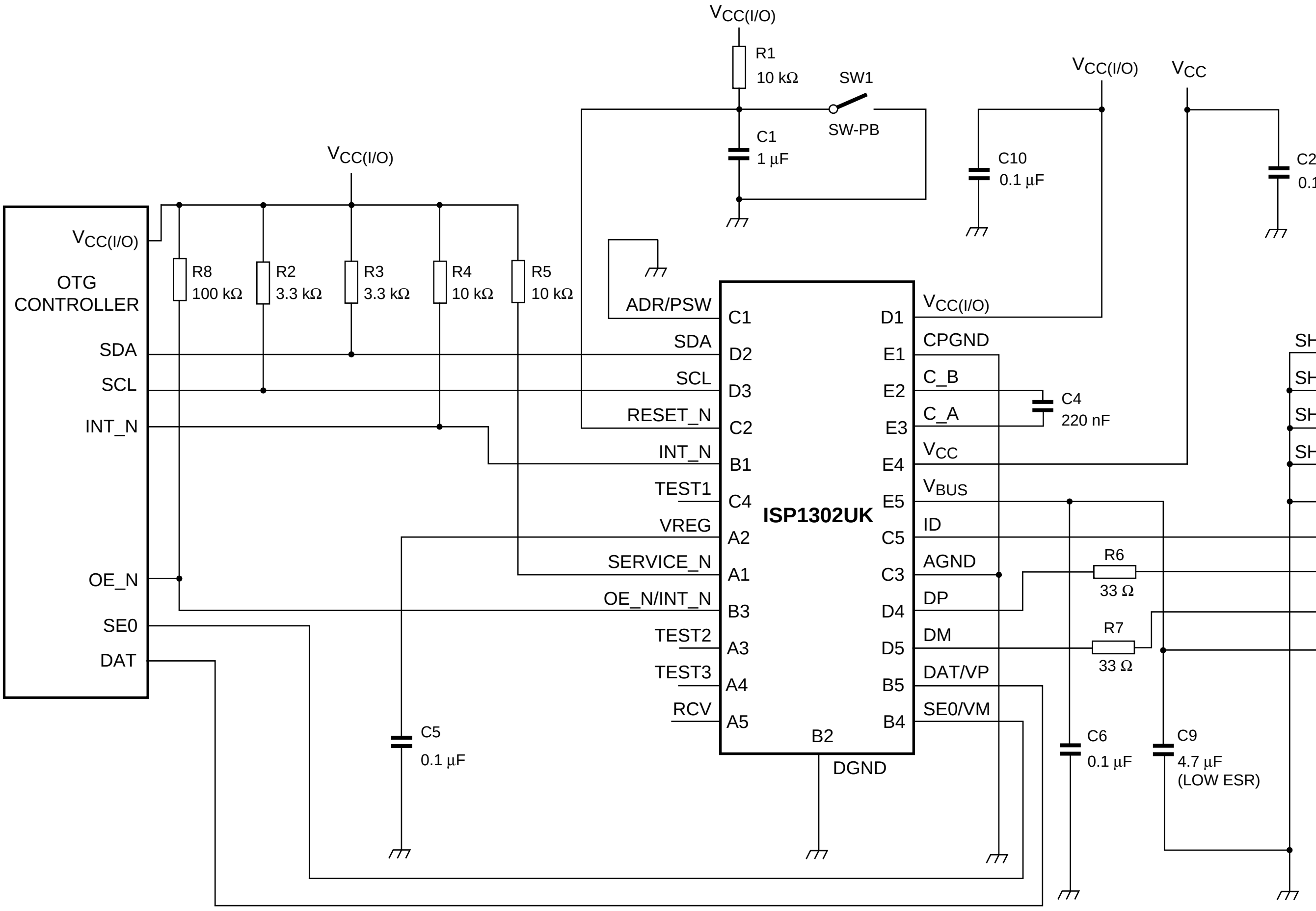
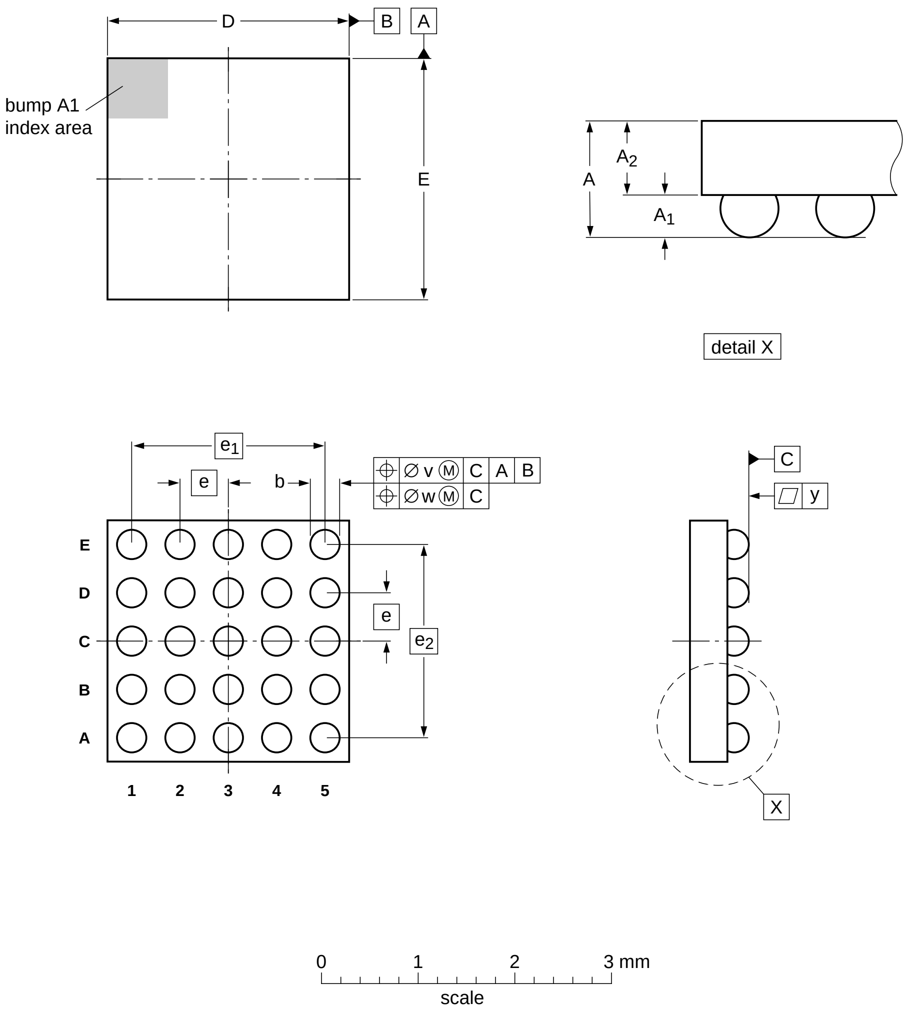


Fig 19. Application diagram

16. Package outline

WLCSP25: wafer level chip-size package; 25 bumps; 2.5 x 2.5 x 0.6 mm **ISP1302UK**



DIMENSIONS (mm are the original dimensions)

UNIT	A max	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y
mm	0.64	0.26 0.22	0.38 0.34	0.34 0.30	2.5 2.4	2.5 2.4	0.5	2	2	0.01	0.04	0.02

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
ISP1302UK						~~05-09-28~~ 05-09-30

Fig 20. Package outline ISP1302UK (WLCSP25)

17. Abbreviations

Table 56. Abbreviations

Acronym	Description
ATX	Analog USB Transceiver
HNP	Host Negotiation Protocol
I^{2}C-bus	Inter IC-bus
LSB	Least Significant Bit
OTG	On-The-Go
POR	Power-On Reset
PORP	Power-On Reset Pulse
RxD	Receive Data
SE0	Single-Ended Zero
SIE	Serial Interface Engine
SoC	System-on-a-Chip
SRP	Session Request Protocol
TxD	Transmit Data
UART	Universal Asynchronous Receiver-Transmitter
USB	Universal Serial Bus
WLCSP	Wafer-Level Chip-Scale Package

18. References

[1] Universal Serial Bus Specification Rev. 2.0

[2] On-The-Go Supplement to the USB 2.0 Specification Rev. 1.3

[3] On-The-Go Transceiver Specification (CEA-2011)

[4] ECN_27%_Resistor (Pull-up/pull-down Resistors ECN)

[5] The I^{2}C-bus specification; ver. 2.1

[6] Human Body Model (JESD22-A114D)

[7] Machine Model (JESD22-A115-A)

[8] Charge Device Model (JESD22-C101-C)

19. Revision history

Table 57. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
ISP1302UK_3	20090929	Product data sheet	-	ISP1302UK_2
Modifications:	• Rebranded to the ST-Ericsson template. • Table 1 “Ordering information”: updated. • Table 25 “Misc Control register (address S = 18h, C = 19h) bit description”: updated bit DP_WKPU_EN. • Section 9.2 “Interrupts”: added the last paragraph. • Table 44 “Limiting values”: removed I_{LI}. • Table 46 “Static characteristics: supply pins”: updated the conditions column for $I_{CC(stat)}$. • Table 49 “Static characteristics: analog I/O pin ID”: updated. • Table 50 “Static characteristics: charge pump”: updated $R_{I(idle)(VBUS)}$. • Table 51 “Dynamic characteristics: reset and clock”: updated f_{clk_I2C} and $t_{d(clkstp)}$. • Removed soldering information.			
ISP1302UK_2	20090202	Product data sheet	-	ISP1302_1
ISP1302_1	20070524	Product data sheet	-	-

20. Tables

21. Figures

22. Contents

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