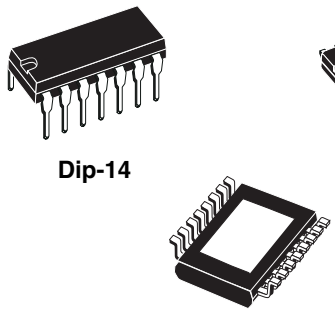
STP04CM05

4-bit constant current power-LED sink driver

Features

- 4 constant current output channels
- Adjustable output current through one external resistor
- Can be driven by a 3.3 V microcontroller
- Serial data IN/parallel data OUT
- Output current: 80-400 mA
- 20 V of output driving capability
- 30 MHz clock frequency
- UVLO (under voltage lockout) and POR (power ON reset)
- TSD, thermal shutdown, output off when junction temperature exceeds limit
- Operating free-air temperature range -40 to 125 ºC
- ESD protection 2.5 kV HBM, 200 V MM
- Available in high thermal TSSOP exposed pad.



Description

The STP04CM05 is a high-power LED driver and 4-bit shift register designed for Power-LED applications.

The STP04CM05 contains a 4-bit serial IN, parallel OUT shift register that feeds a 4-bit D-type storage register. In the output stage, four regulated current sources were designed to provide 80-400 mA constant current to drive high power LEDs.

The STP04CM05 guarantees 20 V output driving capability, allowing users to connect more LEDs in series. The high clock frequency, 30 MHz, also satisfies the system requirements which include high volume data transmission.

The STP04CM05 is well suited for very high brightness displays and special lighting applications.

The STP04CM05 is offered in DIP-14, SO-14 and TSSOP16 exposed pad packages.

Table 1. Device summary

Order codes	Package	Packaging
STP04CM05B1R	DIP-14	25 parts per tube
STP04CM05MTR	SO-14 (tape and reel)	2500 parts per reel
STP04CM05XTTR	TSSOP16 exposed-pad (tape and reel)	2500 parts per reel

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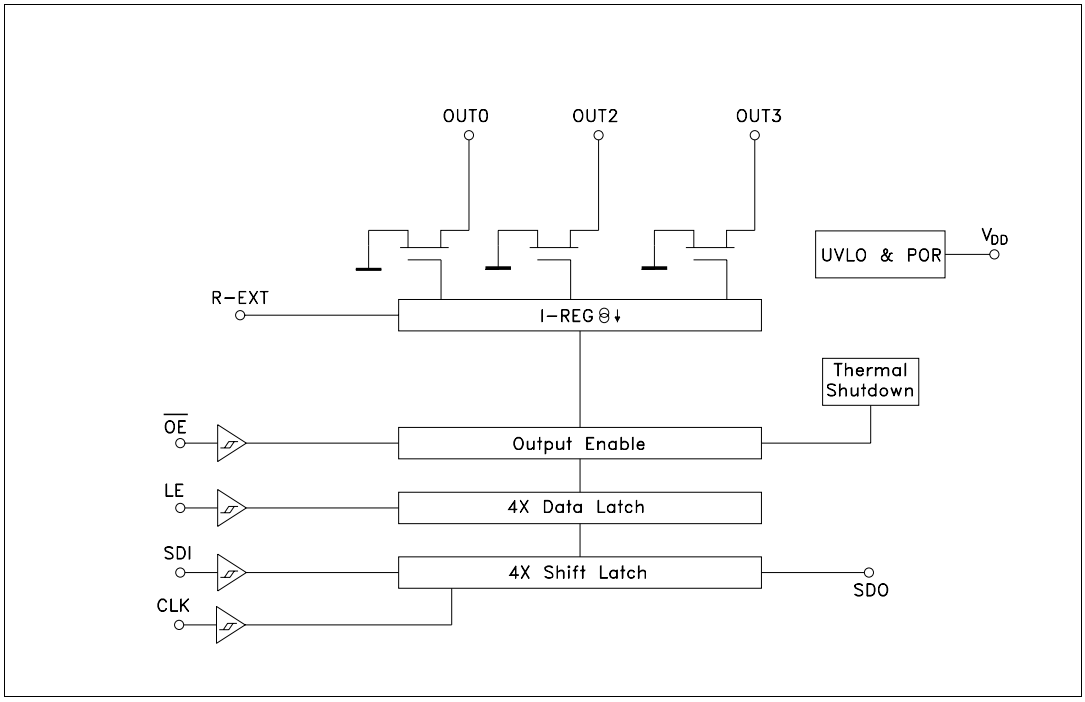
1 Internal schematic

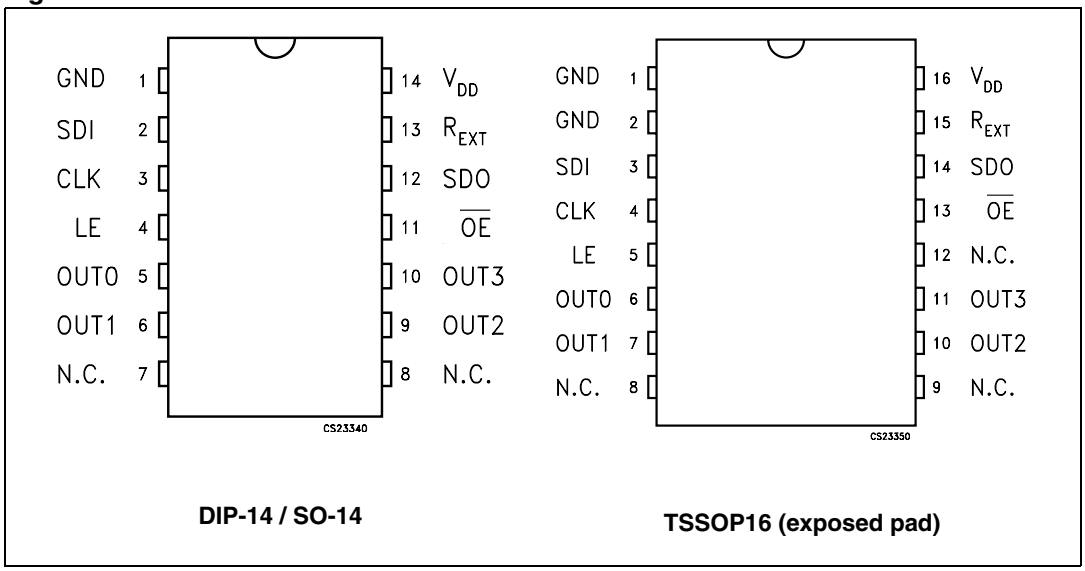
Figure 1. Block diagram



2 Pin settings

2.1 Pin connection

Figure 2. Pin connection



Note: The Exposed-pad is electrically not connected

2.2 Pin description

Table 2. Pin description

DIP-14 and SO-14 pin N°	TSSOP16 pin N°	Symbol	Name and function
1	1, 2	GND	Ground terminal
2	3	SDI	Serial data input terminal
3	4	CLK	Clock input terminal
4	5	LE	Latch input terminal
5	6	OUT 0	Output terminal
6	7	OUT 1	Output terminal
7, 8	8, 9, 12	N.C.	Not connected
9	10	OUT 2	Output terminal
10	11	OUT 3	Output terminal
11	13	$\overline{OE}$	Output enable input terminal (active low)
12	14	SDO	Serial data out terminal
13	15	R-EXT	Constant current programming
14	16	V_{DD}	5 V supply voltage terminal

3 Maximum rating

Stressing the device above the rating listed in the “absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DD}	Supply voltage	0 to 7	V
V_O	Output voltage	-0.5 to 20	V
I_O	Output current	500	mA
V_I	Input voltage	-0.4 to V_{DD}+0.4	V
I_{GND}	GND terminal current	2000	mA
f_{CLK}	Clock frequency	50	MHz
T_{OPR}	Operating temperature range	-40 to +125	°C
T_{STG}	Storage temperature range	-55 to +150	°C

3.1 Thermal data

Table 4. Thermal data

Symbol	Parameter	DIP-14	SO-14	TSSOP16	Unit
R_{thJA}	Thermal resistance junction-ambient	70 (1)	105 (2)	37.5 (3)	°C/W

1. 1 W of dissipated power, mounted on the board
2. 1 W of dissipated power, mounted on SM PCB1 SGS board
3. Using the PCB Multi-Layer JEDEC Standard test boards

3.2 Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{DD}	Supply voltage		3.3	5.0	5.5	V
V_O	Output voltage				19	V
I_O	Output current	OUTn V_{DD} = 5 V	80		400	mA
I_{OH}	Output current	Serial-OUT			+1	mA
I_{OL}	Output current	Serial-OUT			-1	mA
V_{IH}	Input voltage		0.7V_{DD}		V_{DD}+0.3	V
V_{IL}	Input voltage		-0.3		0.3V_{DD}	V
t_{wEN}	$\overline{OE}$ pulse width	V_{DD} = 5 V, I_O = 350 mA	80	50		ns
		V_{DD} = 3.3 V, I_O = 350 mA	250	150		
t_{wLAT}	LE pulse width	V_{DD} = 3.0 to 3.6 V	8	4		ns
t_{wCLK}	CLK pulse width		8.5	7.5		ns
$t_{SETUP(D)}$	Setup time for DATA		8.5	7.5		ns
$t_{HOLD(D)}$	Hold time for DATA		8.5	7.5		ns
$t_{SETUP(L)}$	Setup time for LATCH		8.5	7.0		ns
$t_{HOLD(E)}$	Hold time for ENABLE		8.5	7.0		ns
f_{CLK}	Clock frequency	Cascade operation (1)			30	MHz
T_{OPR}	Operating temperature range		-40		+125	°C

1. If multiple devices are cascaded, it may not be possible achieve the maximum data transfer. Please consider the timing conditions carefully.

4 Electrical characteristics

Table 6. Current accuracy

Output voltage	Current accuracy		Output current
	Between bits	Between ICs	
≥ 1.4 V	Typ. ± 1 %	± 6 %	80 to 400 mA

Table 7. Electrical characteristics
(V_{DD} = 3.3 to 5 V, T_A = 25°C, unless otherwise specified.)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{IH}	Input voltage high level		0.7 V_{DD}		V_{DD}	V
V_{IL}	Input voltage low level		GND		0.3 V_{DD}	V
I_{OH}	Output leakage current	V_{OH} = 19 V			10	µA
V_{OL}	Output voltage (Serial-OUT)	I_{OL} = 1 mA			0.4	V
V_{OH}	Output voltage (Serial-OUT)	I_{OH} = -1 mA	V_{DD}-0.4V			V
I_{OL1}	Output current	V_O = 0.3 VR_{EXT} = 980 Ω	75.2	80	84.8	mA
I_{OL2}		V_O = 1.2 VR_{EXT} = 190 Ω	376	400	424	mA
ΔI_{OL1}	Output current error between bit (All Output ON)	V_O = 0.3 VR_{EXT} = 980 Ω I_O = 80 mA		1	1.5	%
ΔI_{OL2}		V_O = 1.2 VR_{EXT} = 190 Ω I_O = 400 mA		1	1.5	%
$R_{SIN(up)}$	Pull-up resistor		150	300	600	KΩ
$R_{SIN(down)}$	Pull-down resistor		100	200	400	KΩ
$I_{DD(OFF1)}$	Supply current (OFF)	R_{EXT} = OPEN OUT 0 to 3 = OFF		1	1.5	mA
$I_{DD(OFF2)}$		R_{EXT} = 980 Ω OUT 0 to 3 = OFF		3.8	6	
$I_{DD(OFF3)}$		R_{EXT} = 190 Ω OUT 0 to 3 = OFF		14	18.5	
$I_{DD(ON1)}$	Supply current (ON)	R_{EXT} = 980 Ω OUT 0 to 3 = ON		4.0	6.0	
$I_{DD(ON2)}$		R_{EXT} = 190 Ω OUT 0 to 3 = ON		14.5	19	

Table 8. Switching characteristics
(V_{DD} = 3.3 to 5 V, T = 25 °C, unless otherwise specified.)

Symbol	Parameter	Test conditions		Min	Typ	Max	Unit
t_{PLH1}	Propagation delay time, CLK-$\overline{OUTn}$, LE = H, /$\overline{OE}$ = L	R_L = 5.0 Ω C_L = 10 pF I_O = 350 mA R_{ext} = 224 Ω V_L = 3.0 V	V_{DD} = 3.3 V		82	130	ns
			V_{DD} = 5 V		45	61	
t_{PLH2}	Propagation delay time, LE-$\overline{OUTn}$, /$\overline{OE}$ = L		V_{DD} = 3.3 V		81	135	ns
			V_{DD} = 5 V		43	62	
t_{PLH3}	Propagation delay time, /$\overline{OE}$-$\overline{OUTn}$, LE = H		V_{DD} = 3.3 V		147	250	ns
			V_{DD} = 5 V		50	76	
t_{PLH}	Propagation delay time, CLK-SDO		V_{DD} = 3.3 V		8	12	ns
			V_{DD} = 5 V		6	8	
t_{PHL1}	Propagation delay time, CLK-$\overline{OUTn}$, LE = H, /$\overline{OE}$ = L		V_{DD} = 3.3 V		29	42	ns
			V_{DD} = 5 V		23	32	
t_{PHL2}	Propagation delay time, $\overline{LE}$-$\overline{OUTn}$, /$\overline{OE}$ = L		V_{DD} = 3.3 V		33	60	ns
			V_{DD} = 5 V		31	47	
t_{PHL3}	Propagation delay time, /$\overline{OE}$-$\overline{OUTn}$, LE = H		V_{DD} = 3.3 V		16	22	ns
			V_{DD} = 5 V		12	16	
t_{PHL}	Propagation delay time, CLK-SDO		V_{DD} = 3.3 V		9	13	ns
			V_{DD} = 5 V		6.5	9	
t_{ON}	Output rise time 10~90% of voltage waveform		V_{DD} = 3.3 V		85	135	ns
			V_{DD} = 5 V		50	76	
t_{OFF}	Output fall time 90~10% of voltage waveform		V_{DD} = 3.3 V		6.5	9	ns
			V_{DD} = 5 V		5	7	
t_r	CLK rise time (1)	V_O = 5.0 V R_{ext} = 224 Ω				5000	ns
t_f	CLK fall time (1)					5000	ns

1. In order to achieve high cascade data transfer, please consider tr/tf timings carefully.

5 Equivalent circuit of inputs and outputs

Figure 3. $\overline{OE}$ terminal

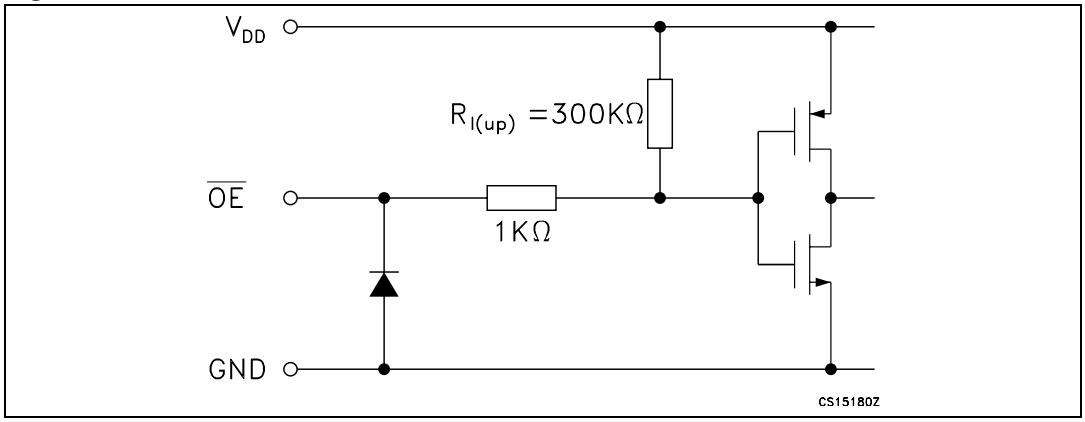


Figure 4. LE terminal

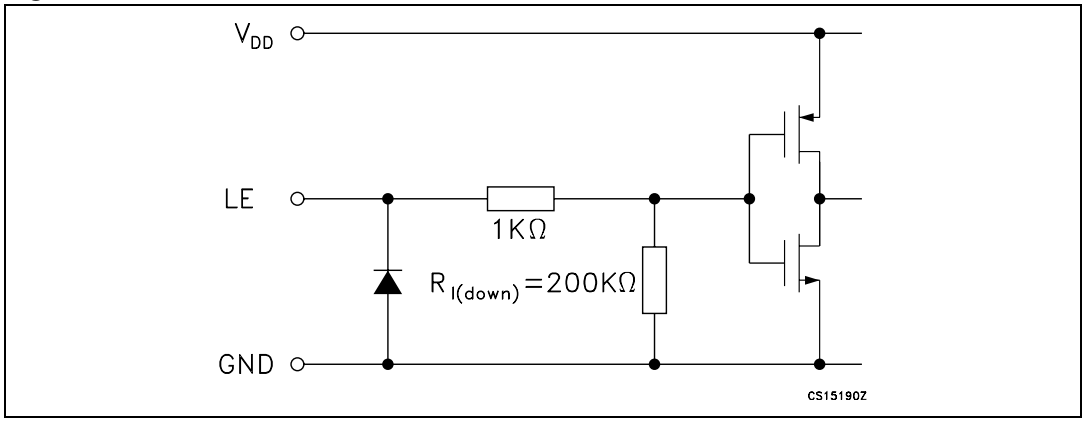


Figure 5. CLK, SDI terminal

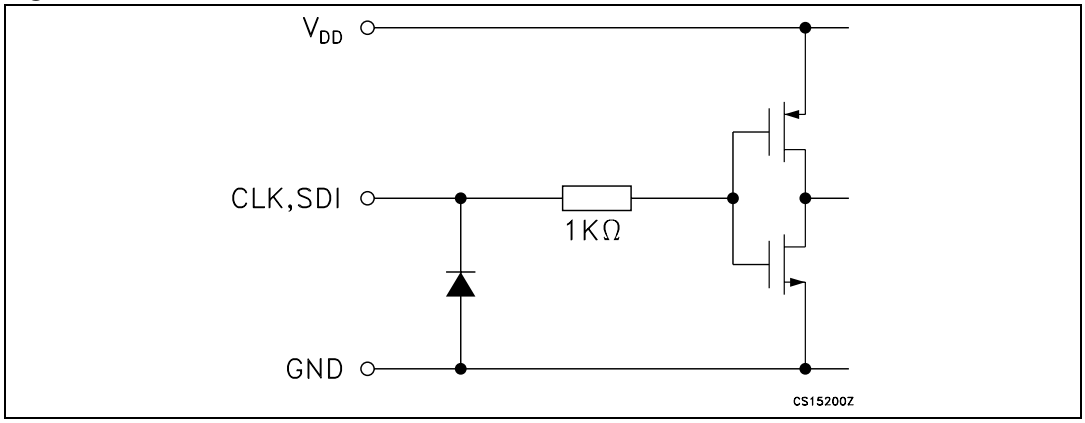
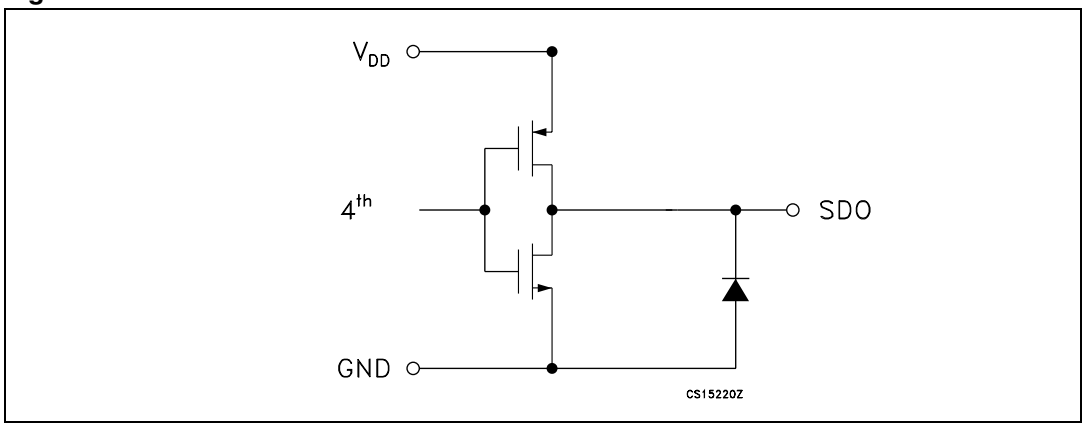
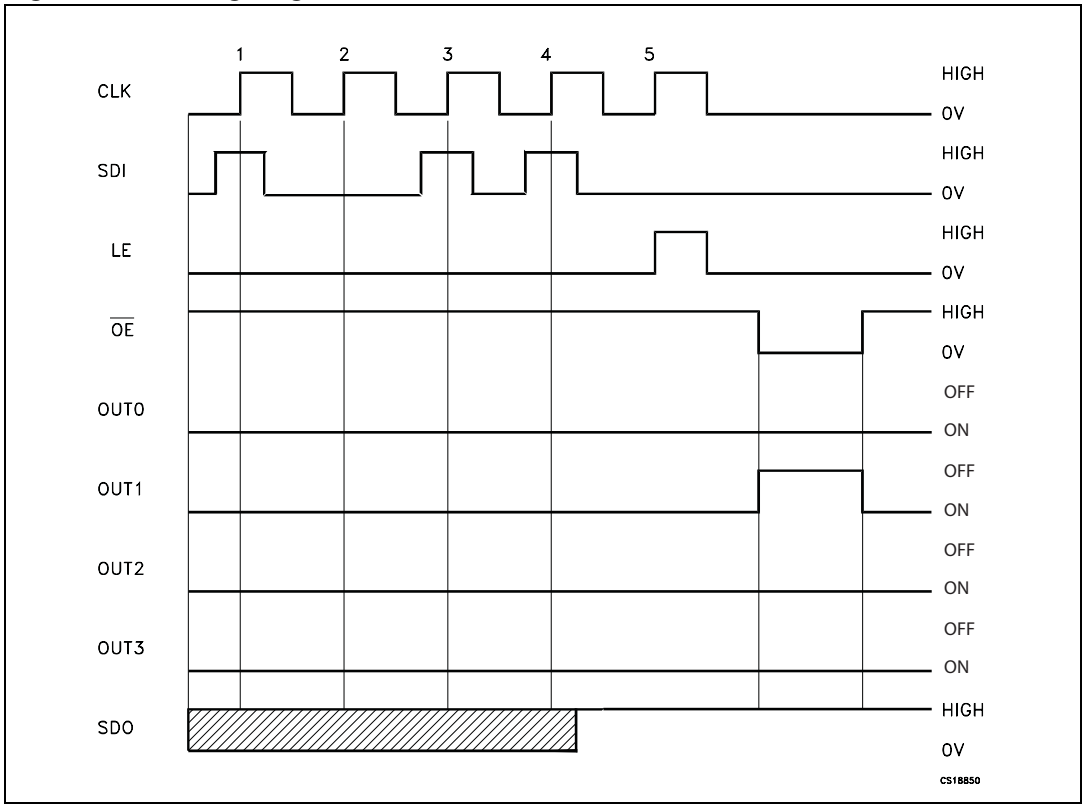


Figure 6. SDO terminal



6 Timing diagrams

Figure 7. Timing diagram



Note: The latches circuit holds data when the LE terminal is low.

1. *When the LE terminal is at a high level, the latch circuit holds the data it passes from the input to the output.*
2. *When the $\overline{OE}$ terminal is at a low level, the output terminals OUT0 to OUT3 respond to the data, either ON or OFF.*
3. *When the $\overline{OE}$ terminal is at a high level, it switches off all the data on the output terminal.*

Figure 8. Clock, serial-in, serial-out

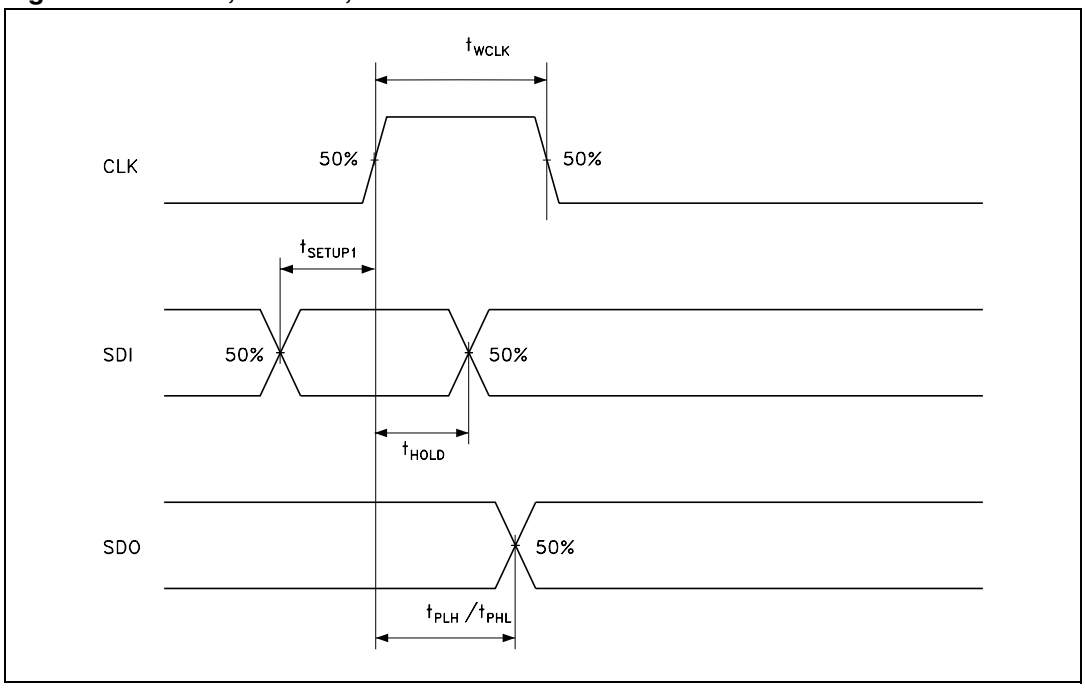


Figure 9. Clock, serial-in, latch, enable, outputs

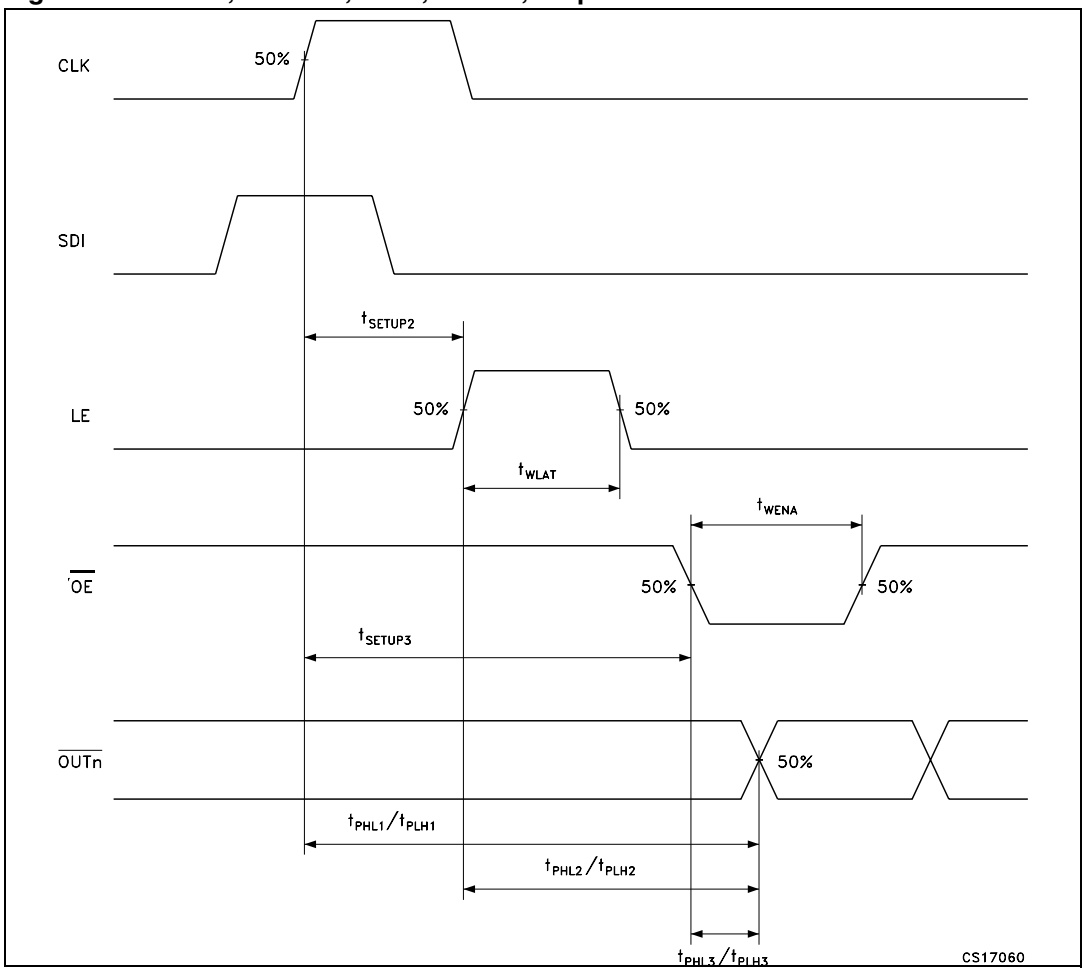
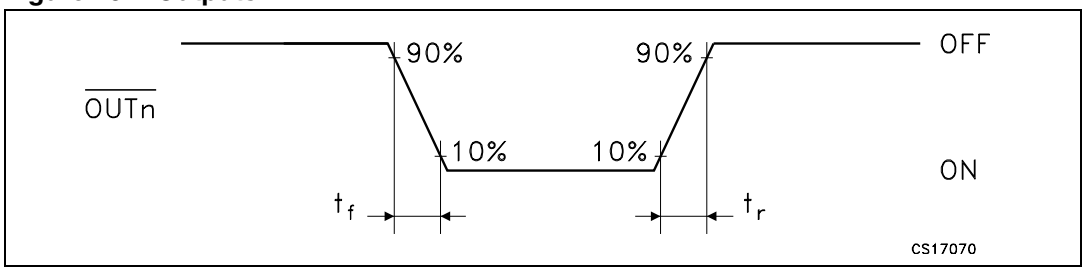


Figure 10. Outputs



7 Test circuit

Figure 11. DC characteristic

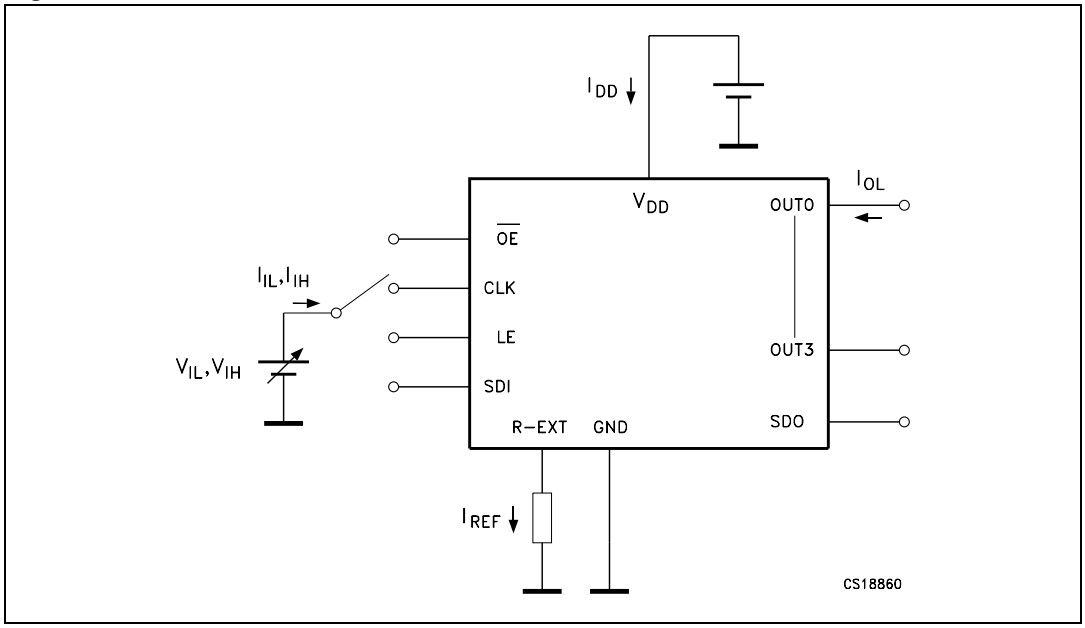
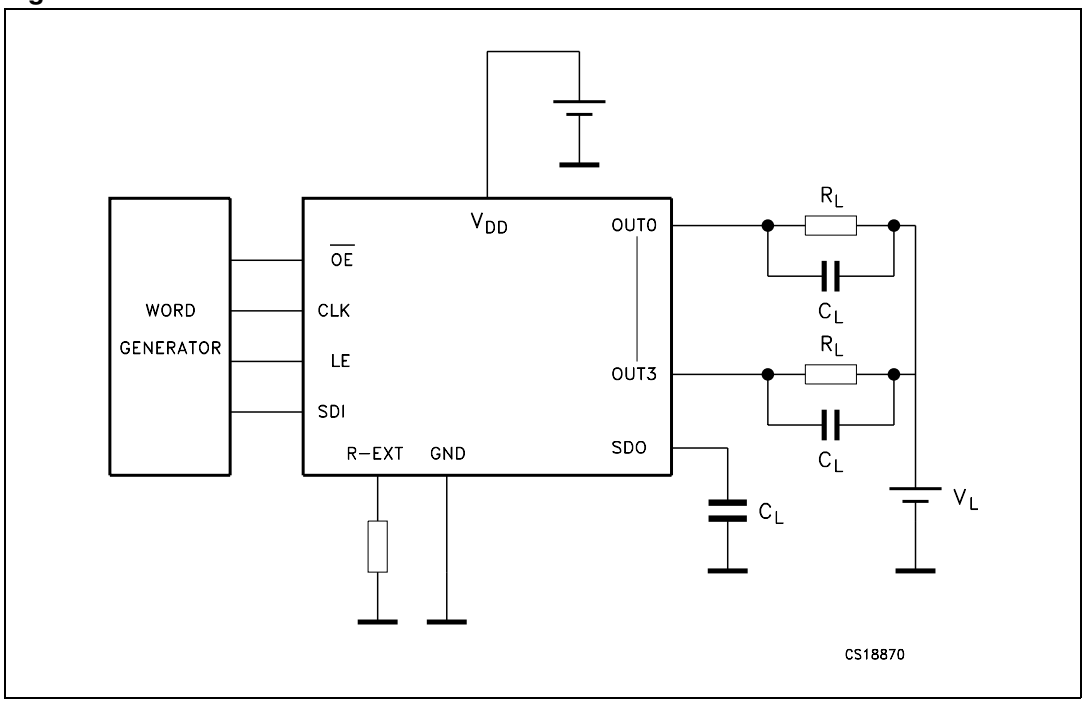


Figure 12. AC characteristic



8 Typical characteristics

Figure 13. Output current-R_{EXT} resistor

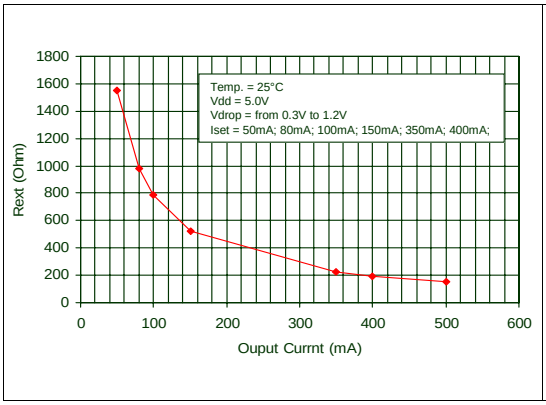


Figure 14. Output current vs dropout voltage

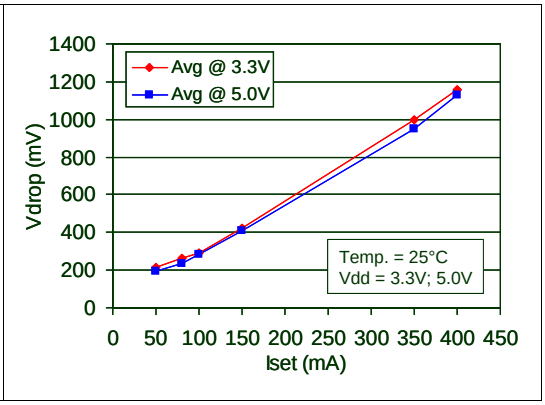


Figure 15. Output current vs $\pm \Delta I_{OL}$(%)

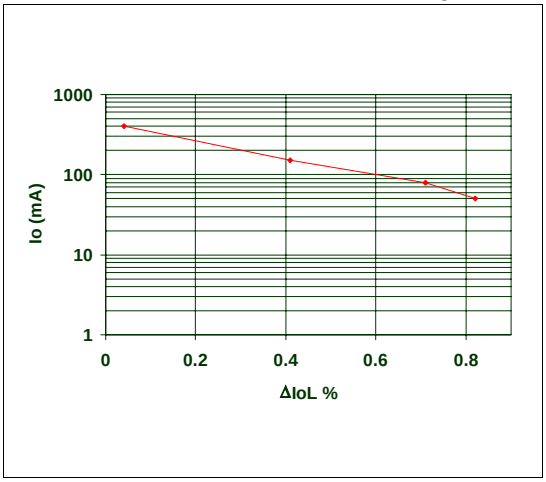
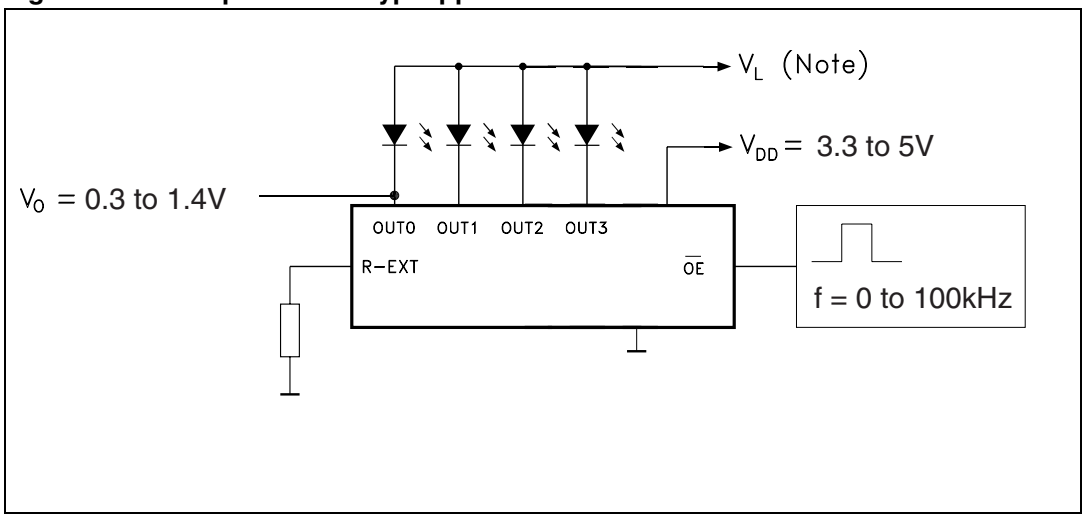
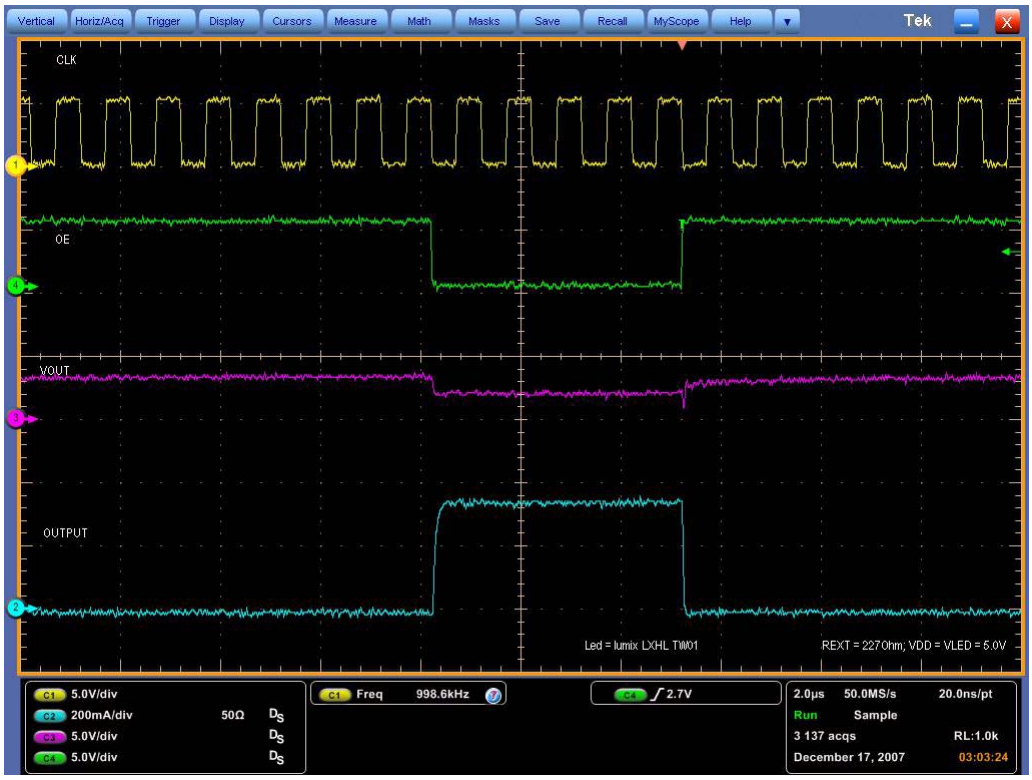


Figure 16. Four power-LED typ. application circuit



Note: V_L will be determined by the V_F of the LEDs

Figure 17. Typical output waveform



Note: Conditions: T_A = 25 C ,VDD = 5 V ,VL = 5 V, Rext = 227 Ω, LED = Lumix LXHL TW01

9 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

Table 9. DIP-14 mechanical data

Dim.	mm.			inch		
	Min	Typ	Max	Min	Typ	Max
a1	0.51			0.020		
B	1.39		1.65	0.055		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		15.24			0.600	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z	1.27		2.54	0.050		0.100

Figure 18. Package dimensions

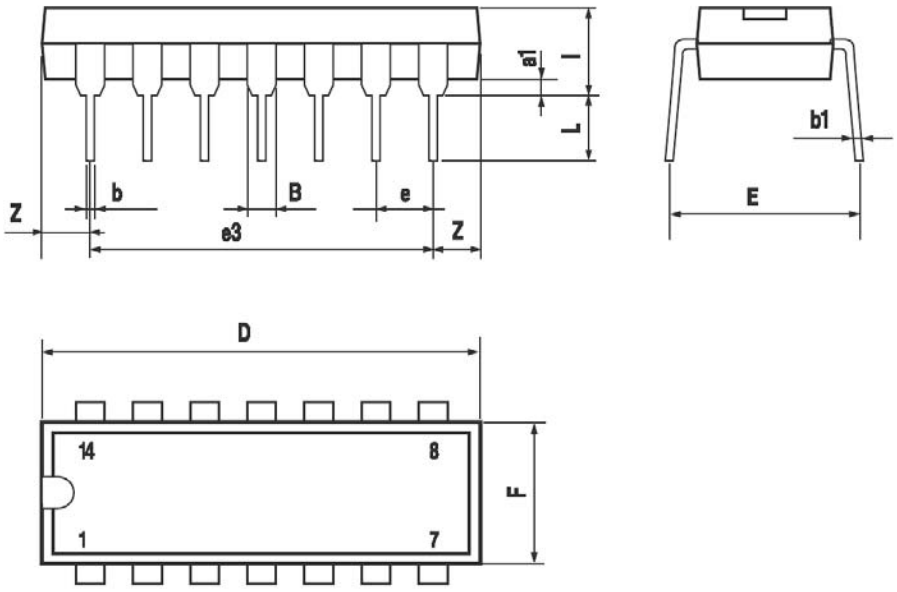


Table 10. SO-14 mechanical data

Dim.	mm.			inch		
	Min	Typ	Max	Min	Typ	Max
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	8.55		8.75	0.336		0.344
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		7.62			0.300	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.68			0.026
S	8° (max.)					

Figure 19. Package dimensions

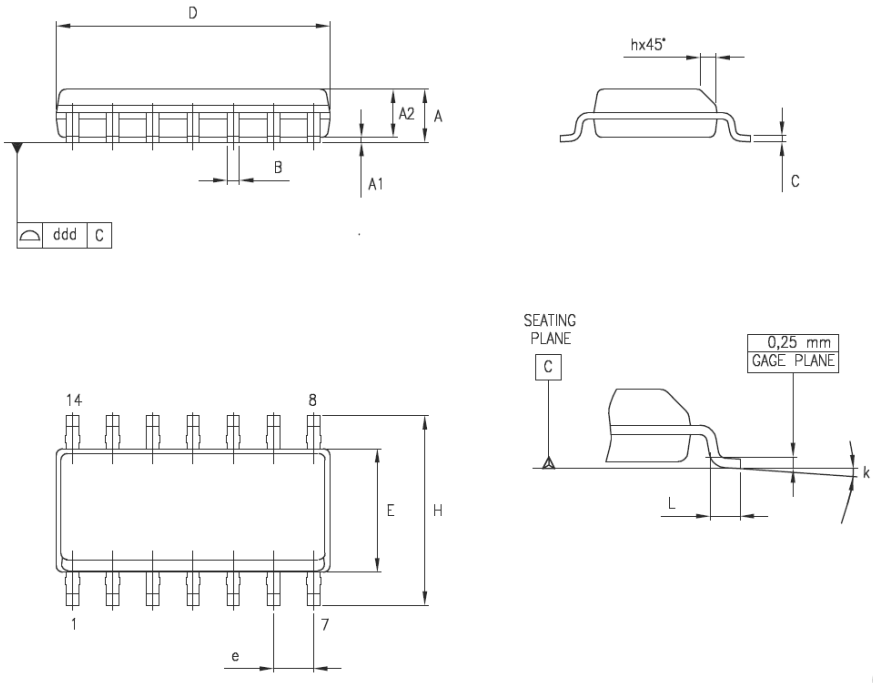


Figure 20. TSSOP16 exposed pad mechanical data

TSSOP16 EXPOSED PAD MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.2			0.047
A1			0.15		0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0089
D	4.9	5	5.1	0.193	0.197	0.201
D1	1.7			0.067		
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.5	0.169	0.173	0.177
E2	1.5			0.059		
e		0.65			0.0256	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030

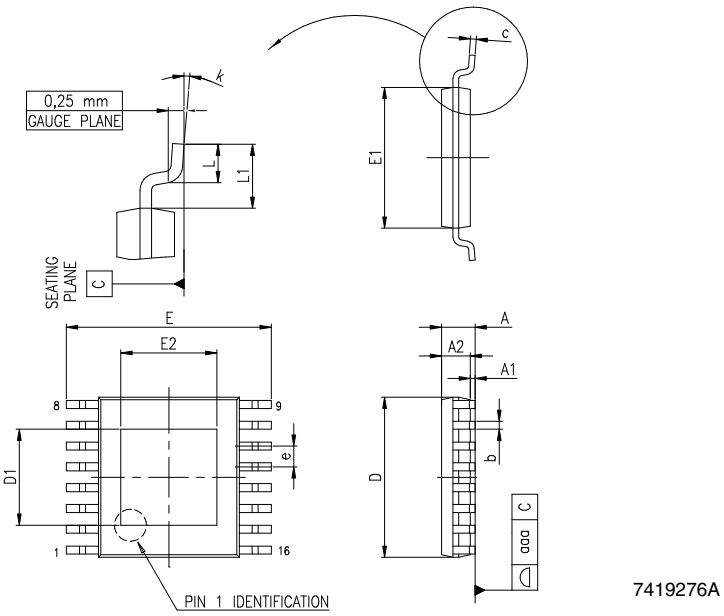


Table 11. Tape and reel SO-14

Dim.	mm.			inch		
	Min	Typ	Max	Min	Typ	Max
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			22.4			0.882
Ao	6.4		6.6	0.252		0.260
Bo	9		9.2	0.354		0.362
Ko	2.1		2.3	0.082		0.090
Po	3.9		4.1	0.153		0.161
P	7.9		8.1	0.311		0.319

Figure 21. Tape and reel dimensions

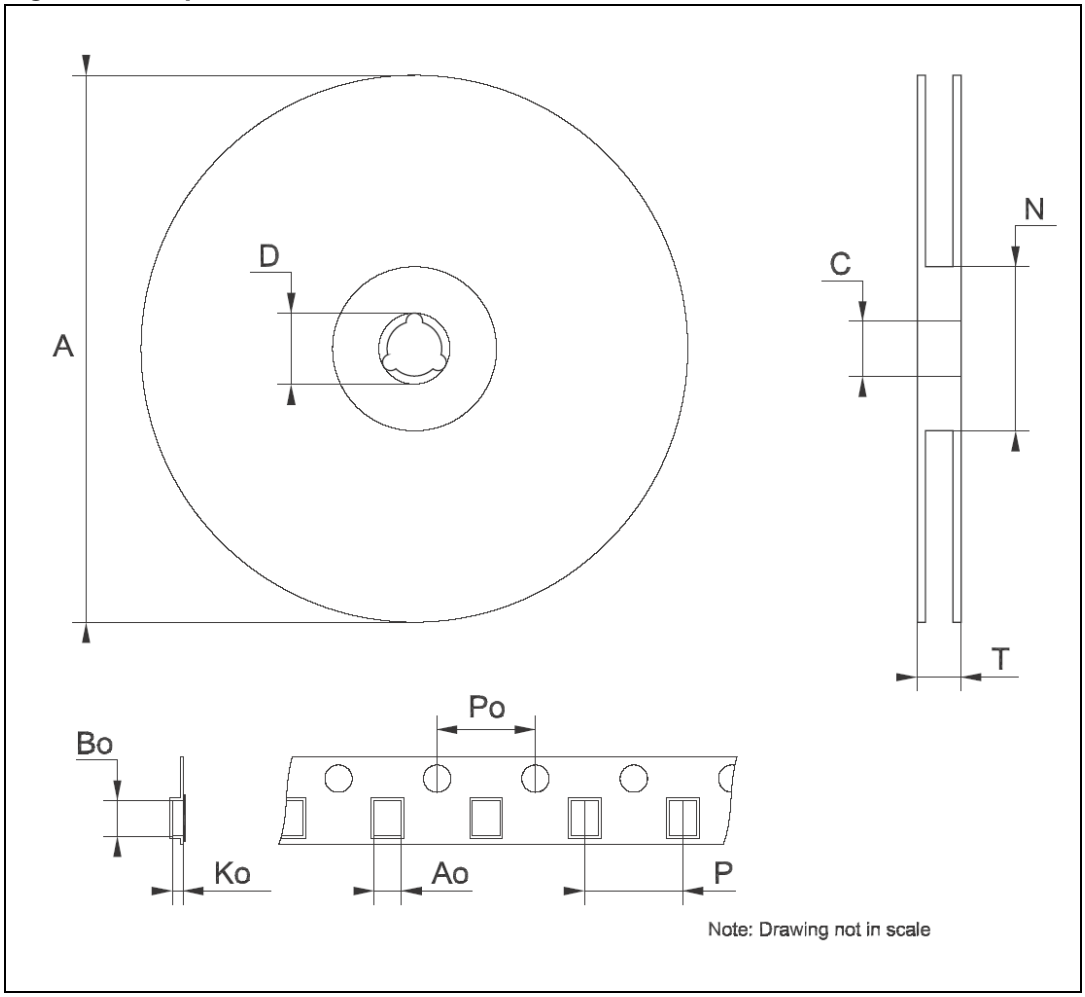
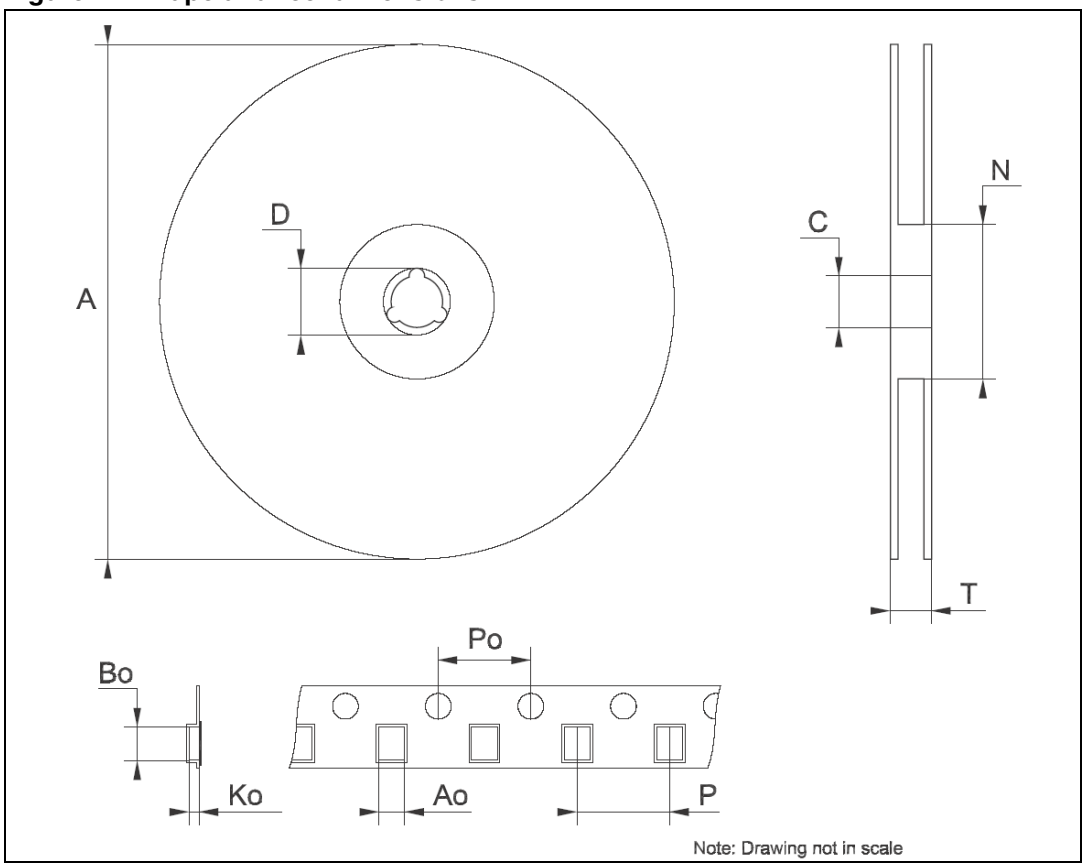


Table 12. TSSOP16 tape and reel

Dim.	mm.			inch		
	Min	Typ	Max	Min	Typ	Max
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			22.4			0.882
Ao	6.7		6.9	0.264		0.272
Bo	5.3		5.5	0.209		0.217
Ko	1.6		1.8	0.063		0.071
Po	3.9		4.1	0.153		0.161
P	7.9		8.1	0.311		0.319

Figure 22. Tape and reel dimensions



10 Revision history

Table 13. Document revision history

Date	Revision	Changes
26-Nov-2007	1	Initial release
16-Jan-2008	2	Added: *Figure 15 on page 15* and *Figure 17 on page 16*, Updated: *Table 8 on page 8*.
12-Mar-2008	3	Updated: *Figure 8 on page 12*.
23-Jun-2008	4	Updated: *Table 1 on page 1*, *Figure 20 on page 20*.

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