

# MC74VHCT373A

## Octal D-Type Latch with 3-State Output

The MC74VHCT373A is an advanced high speed CMOS octal latch with 3-state output fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

This 8-bit D-type latch is controlled by a latch enable input and an output enable input. When the output enable input is high, the eight outputs are in a high impedance state.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output.

The VHCT inputs are compatible with TTL levels. This device can be used as a level converter for interfacing 3.3 V to 5.0 V, because it has full 5.0 V CMOS level output swings.

The VHCT373A input and output (when disabled) structures provide protection when voltages between 0 V and 5.5 V are applied, regardless of the supply voltage. These input and output structures help prevent device destruction caused by supply voltage-input/output voltage mismatch, battery backup, hot insertion, etc.

### Features

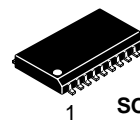
- High Speed:  $t_{PD} = 7.7$  ns (Typ) at  $V_{CC} = 5.0$  V
- Low Power Dissipation:  $I_{CC} = 4$   $\mu$ A (Max) at  $T_A = 25^\circ$ C
- TTL-Compatible Inputs:  $V_{IL} = 0.8$  V;  $V_{IH} = 2.0$  V
- Power Down Protection Provided on Inputs and Outputs
- Balanced Propagation Delays
- Designed for 4.5 V to 5.5 V Operating Range
- Low Noise:  $V_{OLP} = 1.6$  V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300 mA
- ESD Performance:
  - Human Body Model > 2000 V;
  - Machine Model > 200 V
- Chip Complexity: 196 FETs or 49 Equivalent Gates
- Pb-Free Packages are Available\*



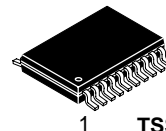
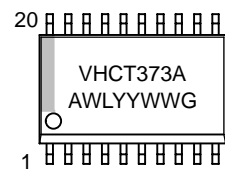
**ON Semiconductor®**

<http://onsemi.com>

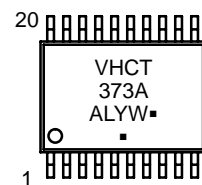
### MARKING DIAGRAMS



1  
**SOIC-20WB**  
**SUFFIX DW**  
**CASE 751D**



1  
**TSSOP-20**  
**SUFFIX DT**  
**CASE 948E**



A = Assembly Location  
 WL, L = Wafer Lot  
 YY, Y = Year  
 WW, W = Work Week  
 G or  $\blacksquare$  = Pb-Free Package  
 (Note: Microdot may be in either location)

### FUNCTION TABLE

INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	No Change
H	X	X	Z

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# MC74VHCT373A

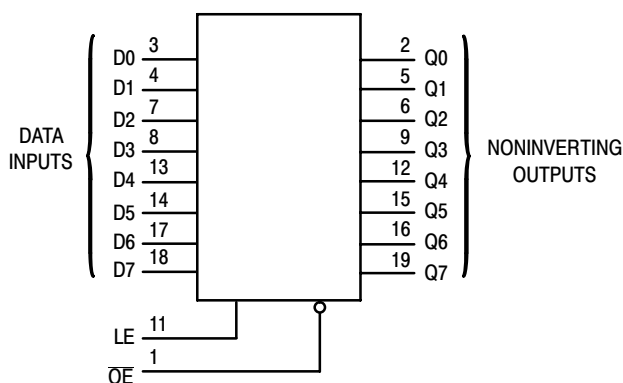


Figure 1. Logic Diagram

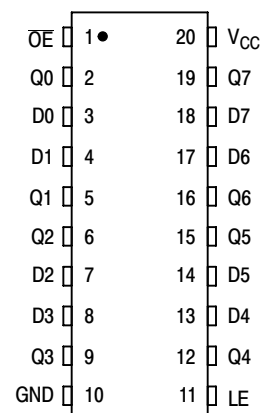


Figure 2. Pin Assignment

## MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_{CC}$	DC Supply Voltage	- 0.5 to + 7.0	V
$V_{in}$	DC Input Voltage	- 0.5 to + 7.0	V
$V_{out}$	DC Output Voltage Outputs in 3-State High or Low State	- 0.5 to + 7.0 - 0.5 to $V_{CC} + 0.5$	V
$I_{IK}$	Input Diode Current	- 20	mA
$I_{OK}$	Output Diode Current ( $V_{OUT} < GND$ ; $V_{OUT} > V_{CC}$ )	$\pm 20$	mA
$I_{out}$	DC Output Current, per Pin	$\pm 25$	mA
$I_{CC}$	DC Supply Current, $V_{CC}$ and GND Pins	$\pm 75$	mA
$P_D$	Power Dissipation in Still Air, SOIC Packages† TSSOP Package†	500 450	mW
$T_{stg}$	Storage Temperature	- 65 to + 150	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open.

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

†Derating - SOIC Packages: - 7 mW/°C from 65° to 125°C  
TSSOP Package: - 6.1 mW/°C from 65° to 125°C

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
$V_{CC}$	DC Supply Voltage	4.5	5.5	V
$V_{in}$	DC Input Voltage	0	5.5	V
$V_{out}$	DC Output Voltage Outputs in 3-State High or Low State	0 0	5.5 $V_{CC}$	V
$T_A$	Operating Temperature	- 40	+ 85	°C
$t_r, t_f$	Input Rise and Fall Time $V_{CC} = 5.0V \pm 0.5V$	0	20	ns/V

# MC74VHCT373A

## DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	T <sub>A</sub> = 25°C			T <sub>A</sub> = -40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
V <sub>IH</sub>	Minimum High-Level Input Voltage		4.5 to 5.5	2.0			2.0		V
V <sub>IL</sub>	Maximum Low-Level Input Voltage		4.5 to 5.5			0.8		0.8	V
V <sub>OH</sub>	Minimum High-Level Output Voltage V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -50μA	4.5	4.4	4.5		4.4		V
		I <sub>OH</sub> = -8mA	4.5	3.94			3.80		
V <sub>OL</sub>	Maximum Low-Level Output Voltage V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 50μA	4.5		0.0	0.1		0.1	V
		I <sub>OL</sub> = 8mA	4.5			0.36		0.44	
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = 5.5 V or GND	0 to 5.5			± 0.1		± 1.0	μA
I <sub>OZ</sub>	Maximum 3-State Leakage Current	V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub> V <sub>out</sub> = V <sub>CC</sub> or GND	5.5			± 0.25		± 2.5	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current	V <sub>in</sub> = V <sub>CC</sub> or GND	5.5			4.0		40.0	μA
I <sub>CC(T)</sub>	Quiescent Supply Current	Per Input: V <sub>IN</sub> = 3.4V Other Input: V <sub>CC</sub> or GND	5.5			1.35		1.50	mA
I <sub>OPD</sub>	Output Leakage Current	V <sub>OUT</sub> = 5.5V	0			0.5		5.0	μA

## AC ELECTRICAL CHARACTERISTICS (Input t<sub>r</sub> = t<sub>f</sub> = 3.0ns)

Symbol	Parameter	Test Conditions	T <sub>A</sub> = 25°C			T <sub>A</sub> = -40 to 85°C		Unit
			Min	Typ	Max	Min	Max	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, LE to Q	V <sub>CC</sub> = 5.0 ± 0.5V C <sub>L</sub> = 15pF C <sub>L</sub> = 50pF		7.7	12.3	1.0	13.5	ns
				8.5	13.3	1.0	14.5	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, D to Q	V <sub>CC</sub> = 5.0 ± 0.5V C <sub>L</sub> = 15pF C <sub>L</sub> = 50pF		5.1	8.5	1.0	9.5	ns
				5.9	9.5	1.0	10.5	
t <sub>PZL</sub> , t <sub>PZH</sub>	Output Enable Time, OE to Q	V <sub>CC</sub> = 5.0 ± 0.5V R <sub>L</sub> = 1kΩ C <sub>L</sub> = 50pF		6.3	10.9	1.0	12.5	ns
				7.1	11.9	1.0	13.5	
t <sub>PLZ</sub> , t <sub>PHZ</sub>	Output Disable Time, OE to Q	V <sub>CC</sub> = 5.0 ± 0.5V R <sub>L</sub> = 1kΩ		8.8	11.2	1.0	12.0	ns
t <sub>OSLH</sub> , t <sub>OSHL</sub>	Output to Output Skew	V <sub>CC</sub> = 5.5 ± 0.5V C <sub>L</sub> = 50pF (Note 1)			1.0		1.0	ns
C <sub>in</sub>	Maximum Input Capacitance			4	10		10	pF
C <sub>out</sub>	Maximum Three-State Output Capacitance (Output in High-Impedance State)			6				pF
C <sub>PD</sub>	Power Dissipation Capacitance (Note 2)	<b>Typical @ 25°C, V<sub>CC</sub> = 5.0V</b>						pF
		25						

- Parameter guaranteed by design. t<sub>OSLH</sub> = |t<sub>PLHm</sub> - t<sub>PLHn</sub>|, t<sub>OSHL</sub> = |t<sub>PHLm</sub> - t<sub>PHLn</sub>|.
- C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I<sub>CC(OPR)</sub> = C<sub>PD</sub> • V<sub>CC</sub> • f<sub>in</sub> + I<sub>CC</sub>/8 (per latch). C<sub>PD</sub> is used to determine the no-load dynamic power consumption; P<sub>D</sub> = C<sub>PD</sub> • V<sub>CC</sub><sup>2</sup> • f<sub>in</sub> + I<sub>CC</sub> • V<sub>CC</sub>.

# MC74VHCT373A

## NOISE CHARACTERISTICS (Input $t_r = t_f = 3.0\text{ns}$ , $C_L = 50\text{pF}$ , $V_{CC} = 5.0\text{V}$ )

Symbol	Parameter	$T_A = 25^\circ\text{C}$		Unit
		Typ	Max	
$V_{OLP}$	Quiet Output Maximum Dynamic $V_{OL}$	1.2	1.6	V
$V_{OLV}$	Quiet Output Minimum Dynamic $V_{OL}$	-1.2	-1.6	V
$V_{IHD}$	Minimum High Level Dynamic Input Voltage		2.0	V
$V_{ILD}$	Maximum Low Level Dynamic Input Voltage		0.8	V

## TIMING REQUIREMENTS (Input $t_r = t_f = 3.0\text{ns}$ )

Symbol	Parameter	Test Conditions	$T_A = 25^\circ\text{C}$		$T_A = -40\text{ to }85^\circ\text{C}$	Unit
			Typ	Limit	Limit	
$t_{w(h)}$	Minimum Pulse Width, LE	$V_{CC} = 5.0 \pm 0.5\text{V}$		6.5	8.5	ns
$t_{su}$	Minimum Setup Time, D to LE	$V_{CC} = 5.0 \pm 0.5\text{V}$		1.5	1.5	ns
$t_h$	Minimum Hold Time, D to LE	$V_{CC} = 5.0 \pm 0.5\text{V}$		3.5	3.5	ns

## ORDERING INFORMATION

Device	Package	Shipping†
MC74VHCT373ADWR2	SOIC-20WB	1000 / Tape & Reel
MC74VHCT373ADWRG	SOIC-20WB (Pb-Free)	1000 / Tape & Reel
MC74VHCT373ADTR2	TSSOP-20*	2500 / Tape & Reel
MC74VHCT373ADTRG	TSSOP-20*	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*This package is inherently Pb-Free.

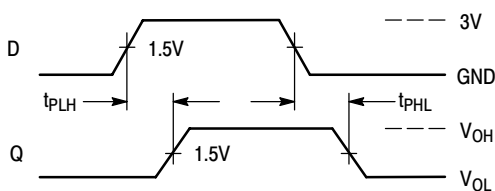


Figure 3. Switching Waveform

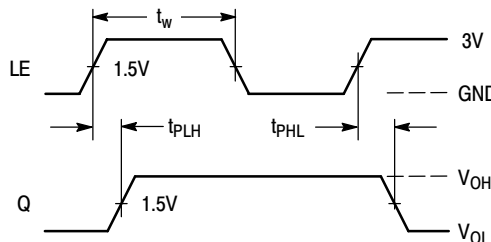


Figure 4. Switching Waveform

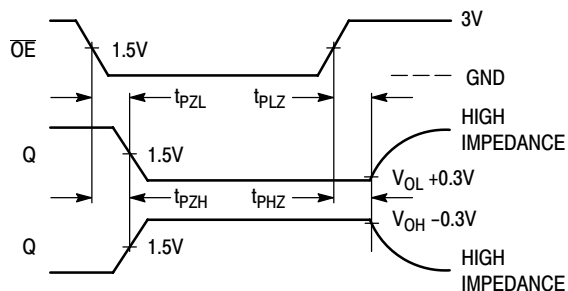


Figure 5. Switching Waveform

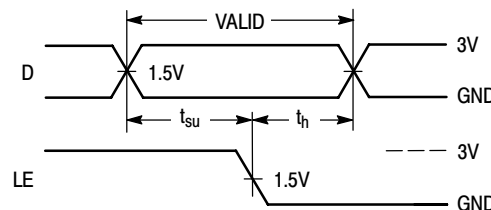
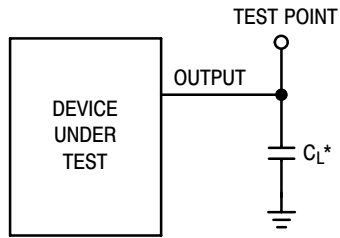


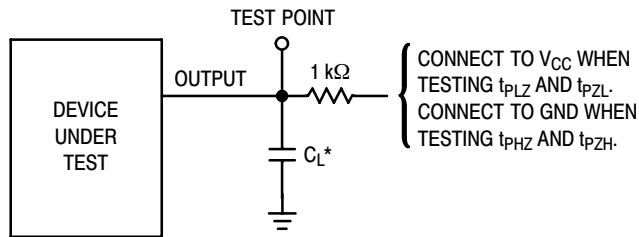
Figure 6. Switching Waveform

# MC74VHCT373A



\*Includes all probe and jig capacitance

Figure 7. Test Circuit



\*Includes all probe and jig capacitance

Figure 8. Test Circuit

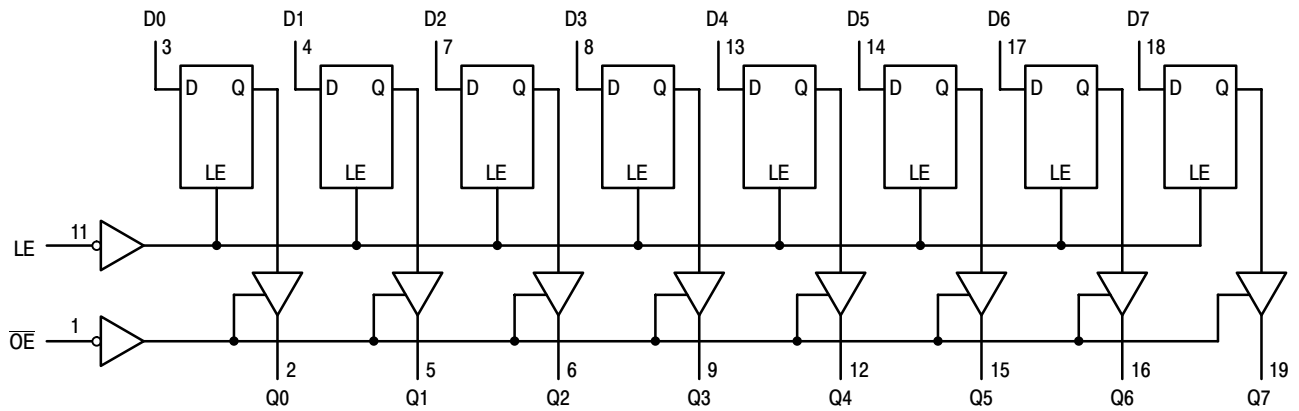
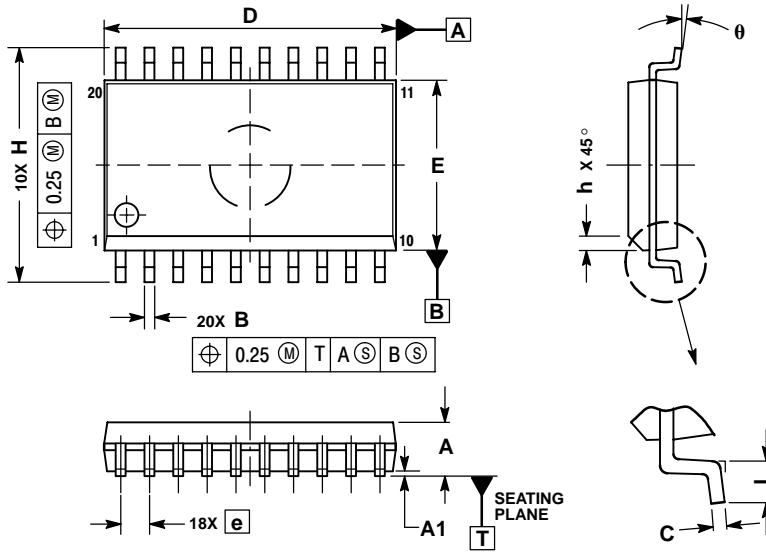


Figure 9. Expanded Logic Diagram

# MC74VHCT373A

## PACKAGE DIMENSIONS

SOIC-20 WB  
DW SUFFIX  
CASE 751D-05  
ISSUE G



### NOTES:

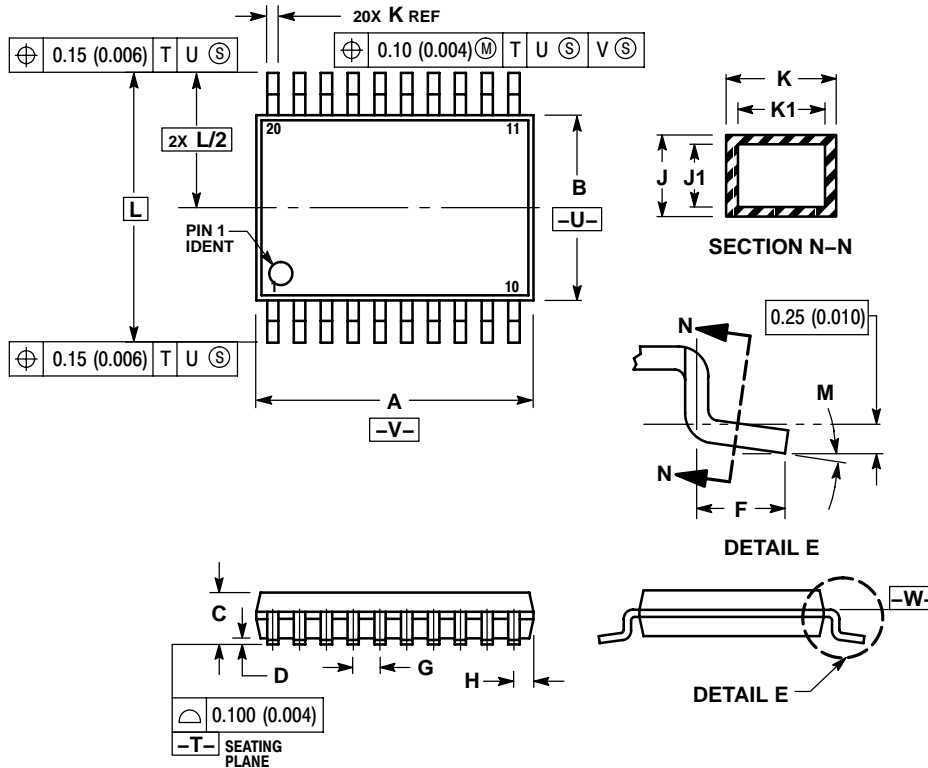
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

# MC74VHCT373A

## PACKAGE DIMENSIONS

TSSOP-20  
D5 SUFFIX  
CASE 948E-02  
ISSUE B



### NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: MILLIMETER.
- DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
- DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
- DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
- TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
- DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE  $-W-$ .

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

### PUBLICATION ORDERING INFORMATION

**LITERATURE FULFILLMENT:**  
Literature Distribution Center for ON Semiconductor  
P.O. Box 61312, Phoenix, Arizona 85082-1312 USA  
**Phone:** 480-829-7710 or 800-344-3860 Toll Free USA/Canada  
**Fax:** 480-829-7709 or 800-344-3867 Toll Free USA/Canada  
**Email:** orderlit@onsemi.com

**N. American Technical Support:** 800-282-9855 Toll Free  
USA/Canada

**Japan:** ON Semiconductor, Japan Customer Focus Center  
2-9-1 Kamimeguro, Meguro-ku, Tokyo, Japan 153-0051  
**Phone:** 81-3-5773-3850

**ON Semiconductor Website:** <http://onsemi.com>

**Order Literature:** <http://www.onsemi.com/litorder>

For additional information, please contact your local Sales Representative.

MC74VHCT373A/D