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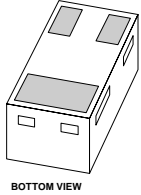
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Team Nexperia



BOTTOM VIEW

PMZ1000UN

N-channel TrenchMOS standard level FET

Rev. 2 — 17 September 2010

Product data sheet

1. Product profile

1.1 General description

Standard level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product is designed and qualified for use in computing, communications, consumer and industrial applications only.

1.2 Features and benefits

- Fast switching
- Low conduction losses due to low on-state resistance
- Saves PCB space due to small footprint (90 % smaller than SOT23)
- Suitable for use in compact designs due to low profile (55 % lower than SOT23)

1.3 Applications

- Driver circuits
- Switching in portable appliances

1.4 Quick reference data

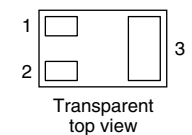
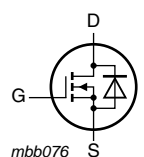
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 150\text{ °C}$	-	-	30	V
I_D	drain current	$T_{amb} = 25\text{ °C}; V_{GS} = 10\text{ V};$ see Figure 1	-	-	480	mA
P_{tot}	total power dissipation	$T_{amb} = 25\text{ °C};$ see Figure 2	-	-	350	mW
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 4.5\text{ V}; I_D = 0.2\text{ A};$ $T_j = 25\text{ °C};$ see Figure 8	-	-	1	Ω



2. Pinning information

Table 2. Pinning

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 <p>SOT883 (SC-101)</p>	 <p>mbb076</p>
2	S	source		
3	D	drain		

3. Ordering information

Table 3. Ordering information

Type number	Package		Version
	Name	Description	
PMZ1000UN	SC-101	leadless ultra small plastic package; 3 solder lands; body 1.0 × 0.6 × 0.5 mm	SOT883

4. Marking

Table 4. Marking codes

Type number	Marking code
PMZ1000UN	6N

5. Limiting values

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

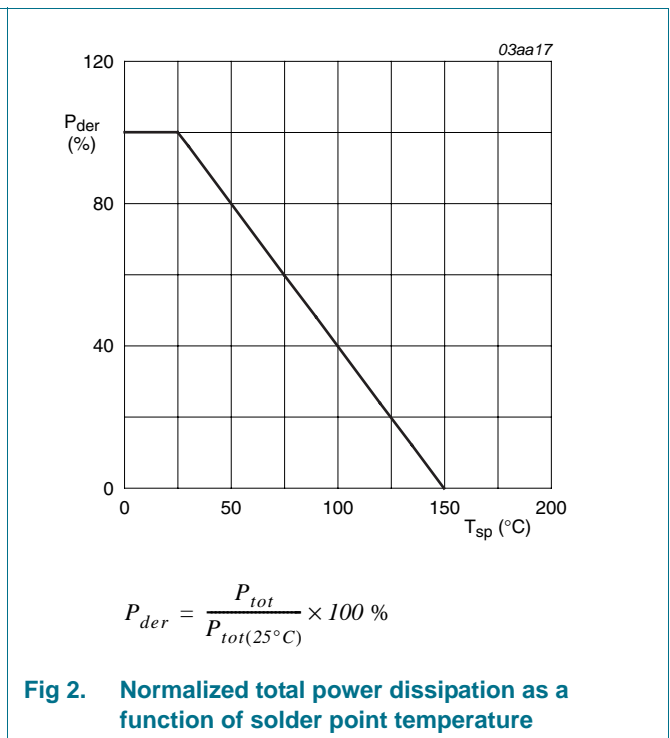
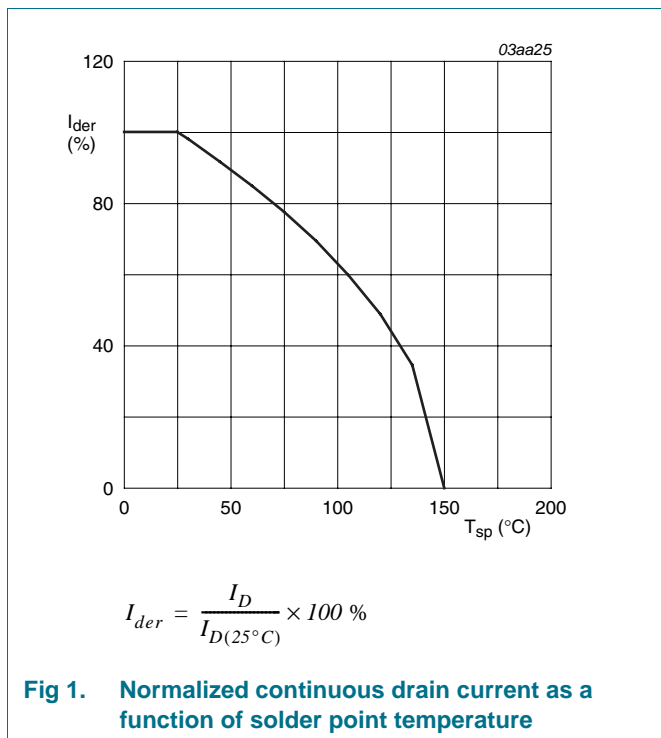
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 150\text{ °C}$	-	30	V
V_{DGR}	drain-gate voltage	$25\text{ °C} \leq T_j \leq 150\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$	-	30	V
V_{GS}	gate-source voltage		-8	+8	V
I_D	drain current	$T_{amb} = 25\text{ °C}$; $V_{GS} = 10\text{ V}$; see Figure 1	-	480	mA
I_{DM}	peak drain current	$T_{amb} = 25\text{ °C}$; $t_p \leq 10\text{ }\mu\text{s}$; pulsed	-	1.8	A
P_{tot}	total power dissipation	$T_{amb} = 25\text{ °C}$; see Figure 2	-	350	mW
T_{stg}	storage temperature		-55	+150	°C
T_j	junction temperature		-55	+150	°C

Table 5. Limiting values ...continued
 In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
Source-drain diode					
I_S	source current	$T_{amb} = 25\text{ }^\circ\text{C}$	-	480	mA
Electrostatic discharge					
V_{ESD}	electrostatic discharge voltage	HBM; C = 100 pF; R = 1.5 k Ω	-	60	V
		MM; C = 200 pF	-	30	V



6. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	see Figure 3	-	-	50	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient		[1]	-	355	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

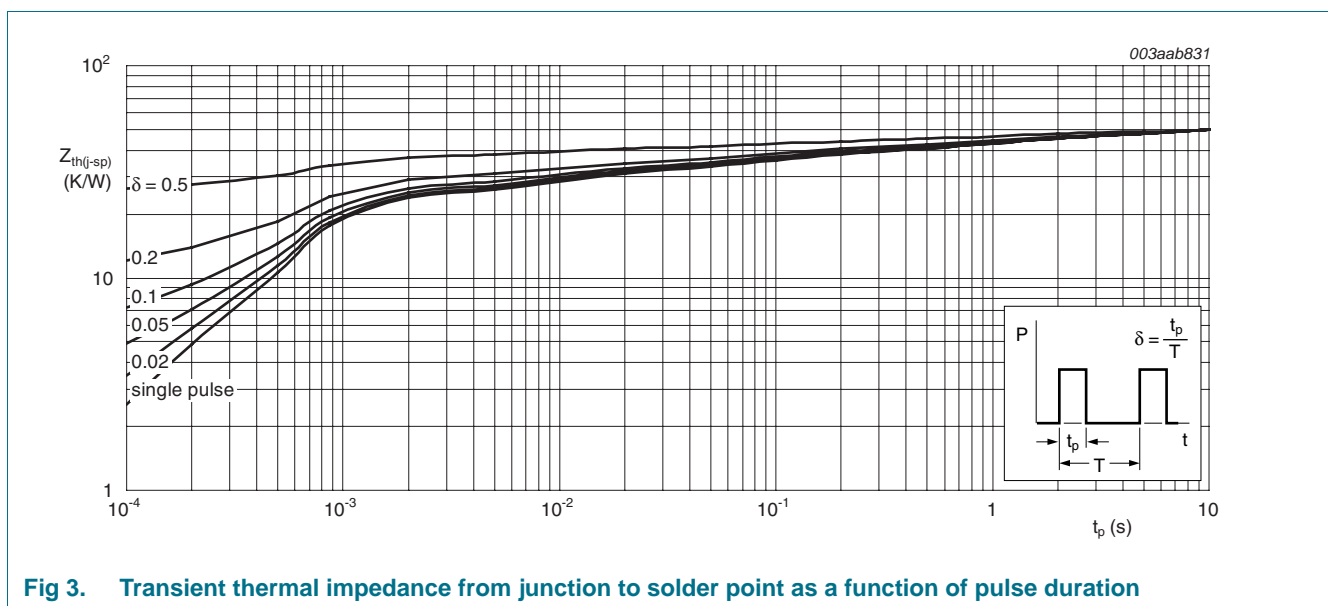


Fig 3. Transient thermal impedance from junction to solder point as a function of pulse duration

7. Characteristics

Table 7. Characteristics
T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 10 μA; V _{GS} = 0 V				
		T _j = 25 °C	30	-	-	V
		T _j = -55 °C	27	-	-	V
V _{GS(th)}	gate-source threshold voltage	I _D = 0.25 mA; V _{DS} = V _{GS} ; see Figure 6 and 7				
		T _j = 25 °C	0.45	0.7	0.95	V
		T _j = 150 °C	0.25	-	-	V
		T _j = -55 °C	-	-	1.15	V
I _{DSS}	drain leakage current	V _{DS} = 30 V; V _{GS} = 0 V				
		T _j = 25 °C	-	-	1	μA
		T _j = 150 °C	-	-	100	μA
I _{GSS}	gate leakage current	V _{GS} = ±8 V; V _{DS} = 0 V	-	10	100	nA
R _{DS(on)}	drain-source on-state resistance	V _{GS} = 4.5 V; I _D = 0.2 A; see Figure 8				
		T _j = 25 °C	-	-	1	Ω
		T _j = 150 °C	-	-	1.5	Ω
		V _{GS} = 2.5 V; I _D = 0.1 A; Figure 8	-	-	1.1	Ω
		V _{GS} = 1.8 V; I _D = 0.075 A; Figure 8	-	-	1.4	Ω
Dynamic characteristics						
Q _{G(tot)}	total gate charge	I _D = 1 A; V _{DS} = 15 V; V _{GS} = 4.5 V; see Figure 9 and 10	-	0.89	-	nC
Q _{GS}	gate-source charge		-	0.1	-	nC
Q _{GD}	gate-drain charge		-	0.2	-	nC
C _{iss}	input capacitance	V _{DS} = 25 V; V _{GS} = 0 V; f = 1 MHz; see Figure 11	-	43	-	pF
C _{oss}	output capacitance		-	7.7	-	pF
C _{rss}	reverse transfer capacitance		-	4.8	-	pF
t _{d(on)}	turn-on delay time	V _{DS} = 15 V; R _L = 15 Ω; V _{GS} = 10 V; R _{G(ext)} = 6 Ω	-	4	-	ns
t _r	rise time		-	7.5	-	ns
t _{d(off)}	turn-off delay time		-	18	-	ns
t _f	fall time		-	4.5	-	ns
Source-drain diode						
V _{SD}	source-drain voltage	I _S = 0.3 A; V _{GS} = 0 V; see Figure 11	-	0.76	1.2	V

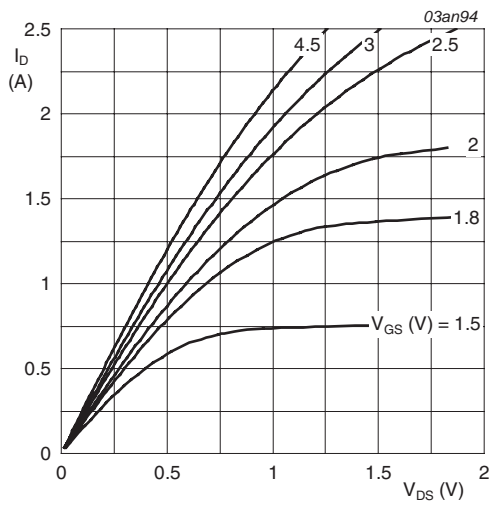


Fig 4. Output characteristics: drain current as a function of drain-source voltage; typical values

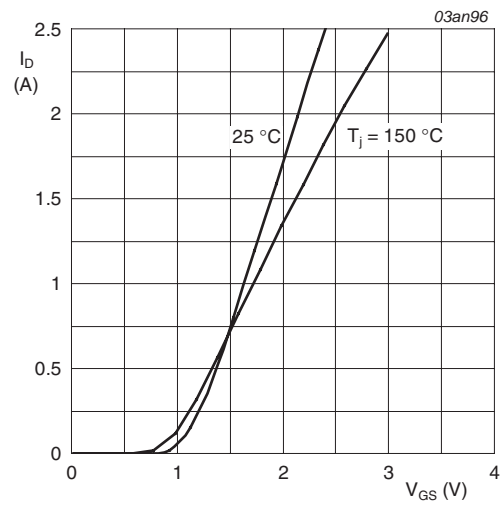


Fig 5. Transfer characteristics: drain current as a function of gate-source voltage; typical values

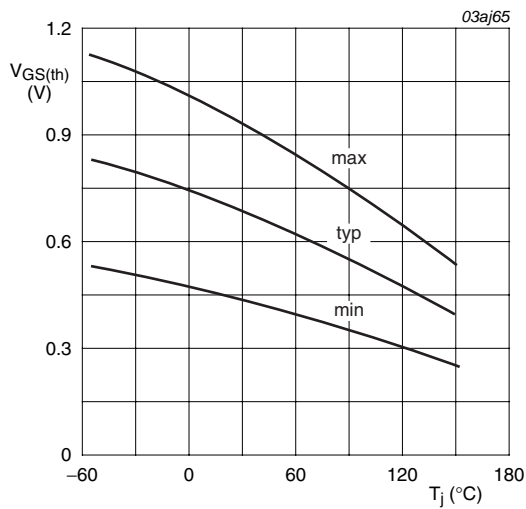


Fig 6. Gate-source threshold voltage as a function of junction temperature

$I_D = 1\text{ mA}$; $V_{DS} = V_{GS}$

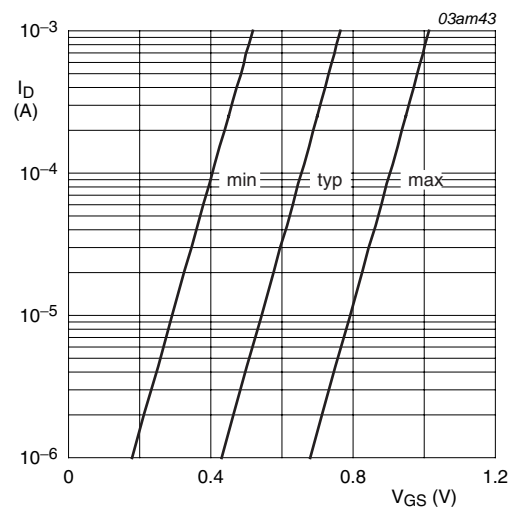
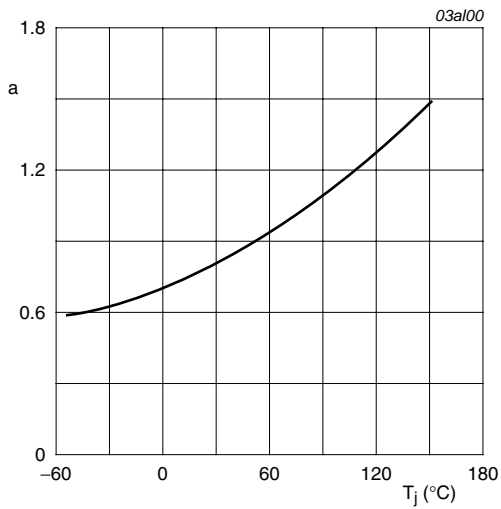


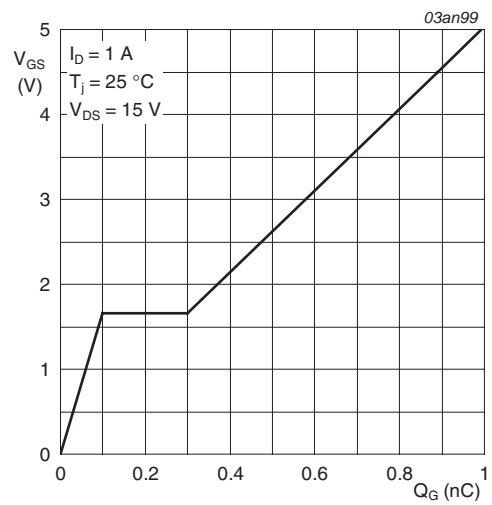
Fig 7. Sub-threshold drain current as a function of gate-source voltage

$T_j = 25\text{ °C}$; $V_{DS} = 5\text{ V}$



$$a = \frac{R_{DSon}}{R_{DSon(25^{\circ}C)}}$$

Fig 8. Normalized drain-source on-state resistance as a function of junction temperature



$I_D = 1 \text{ A}; V_{DS} = 15 \text{ V}$

Fig 9. Gate-source voltage as a function of gate charge; typical values

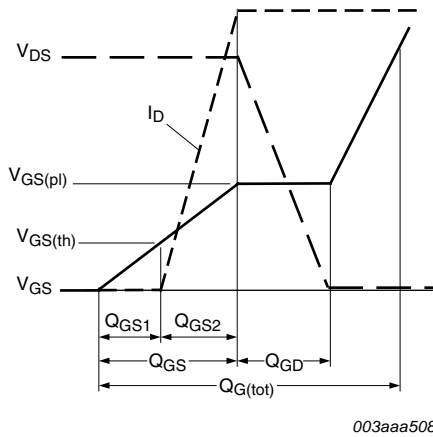
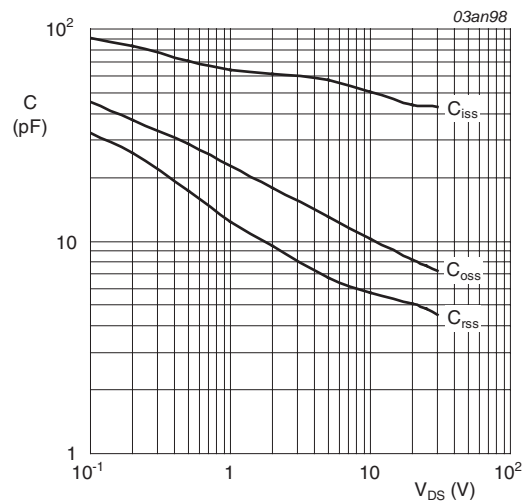
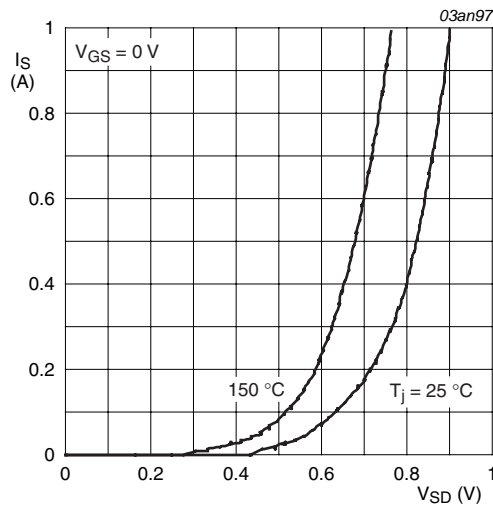


Fig 10. Gate charge waveform definitions



$V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$

Fig 11. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$T_j = 25\text{ }^\circ\text{C}$ and $150\text{ }^\circ\text{C}$; $V_{GS} = 0\text{ V}$

Fig 12. Source current as a function of source-drain voltage; typical values

8. Package outline

Leadless ultra small plastic package; 3 solder lands; body 1.0 x 0.6 x 0.5 mm

SOT883

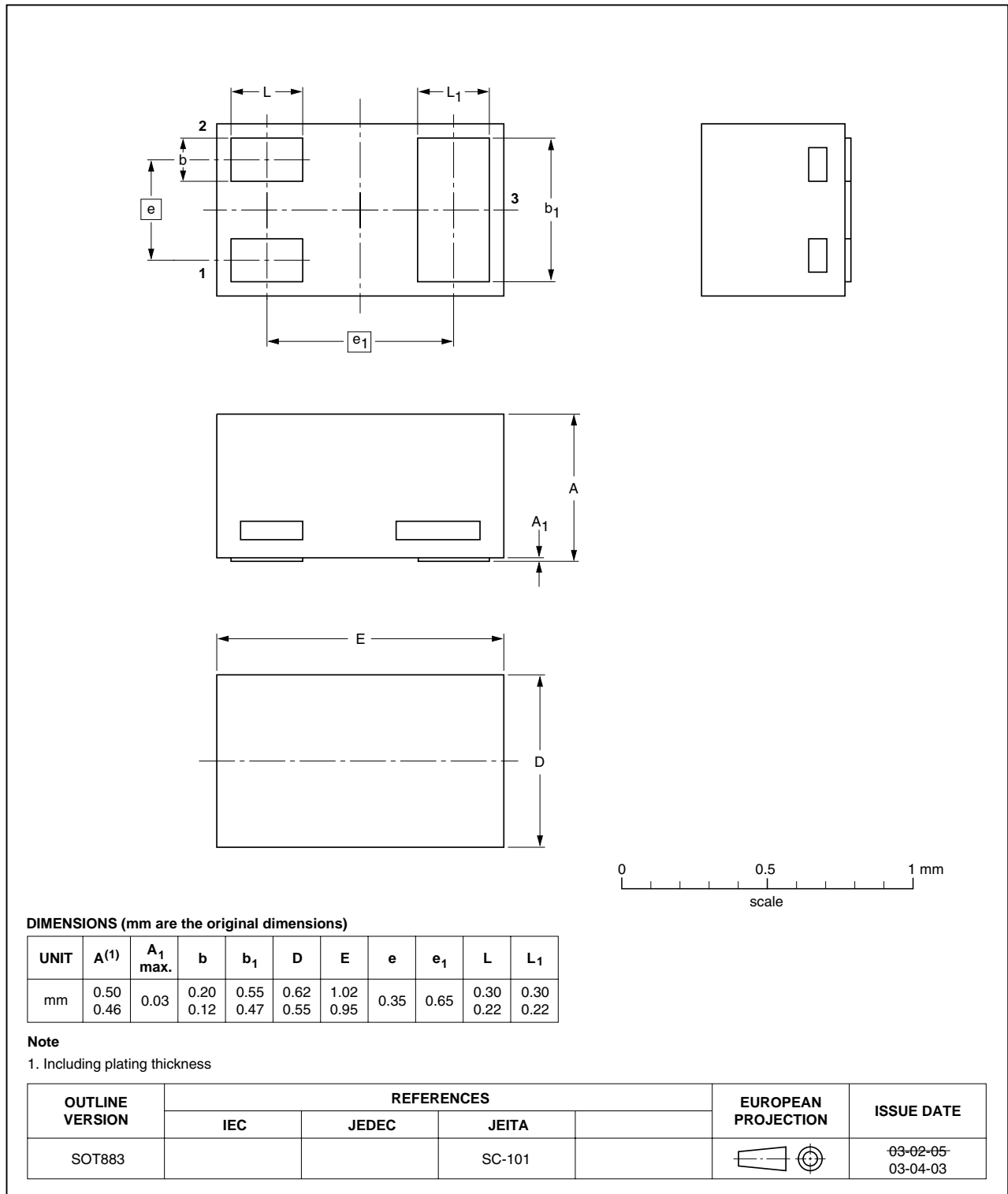


Fig 13. Package outline SO883 (SC-101)

9. Soldering

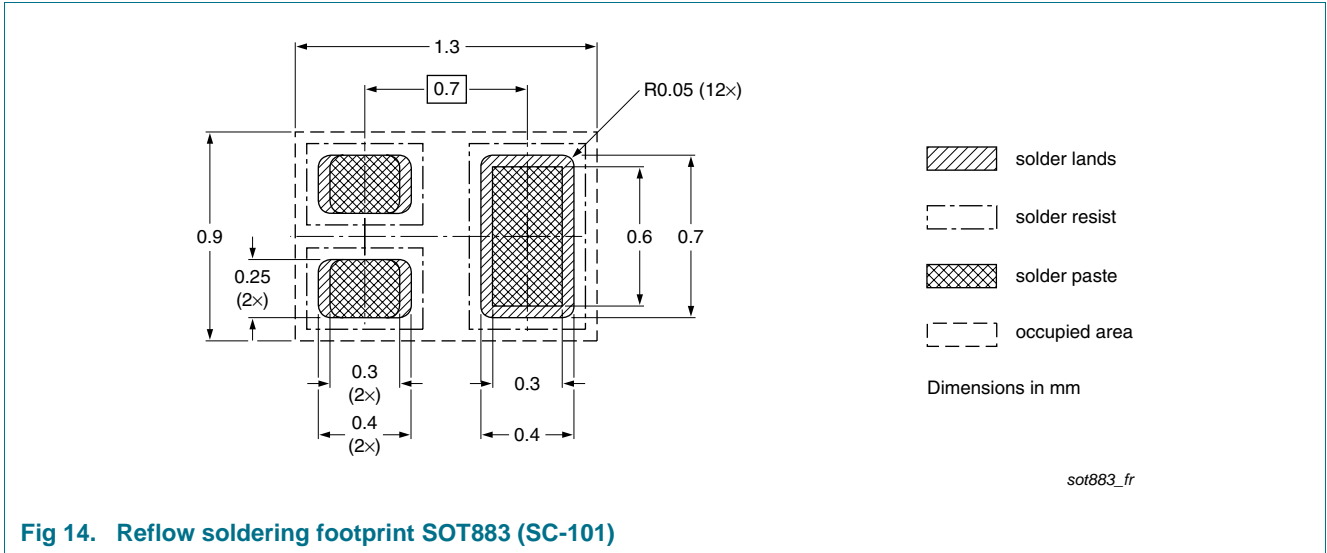


Fig 14. Reflow soldering footprint SOT883 (SC-101)

10. Revision history

Table 8. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PMZ1000UN v.2	20100917	Product data sheet	-	PMZ1000UN_1
Modifications:	<ul style="list-style-type: none">• Modifications of thermal parameters• Section 11 "Legal information": updated			
PMZ1000UN_1	20100224	Product data sheet	-	-

11. Legal information

11.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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