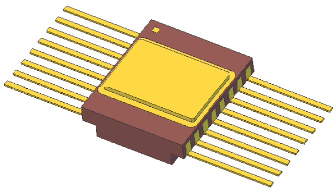
RHFLVDS315

Rad-hard quad LVDS driver

Datasheet - production data



Ceramic Flat-16

The upper metallic lid is electrically connected to ground

Features

- LVDS output
- CMOS input
- Enable/Disable function with high-impedance
- ANSI TIA/EIA-644 compliant
- 400 Mbps (200 MHz)
- Cold spare on all pins
- 3.3 V operating power supply
- 4.8 V absolute rating
- Output voltage: 350 mV on 100 Ω load
- Hermetic package
- Guaranteed up to 300 krad TID
- SEL immune up to 135 MeV.cm²/mg
- SET/SEU immune up to 67 MeV.cm²/mg

Description

The RHFLVDS315 is a quad, low-voltage, differential signaling (LVDS) driver specifically designed, packaged, and qualified for use in aerospace environments in a low-power and fast point-to-point baseband data transmission standard.

Operating at 3.3 V power supply, the RHFLVDS315 operates over a controlled impedance of 100-ohm transmission media that may be printed circuit board traces, back planes or cables.

The circuit features an internal fail-safe function to ensure a known state in case of floating input. All pins have cold spare buffers to ensure they are in high impedance when V_{CC} is tied to GND.

Designed using ST's proprietary CMOS process with specific mitigation techniques, the RHFLVDS315 achieves “best in the class” for hardness to total ionisation dose and heavy ions.

The RHFLVDS315 can operate over a large temperature range of -55 °C to +125 °C and is housed in a hermetic Ceramic Flat-16 package.

Table 1. Device summary

Reference	SMD pin	Quality level	Package	Lead finish	Mass	EPPL(1)	Temp. range
RHFLVDS315K1	-	Engineering model	Ceramic Flat-16	Gold	0.65 g	-	-55 °C to 125 °C
RHFLVDS315K01V	5962F98651	QML-V flight				Target	

1. EPPL = ESA preferred part list

Contents

1 Functional description

Figure 1. Logic diagram and logic symbol

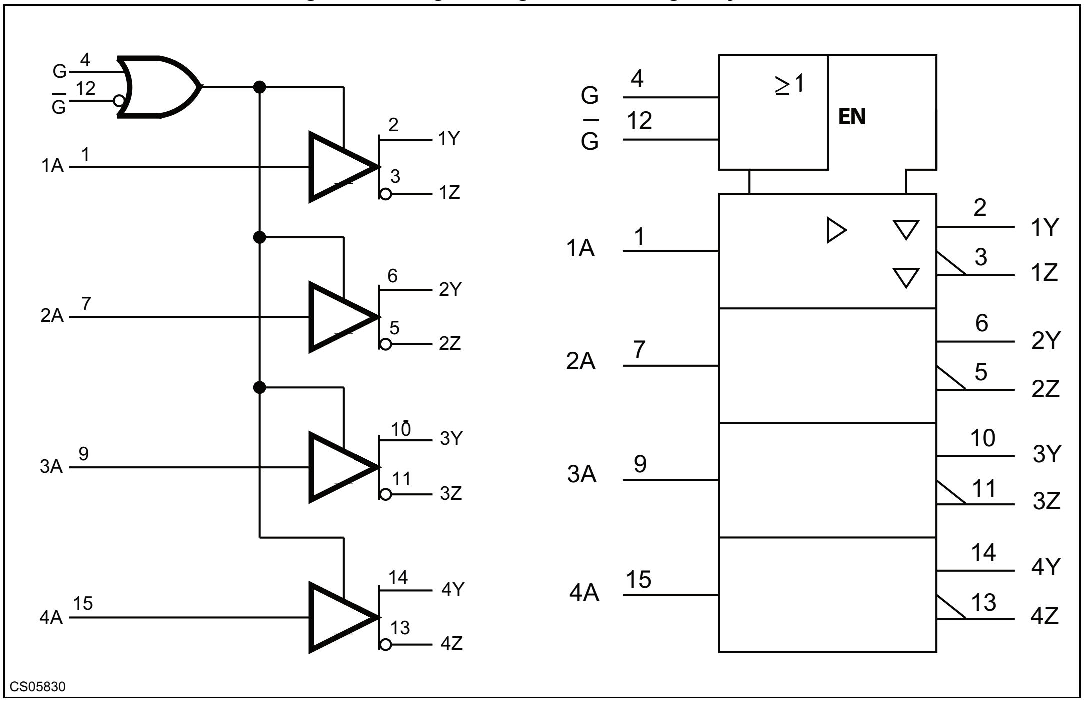


Table 2. Truth table

Input	Enables		Outputs	
A	**G**	**$\overline{G}$**	**Y**	**Z**
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z
OPEN	H	X	L	H
OPEN	X	L	L	H

Note: 1 *The G input features an internal pull-up network. The $\overline{G}$ input features an internal pull-down network. If they are floating the circuit is enabled.*

2 *L = low level, H = high Level, X = irrelevant, Z = high impedance (off)*

2 Pin configuration

Figure 2. Pin connections (top view)

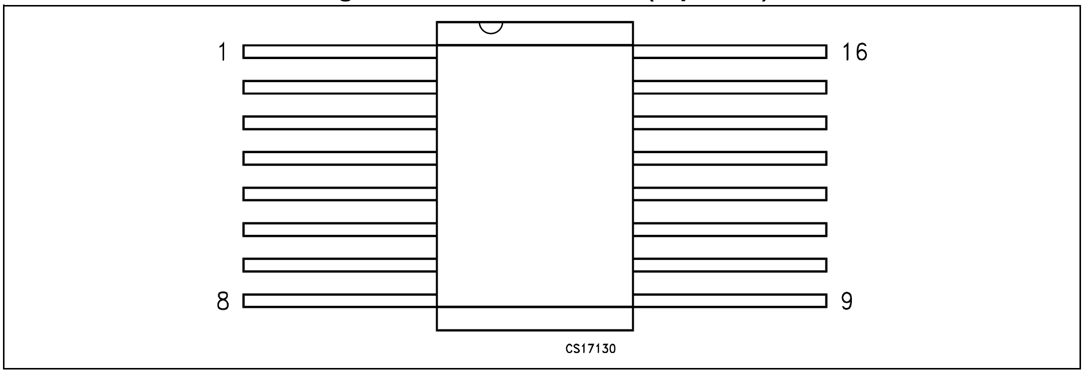


Table 3. Pin description

Pin number	Symbol	Name and function
1, 7, 9, 15	1A to 4A	Driver inputs
2, 6, 10, 14	1Y to 4Y	Driver outputs
3, 5, 11, 13	1Z to 4Z	
4	G	Enable
12	$\overline{G}$	
8	GND	Ground
16	V_{CC}	Supply voltage

3 Maximum ratings and operating conditions

Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage(1)	4.8	V
V_i	TTL inputs (operating or cold spare)	-0.3 to 4.8	
V_{OUT}	LVDS outputs (operating or cold spare)	-0.3 V to +4.8 V	
T_{stg}	Storage temperature range	-65 to +150	°C
T_j	Maximum junction temperature	+150	
R_{thjc}	Thermal resistance junction to case(2)	22	°C/W
ESD	HBM: Human body model – All pins except LVDS outputs – LVDS outputs vs. GND	 2 8	kV
	CDM: Charge device model	500	V

1. All voltages, except differential I/O bus voltage, are with respect to the network ground terminal.
2. Short-circuits can cause excessive heating. Destructive dissipation can result from short-circuits on the amplifiers.

Table 5. Operating conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply voltage	3	3.3	3.6	V
V_{IN}	Driver DC input voltage (TTL inputs)	0		3.6	
T_A	Ambient temperature range	-55		+125	°C

4 Radiation

Total dose (MIL-STD-883 TM 1019)

The products guaranteed in radiation within the RHA QML-V system fully comply with the MIL-STD-883 TM 1019 specification.

The RHFLVDS315 is RHA QML-V, tested and characterized in full compliance with the MIL-STD-883 specification, between 50 and 300 rad/s only (full CMOS technology).

All parameters provided in *Table 7: Electrical characteristics* apply to both pre- and post-irradiation, as follows:

- All test are performed in accordance with MIL-PRF-38535 and test method 1019 of MIL-STD-883 for total ionizing dose (TID).
- The initial characterization is performed in qualification only on both biased and unbiased parts.
- Each wafer lot is tested at high dose rate only, in the worst bias case condition, based on the results obtained during the initial qualification.

Heavy ions

The behavior of the product when submitted to heavy ions is not tested in production. Heavy-ion trials are performed on qualification lots only.

Table 6. Radiation

Type	Characteristics	Value	Unit
TID	High-dose rate (50 - 300 rad/sec) up to:	300	krad
Heavy ions	SEL immune up to: (with a particle angle of 60 ° at 125 °C)	135	MeV.cm²/mg
	SEL immune up to: (with a particle angle of 0 ° at 125 °C)	67	
	SET/SEU immune up to: (at 25 °C)	67	

5 Electrical characteristics

In *Table 7* below, V_{CC} = 3 V to 3.6 V, capa-load (CL) = 10 pF, typical values are at T_{amb} = +25 °C, min. and max values are at T_{amb} = - 55 °C and + 125 °C unless otherwise specified

Table 7. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{CCL}	Total enabled supply current, drivers enabled, not switching	V_{IN} = 0 V or V_{CC} Load = 100 Ω on all channels		16.5	35	mA
I_{CCZ}	Total disabled supply current, loaded or not loaded, drivers disabled	V_{IN} = 0 V or V_{CC} G = GND, $\overline{G}$ = V_{CC}		2.8	4	mA
I_{OFF} (1)	TTL input power-off leakage current	V_{CC} = 0 V, V_{IN} = 3.6 V	-10		10	µA
	LVDS output power-off leakage current	V_{CC} = 0 V, V_{OUT} = 3.6 V	-50		+50	µA
V_{OH}	Output voltage high	R_L = 100 Ω			1.65	V
V_{OL}	Output voltage low	R_L = 100 Ω	0.925			V
V_{OD1}	Differential output voltage	R_L = 100 Ω	250		400	mV
DV_{OD1}	Change of magnitude of V_{OD1} for complementary output states	R_L = 100 Ω			10	mV
V_{OS}	Offset voltage	R_L = 100 Ω	1.125		1.45	V
DV_{OS}	Change of magnitude of V_{OS} for complementary output states	R_L = 100 Ω			15	mV
I_{OS}	Output short-circuit current	V_{IN} = 0 V and $V_{O(Z)}$ = 0 V or V_{IN} = V_{CC} and $V_{O(Y)}$ = 0 V	-9			mA
I_O	High impedance output current	Disabled, V_{OUT} = 3.6 V or GND	-10		10	µA
V_{IH}	Input voltage high	G, $\overline{G}$, and TTL inputs	2		V_{CC}	V
V_{IL}	Input voltage low	G, $\overline{G}$, and TTL inputs	GND		0.8	V
I_{IH}	High level input current	G, $\overline{G}$, and TTL inputs V_{CC} = 3.6 V, V_{IN} = V_{CC}	-10		10	µA
I_{IL}	Low level input current	G, $\overline{G}$ and TTL inputs V_{CC} = 3.6 V, V_{IN} = 0	-10		10	µA
C_{IN}	Input capacitance			3		pF
t_{PHLD}	Propagation delay time, high to low output	Refer to *Figure 4*	0.3		3.5	ns
t_{PLHD}	Propagation delay time, low to high output	Refer to *Figure 4*	0.3		3.5	ns

Table 7. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_{SK1}	Channel-to-channel skew(2)	Load: refer to *Figure 4*			0.6	ns
t_{SK2}	Chip-to-chip skew(3)(4)				3	
t_{SKD}	Differential skew(5) (t_{PHLD}-t_{PLHD})				0.6	
t_{PHZ}	Propagation delay time, high level to high impedance output				12	
t_{PLZ}	Propagation delay time, low level to high impedance output				12	
t_{PZH}	Propagation delay time, high impedance to high level output				12	
t_{PZL}	Propagation delay time, high impedance to low level output				12	

1. All pins except pin under test and V_{CC} are floating.
2. t_{SK1} is the maximum delay time difference between all outputs of the same device (measured with all inputs connected together).
3. t_{SK2} is the maximum delay time difference between outputs of all devices when they operate with the same supply voltage, at the same temperature.
4. Guaranteed by design.
5. t_{SKD} is the maximum delay time difference between t_{PHLD} and t_{PLHD} (see *Figure 4*).

Cold sparing

The RHFLVDS315 features a cold spare input and output buffer. In high reliability applications, cold sparing enables a redundant device to be tied to the data bus with its power supply at 0 V (V_{CC} = GND) without affecting the bus signals or injecting current from the I/Os to the power supplies. Cold sparing also allows redundant devices to be kept powered off so that they can be switched on only when required. This has no impact on the application. Cold sparing is achieved by implementing a high impedance between the I/Os and V_{CC}. ESD protection is ensured through a non-conventional dedicated structure.

Fail-safe

In many applications, inputs need a fail-safe function to avoid an uncertain output state when the inputs are not connected properly. In case of TTL floating inputs, the LVDS outputs remain in a stable logic-high state.

6 Test circuit

Figure 3. Voltage and current definition

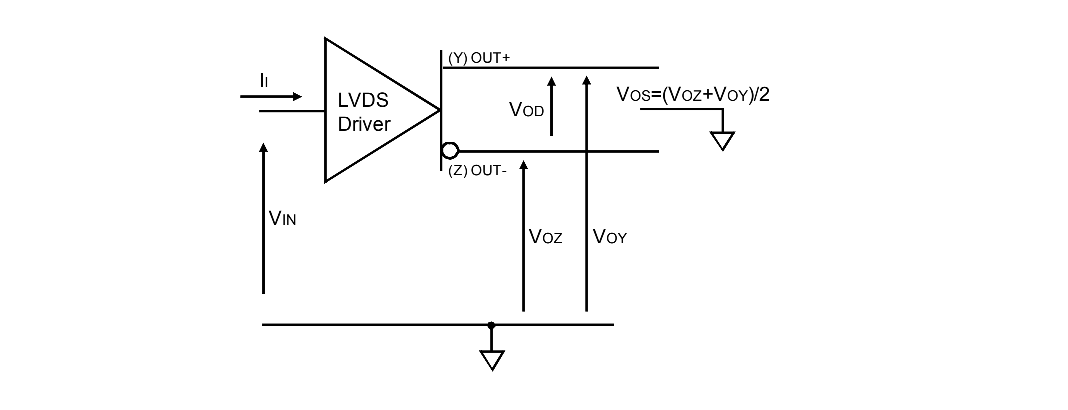
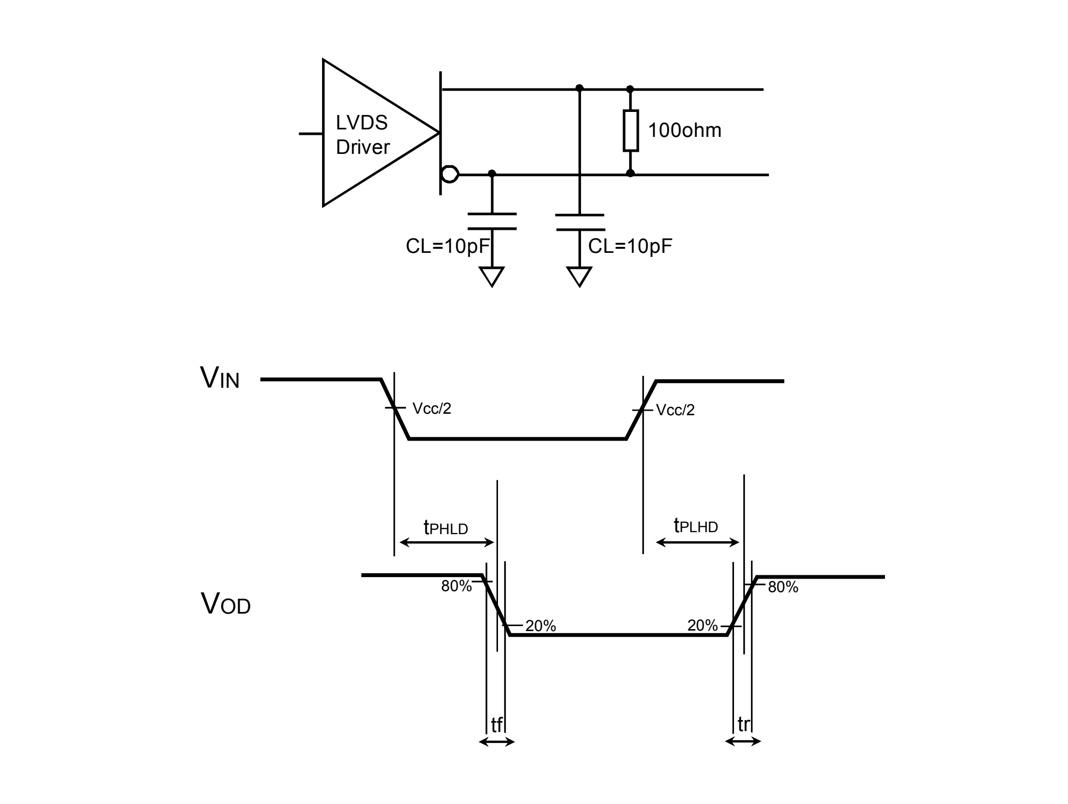
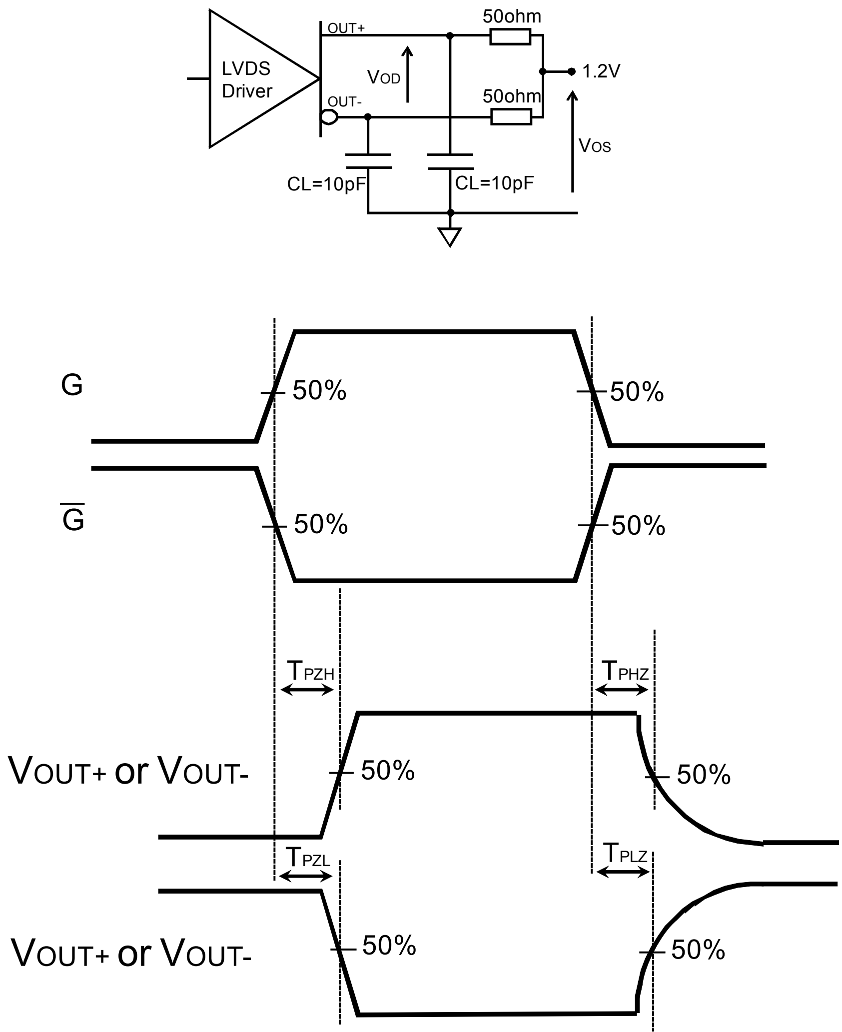


Figure 4. Test circuit, timing and voltage definitions for differential output signal



1. All input pulses are supplied by a generator with the following characteristics: t_r or $t_f \leq 1$ ns, f = 1 MHz, Z_O = 50 Ω, and duty cycle = 50%.
2. The product is guaranteed in test with CL = 10 pF

Figure 5. Enable and disable waveform



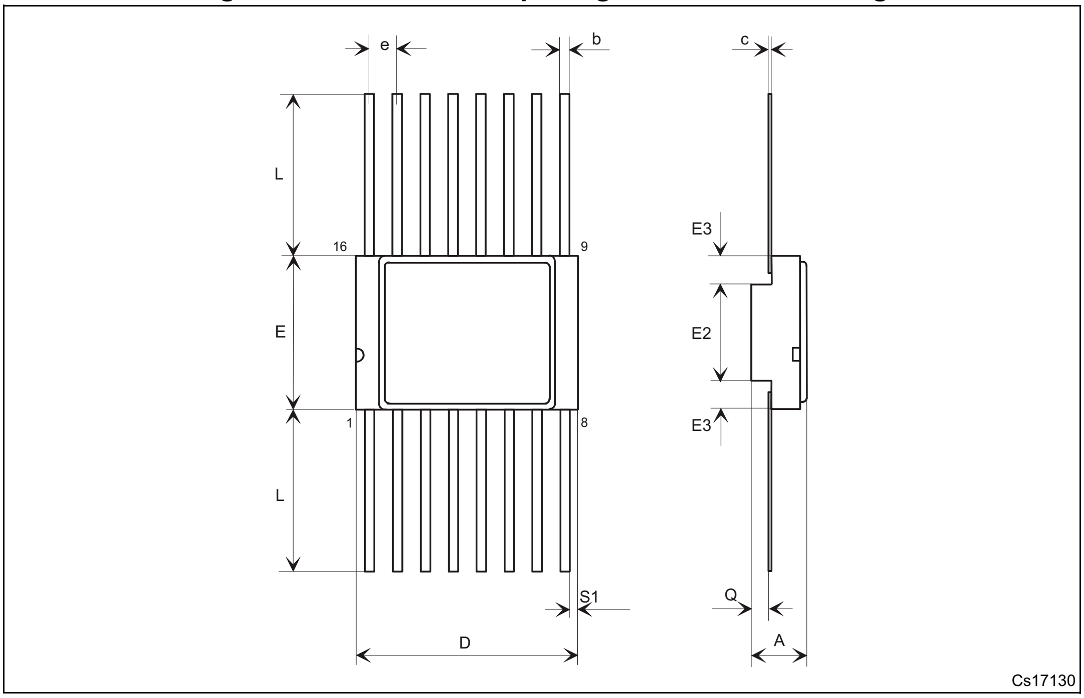
1. All input pulses are supplied by a generator with the following characteristics: t_r or $t_f \leq 1$ ns, f_G or $f_{\overline{G}}$ = 500 kHz, and pulse width G or $\overline{G}$ = 500 ns.
2. The product is guaranteed in test with CL = 10 pF

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

7.1 Ceramic Flat-16 package information

Figure 6. Ceramic Flat-16 package mechanical drawing



1. *The upper metallic lid is electrically connected to ground.*

Table 8. Ceramic Flat-16 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.31		2.72	0.091		0.107
b	0.38		0.48	0.015		0.019
c	0.10		0.18	0.004		0.007
D	9.75		10.13	0.384		0.399
E	6.75		7.06	0.266		0.278
E2		4.32			0.170	
E3	0.76			0.030		
e		1.27			0.050	
L	6.35		7.36	0.250		0.290
Q	0.66		1.14	0.026		0.045
S1	0.13			0.005		

8 Ordering information

Table 9. Order codes

Order code	Description	Temp. range	Package	Marking[(1)]	Packing
RHFLVDS315K1	Engineering model	-55 °C to 125 °C	Ceramic Flat-16	RHFLVDS315K1	Strip pack
RHFLVDS315K01V	QML-V flight			TBD	

1. Specific marking only. Complete marking includes the following:
- SMD pin (on QML-V flight only)
- ST logo
- Date code (date the package was sealed) in YYWWA (year, week, and lot index of week)
- QML logo (Q or V)
- Country of origin (FR = France).

Note: Contact your ST sales office for information regarding the specific conditions for products in die form and QML-Q versions.

9 Shipping information

Date code

The date code is structured as follows:

- Engineering model: EM xyywwz
- QML flight model: FM yywwz

Where:

x = 3 (EM only), assembly location Rennes (France)

yy = last two digits of the year

ww = week digits

z = lot index of the week

10 Revision history

Table 10. Document revision history

Date	Revision	Changes
21-Oct-2015	1	Initial release
28-Apr-2017	2	*Table 1: Device summary*: added mass value