ESDA8V2-1MX2

EOS and ESD Transil™ protection for charger and battery port

Features

- Breakdown voltage V_{BR} = 8.2 V
- Unidirectional device
- High peak power dissipation: 500 W (8/20 µs waveform)
- ESD protection level better than IEC 61000-4-2, level 4: 30 kV contact discharge
- Low leakage current (< 0.5 µA @ 5 V)
- Very small PCB area (1.45 mm^2)
- RoHS compliant

Benefits

- High EOS and ESD protection level
- High integration
- Suitable for high density boards
- Tiny package

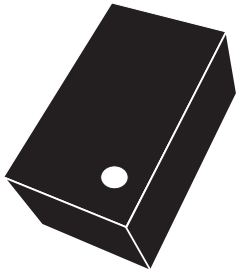
Complies with the following standards:

- IEC 61000-4-2 level 4
  - ±15 kV (air discharge)
  - ±8 kV (contact discharge)
- MIL STD 883G - Method 3015-7: class 3B
  - HBM (human body model): ≥8kV

Applications

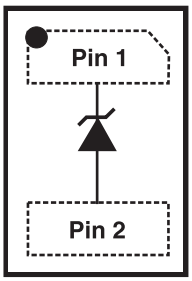
Where EOS and ESD transient overvoltage protection in sensitive equipment is required, such as:

- Computers
- Printers
- Communication systems
- Cellular phone handsets and accessories
- Video equipment



µQFN 2L package

Figure 1. Functional diagram (top view)



Description

The ESDA8V2-1MX2 is a unidirectional single line Transil diode designed specifically for the protection of integrated circuits in portable equipment and miniaturized electonic devices subject to EOS and ESD transient overvoltages.

TM: Transil is a trademark of STMicroelectronics

1 Characteristics

Table 1. Absolute maximum ratings (T_{amb} = 25 °C)

Symbol	Parameter		Value	Unit
V_{PP}	ESD discharge: IEC 61000-4-2 air discharge on input pin IEC 61000-4-2 contact discharge on input pin MIL STD 883G - Method 3015-7: class 3B		 ±30 ±30 ±30	kV
P_{PP}	Peak pulse power dissipation (8/20 µs) (1)	$T_{j\ initial} = T_{amb}$	500	W
I_{PP}	Peak pulse current (8/20 µs)		27	A
T_j	Junction temperature range		-40 to +125	°C
T_{stg}	Storage temperature range		- 55 to +150	°C
T_L	Maximum lead temperature for soldering during 10 s		260	°C

1. For a surge greater than the maximum values, the diode will fail in short-circuit

Table 2. Electrical characteristics (definitions)

Symbol	Parameter
V_{BR}	Breakdown voltage
I_{RM}	Leakage current @ V_{RM}
V_{RM}	Stand-of voltage
V_{CL}	Clamping voltage
I_{PP}	Peak pulse current
C_{line}	Input line capacitance

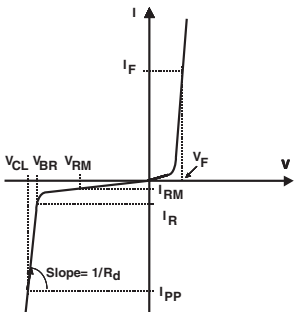


Table 3. Electrical characteristics (values, T_{amb} = 25 °C)

Symbol	Test Condition	Min	Typ	Max	Unit
V_{BR}	I_R = 1 mA	8.2			V
I_{RM}	V_{RM} = 5 V		0.1	0.5	µA
V_{CL}	I_{PP} = 1 A (8/20 µs waveform)			12	V
	I_{PP} = 5 A (8/20 µs waveform)			13	V
	I_{pp} = 27 A (8/20 µs waveform)			18.5	V
C_{line}	V_R = 0 V, F_{osc} = 1 MHz, V_{osc} = 30 mV		350	430	pF

Figure 2. Relative variation of peak pulse power versus initial junction temperature (8/20 µs, typical values)

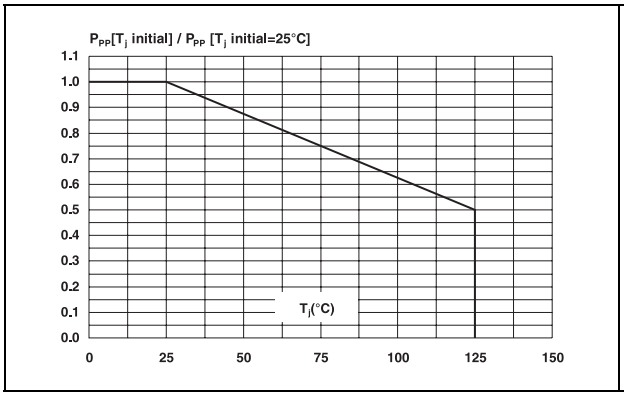


Figure 3. Peak pulse power versus exponential pulse duration (typical values)

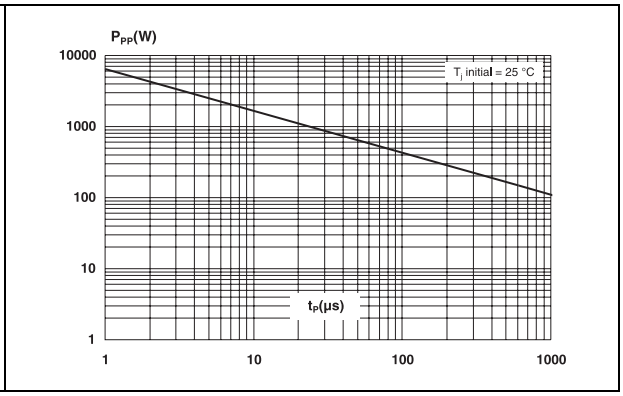


Figure 4. Clamping voltage versus peak pulse current (8/20 µs, typical values)

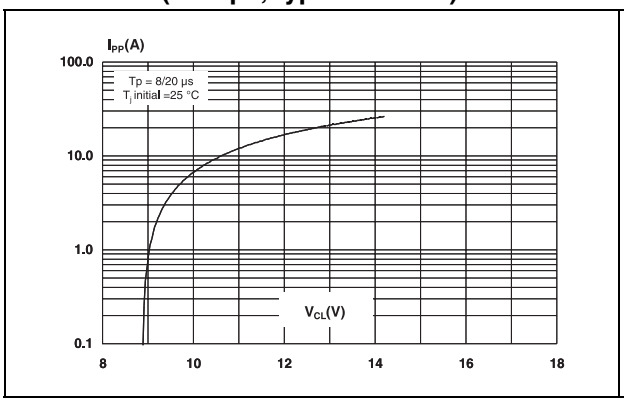


Figure 5. Forward voltage drop versus peak forward current (typical values)

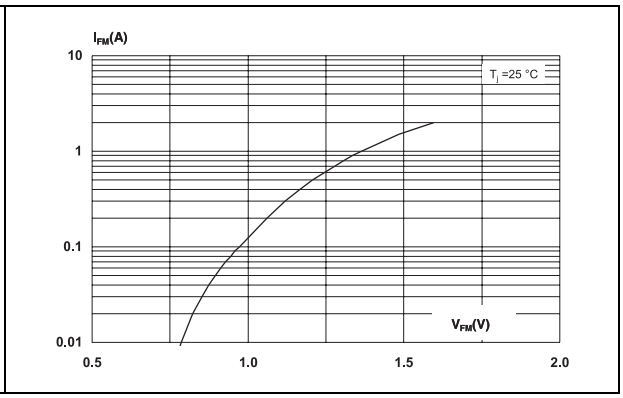


Figure 6. Junction capacitance versus reverse voltage applied (typical values)

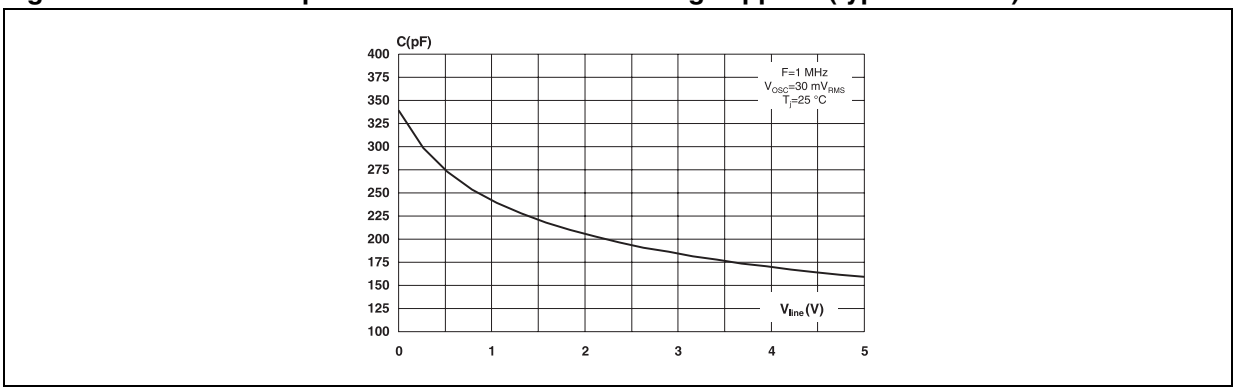


Figure 7. ESD response to IEC 61000-4-2 (+30 kV air discharge)

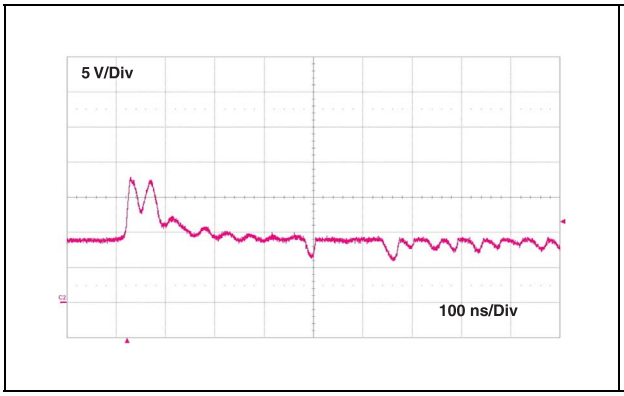
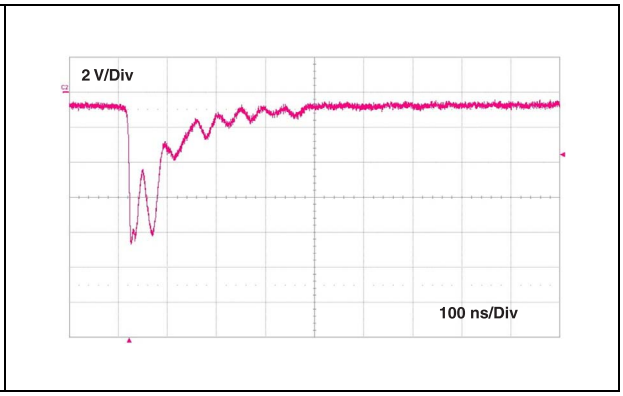
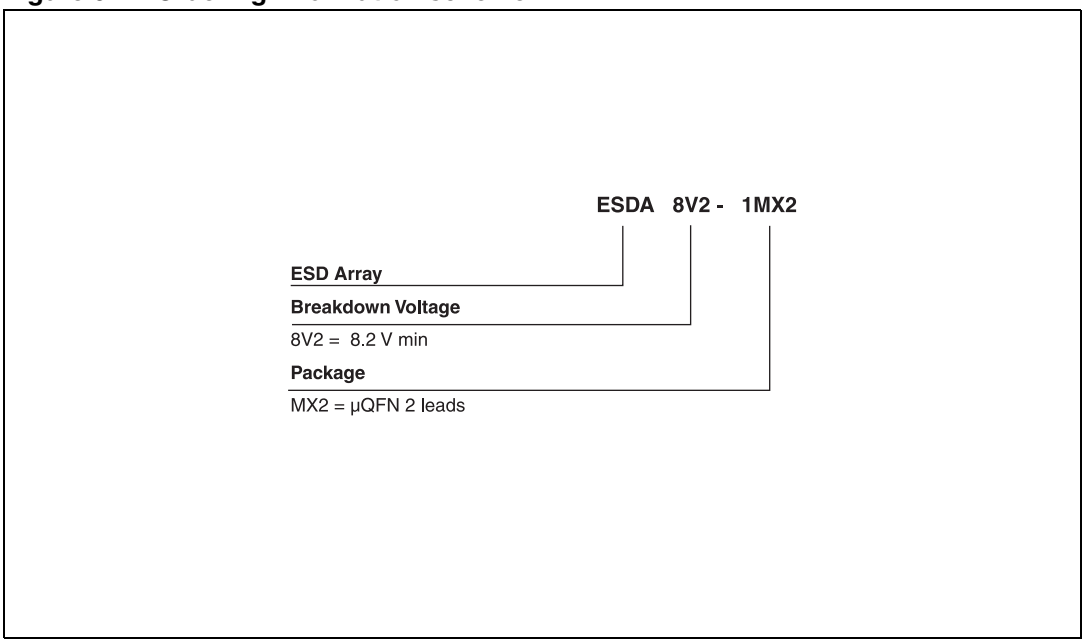


Figure 8. ESD response to IEC 61000-4-2 (-30 kV air discharge)



2 Ordering information scheme

Figure 9. Ordering information scheme

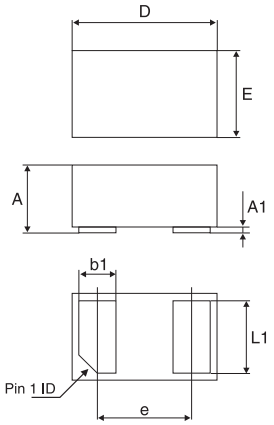


3 Package information

- Epoxy meets UL94, V0

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at *www.st.com*.

Table 4. µQFN 2L dimensions



Ref	Dimensions					
	Millimetres			Inches		
	Min	Typ	Max	Min	Typ	Max
A	0.51	0.55	0.60	0.020	0.022	0.024
A1	0.00	0.02	0.05	0.000	0.001	0.002
b1	0.25	0.30	0.35	0.010	0.012	0.014
D		1.45			0.057	
E		1.00			0.039	
e	0.95	1.00	1.05	0.037	0.039	0.041
L1	0.75	0.80	0.85	0.030	0.031	0.033

Figure 10. Footprint (dimensions in mm)

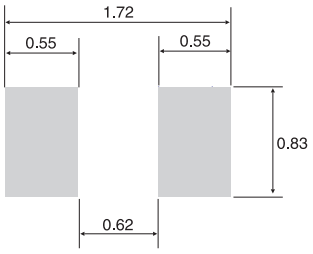
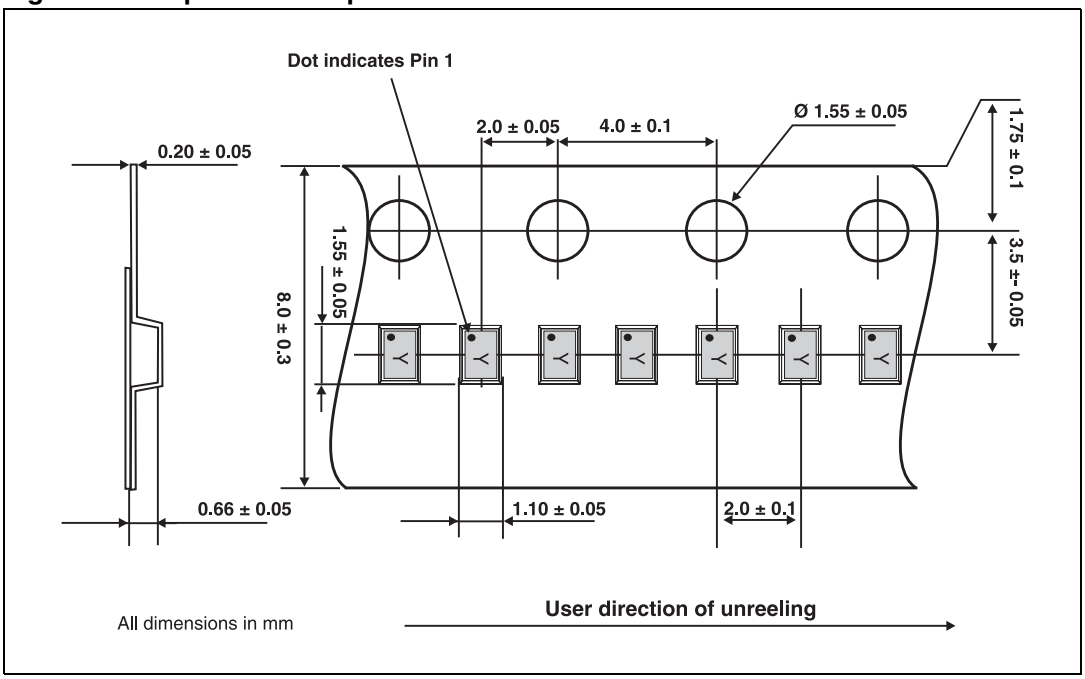


Figure 11. Marking

Note: Product marking may be rotated by 90° for assembly plant differentiation. In no case should this product marking be used to orient the component for its placement on a PCB. Only pin 1 mark is to be used for this purpose.

Figure 12. Tape and reel specifications

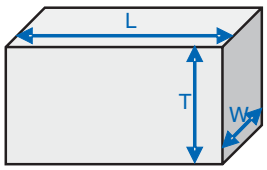


4 Recommendation on PCB assembly

4.1 Stencil opening design

1. General recommendation on stencil opening design
   a) Stencil opening dimensions: L (Length), W (Width), T (Thickness).

Figure 13. Stencil opening dimensions



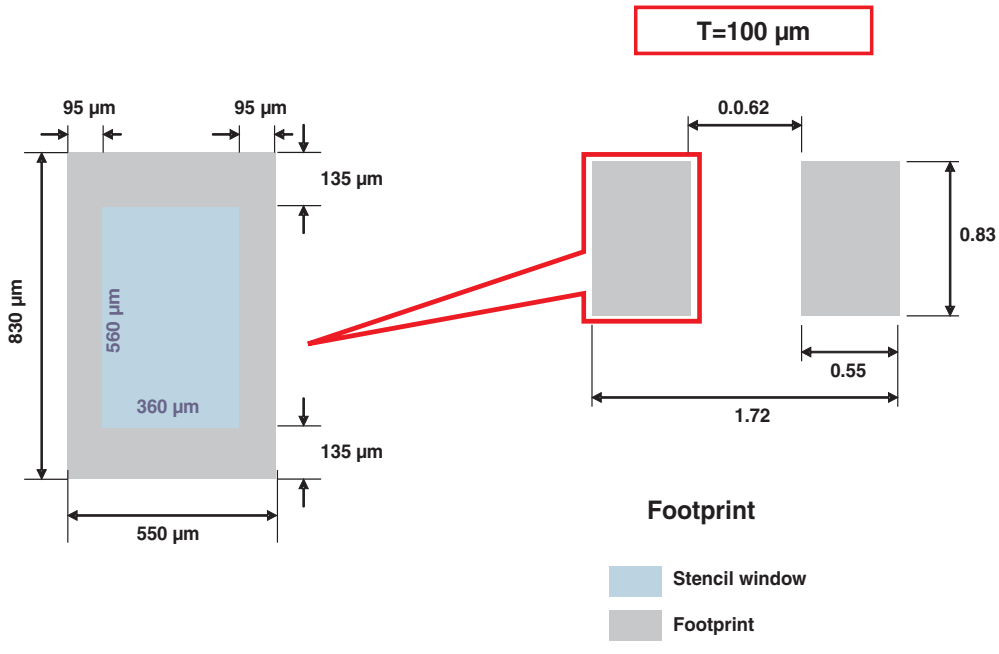
   b) General design rule
   Stencil thickness (T) = 75 ~ 125 µm

$$\text{Aspect Ratio} = \frac{W}{T} \geq 1.5$$

$$\text{Aspect Area} = \frac{L \times W}{2T(L+W)} \geq 0.66$$

2. Reference design
   a) Stencil opening thickness: 100 µm
   b) Stencil opening for leads: Opening to footprint ratio - between 40% and 50%.

Figure 14. Recommended stencil windows position



4.2 Solder paste

1. Halide-free flux qualification ROL0 according to ANSI/J-STD-004.
2. “No clean” solder paste is recommended.
3. Offers a high tack force to resist component movement during high speed
4. Solder paste with fine particles: powder particle size is 20-45 µm.

4.3 Placement

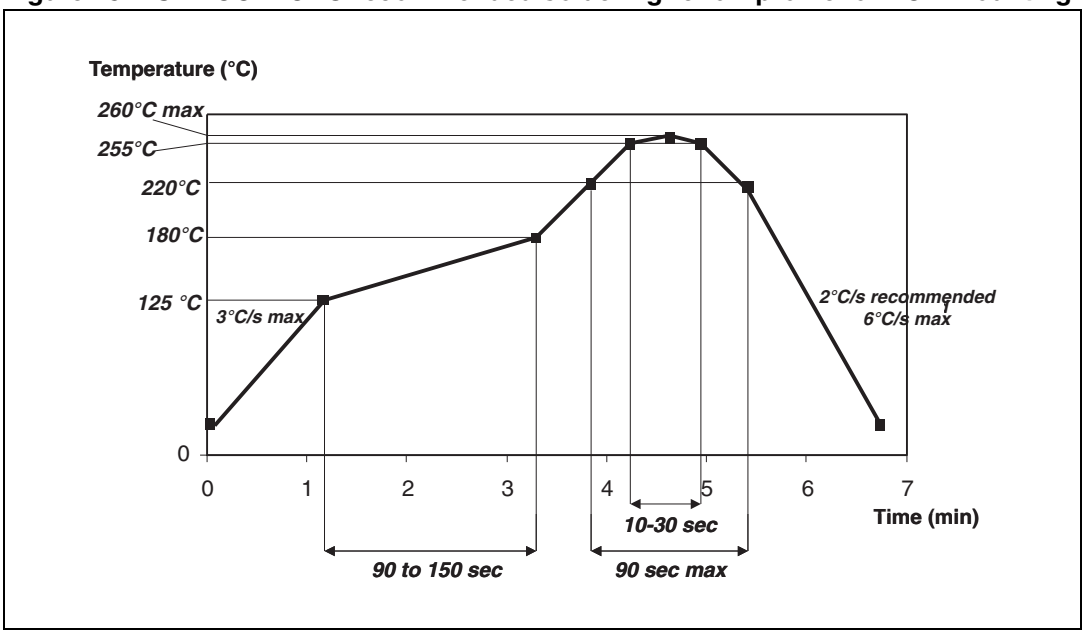
1. Manual positioning is not recommended.
2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering
3. Standard tolerance of ± 0.05 mm is recommended.
4. 3.5 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

4.4 PCB design preference

1. To control the solder paste amount, the closed via is recommended instead of open vias.
2. The position of tracks and open vias in the solder area should be well balanced. The symmetrical layout is recommended, in case any tilt phenomena caused by asymmetrical solder paste amount due to the solder flow away.

4.5 Reflow profile

Figure 15. ST ECOPACK® recommended soldering reflow profile for PCB mounting



Note: Minimize air convection currents in the reflow oven to avoid component movement.

5 Ordering information

Table 5. Ordering information

Order code	Marking	Weight	Base qty	Delivery mode
ESDA8V2-1MX2	Y(1)	2.9 mg	3000	Tape and reel

1. The marking can be rotated by 90° to diferentiate assembly location

6 Revision history

Table 6. Document revision history

Date	Revision	Changes
27-Aug-2008	1	Initial release

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