

August 1989 Revised August 2000

100329

Low Power Octal ECL/TTL Bidirectional Translator with Register

General Description

The 100329 is an octal registered bidirectional translator designed to convert TTL logic levels to 100K ECL logic levels and vice versa. The direction of the translation is determined by the DIR input. A LOW on the output enable input (OE) holds the ECL outputs in a cut-off state and the TTL outputs at a high impedance level. The outputs change synchronously with the rising edge of the clock input (CP) even though only one output is enabled at the time.

The cut-off state is designed to be more negative than a normal ECL LOW level. This allows the output emitter-followers to turn off when the termination supply is –2.0V, presenting a high impedance to the data bus. This high impedance reduces the termination power and prevents loss of low state noise margin when several loads share the bus

The 100329 is designed with FASTTM TTL output buffers, featuring optimal DC drive and capable of quickly charging and discharging highly capacitive loads. All inputs have 50 k Ω pull-down resistors.

Features

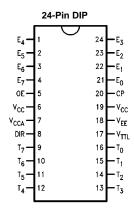
- Bidirectional translation
- ECL high impedance outputs
- Registered outputs
- FAST TTL outputs
- 3-STATE outputs
- Voltage compensated operating range = -4.2V to -5.7V
- High drive IOS

Ordering Code:

Order Number	Package Number	Package Description
100329PC	N24E	24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-010, 0.400 Wide
100329QC	V28A	28-Lead Plastic Lead Chip Carrier (PLCC), JEDEC MO-047, 0.450 Square
100329QI		28-Lead Plastic Lead Chip Carrier (PLCC), JEDEC MO-047, 0.450 Square Industrial Temperature Range (-40°C to +85°C)

Devices also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Connection Diagrams



28-Pin PLCC

T₁ T₂ T₃V_{EES} T₄ T₅ T₆

11 10 9 8 7 6 5

T₀ 12

V_{TIL} 13

V_{EE} 14

V_{EE} 14

V_{EE} 15

V_{CC} 16

CP 17

E₀ 18

19 20 21 22 23 24 25

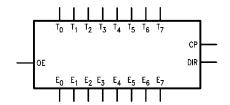
E₁ E₂ E₃V_{EES} E₄ E₅ E₆

FAST® is a registered trademark of Fairchild Semiconductor Corporation.

© 2000 Fairchild Semiconductor Corporation

DS010583

Logic Symbol



Pin Descriptions

Pin Names	Description
E ₀ –E ₇	ECL Data I/O
E ₀ –E ₇ T ₀ –T ₇	TTL Data I/O
OE	Output Enable Input
CP	Clock Pulse Input (Active Rising Edge)
DIR	Direction Control Input

All pins function at 100K ECL levels except for T₀-T₇.

Truth Table

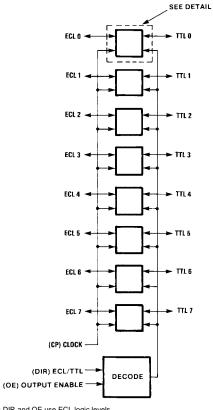
OE	DIR	СР	ECL	TTL	Notes
OE	DIK	CF	Port	Port	Notes
L	L	Χ	Input	Z	(Note 1)(Note 3)
L	Н	Х	LOW	Input	(Note 2)(Note 3)
			(Cut-Off)		
Н	L	\	L	L	(Note 1)
Н	L	\	Н	Н	(Note 1)
Н	L	L	Х	NC	(Note 1)(Note 3)
Н	Н	_	L	L	(Note 2)
Н	Н	\	Н	Н	(Note 2)
Н	Н	L	NC	Χ	(Note 2)(Note 3)

- H = HIGH Voltage Level L = LOW Voltage Level

- X = Don't Care
 Z = High Impedance

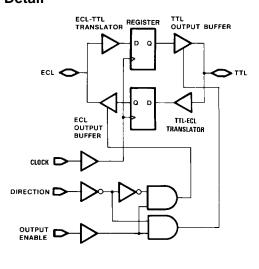
 ✓ = LOW-to-HIGH Clock Transition
- NC = No Change
- Note 1: ECL input to TTL output mode.
- Note 2: TTL input to ECL output mode.
- Note 3: Retains data present before CP.

Functional Diagram



Note: DIR and OE use ECL logic levels

Detail



Absolute Maximum Ratings(Note 4)

-65°C to +150°C Storage Temperature (T_{STG})

Maximum Junction Temperature (T_i) +150°C

V_{EE} Pin Potential to Ground Pin -7.0V to +0.5VV_{TTL} Pin Potential to Ground Pin -0.5V to +6.0VECL Input Voltage (DC) V_{EE} to +0.5V

ECL Output Current

(DC Output HIGH) -50 mA TTL Input Voltage (Note 6) -0.5V to +6.0V TTL Input Current (Note 6) -30 mA to +5.0 mA

Voltage Applied to Output

in HIGH State

3-STATE Output

Current Applied to TTL

Output in LOW State (Max)

ESD (Note 5)

Recommended Operating Conditions

Case Temperature (T_C) 0°C to +85°C ECL Supply Voltage (V_{EE}) -5.7V to -4.2V TTL Supply Voltage (V_{TTL}) +4.5V to +5.5V

Note 4: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical -0.5V to +5.5V Characteristics tables are not guaranteed at the absolute maximum rating. The "Recommended Operating Conditions" table will define the conditions

for actual device operation.

twice the rated I_{OL} (mA) Note 5: ESD testing conforms to MIL-STD-883, Method 3015. ≥2000V Note 6: Either voltage limit or current limit is sufficient to protect inputs.

TTL-to-ECL DC Electrical Characteristics

 $\mbox{V}_{EE} = -4.2 \mbox{V to } -5.7 \mbox{V}, \mbox{ } \mbox{V}_{CC} = \mbox{V}_{CCA} = \mbox{GND}, \mbox{ } \mbox{T}_{C} = 0^{\circ}\mbox{C} \mbox{ to } +85^{\circ}\mbox{C}, \mbox{ } \mbox{V}_{TTL} = +4.5 \mbox{V to } +5.5 \mbox{V (Note 7)}$

Parameter	Min	Тур	Max	Units	Conditions
Output HIGH Voltage	-1025	-955	-870	mV	V _{IN} = V _{IH} (Max) or V _{IL} (Min)
Output LOW Voltage	-1830	-1705	-1620	mV	Loading with 50Ω to –2V
Cutoff Voltage					OE or DIR LOW,
		-2000	-1950	mV	$V_{IN} = V_{IH}$ (Max) or V_{IL} (Min)
					Loading with 50Ω to $-2V$
Output HIGH Voltage	1025			mV	
Corner Point HIGH	-1035				$V_{IN} = V_{IH}$ (Min) or V_{IL} (Max)
Output LOW Voltage			1010	\/	Loading with 50Ω to -2V
Corner Point LOW			-1010	IIIV	
Input HIGH Voltage	2.0		5.0	V	Over V _{TTL} , V _{EE} , T _C Range
Input LOW Voltage	0		0.8	V	Over V _{TTL} , V _{EE} , T _C Range
Input HIGH Current			70	μΑ	V _{IN} = +2.7V
Breakdown Test			1.0	mA	V _{IN} = +5.5V
Input LOW Current	-700			μΑ	V _{IN} = +0.5V
Input Clamp	1.2			V	I 19 mA
Diode Voltage	-1.2			V	$I_{IN} = -18 \text{ mA}$
V _{EE} Supply Current					LE LOW, OE and DIR HIGH
					Inputs Open
	-189		-94	mA	$V_{EE} = -4.2V \text{ to } -4.8V$
	-199		-94		$V_{EE} = -4.2V \text{ to } -5.7V$
	Output LOW Voltage Cutoff Voltage Cutoff Voltage Corner Point HIGH Output LOW Voltage Corner Point LOW Input HIGH Voltage Input LOW Voltage Input LOW Voltage Input HIGH Current Breakdown Test Input LOW Current Input Clamp Diode Voltage	Output LOW Voltage Cutoff Voltage Output HIGH Voltage Corner Point HIGH Output LOW Voltage Corner Point LOW Input HIGH Voltage Input LOW Current Breakdown Test Input LOW Current Input Clamp Diode Voltage VEE Supply Current -189	Output LOW Voltage -1830 -1705 Cutoff Voltage -2000 Output HIGH Voltage -1035 Corner Point HIGH -1035 Output LOW Voltage 2.0 Input HIGH Voltage 0 Input LOW Voltage 0 Input HIGH Current Breakdown Test Input LOW Current -700 Input Clamp -1.2 Diode Voltage VEE Supply Current -189	Output LOW Voltage -1830 -1705 -1620 Cutoff Voltage -2000 -1950 Output HIGH Voltage -1035 -1610 Corner Point HIGH -1610 -1610 Input LOW Voltage 2.0 5.0 Input HIGH Voltage 0 0.8 Input LOW Voltage 0 0.8 Input HIGH Current 70 -700 Breakdown Test 1.0 -1.2 Input LOW Current -7.20 -1.2 Input Clamp -1.2 -1.2 Diode Voltage -1.2 -9.4	Output LOW Voltage -1830 -1705 -1620 mV Cutoff Voltage -2000 -1950 mV Output HIGH Voltage mV mV Corner Point HIGH -1035 mV Input LOW Voltage -1610 mV Input HIGH Voltage 2.0 5.0 V Input LOW Voltage 0 0.8 V Input HIGH Current 70 μA Breakdown Test 1.0 mA Input LOW Current -700 μA Input Clamp -1.2 V Diode Voltage -1.2 V

Note 7: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

ECL-to-TTL DC Electrical Characteristics

 ${\rm V_{EE}} = -4.2 \mbox{V to } -5.7 \mbox{V}, \mbox{ } \mbox{V}_{CC} = \mbox{V}_{CCA} = \mbox{GND}, \mbox{ } \mbox{T}_{C} = 0 \mbox{°C} \mbox{ to } +85 \mbox{°C}, \mbox{ } \mbox{C}_{L} = 50 \mbox{ pF}, \mbox{ } \mbox{V}_{TTL} = +4.5 \mbox{V to } +5.5 \mbox{V (Note 8)} \mbox{Note } \mbox{N$

Symbol	Parameter	Min	Тур	Max	Units	Conditions
V _{OH}	Output HIGH Voltage	2.7	3.1		V	I _{OH} = -3 mA, V _{TTL} = 4.75V
		2.4	2.9		V	$I_{OH} = -3$ mA, $V_{TTL} = 4.50V$
V _{OL}	Output LOW Voltage		0.3	0.5	V	I _{OL} = 24 mA, V _{TTL} = 4.50V
√ _{IH}	Input HIGH Voltage	-1165		-870	mV	Guaranteed HIGH Signal
						for All Inputs
V _{IL}	Input LOW Voltage	-1830		-1475	mV	Guaranteed LOW Signal
						for All Inputs
IH	Input HIGH Current			350	μΑ	V _{IN} = V _{IH} (Max)
IL	Input LOW Current	0.50			μΑ	$V_{IN} = V_{IL}$ (Min)
оzнт	3-STATE Current			70	μΑ	V _{OUT} = +2.7V
	Output HIGH					
l _{OZLT}	3-STATE Current	-700			μΑ	V _{OUT} = +0.5V
	Output LOW					
los	Output Short-Circuit	-225		-100	mA	$V_{OUT} = 0.0V, V_{TTL} = +5.5V$
	Current					
I _{TTL}	V _{TTL} Supply Current			74	mA	TTL Outputs LOW
				49	mA	TTL Outputs HIGH
				67	mA	TTL Outputs in 3-STATE

Note 8: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DIP TTL-to-ECL AC Electrical Characteristics

 $\rm V_{EE} = -4.2V$ to $-5.7V,~V_{TTL} = +4.5V$ to $+5.5V,~V_{CC} = V_{CCA} = GND$

Symbol	Parameter	T _C =	$T_C = 0^{\circ}C$		T _C = 25°C		T _C = 85°C		Conditions
Cyllibol		Min	Max	Min	Max	Min	Max	Units	Conditions
f _{MAX}	Max Toggle Frequency	350		350		350		MHz	
t _{PLH}	CP to E _n	1.7	3.6	1.7	3.7	1.9	3.9	ns	Figures 1, 2
t_{PHL}									
t _{PZH}	OE to E _n	1.3	4.2	1.5	4.4	1.7	4.8	ns	Figures 1, 2
	(Cutoff to HIGH)								
t _{PHZ}	OE to E _n	1.5	4.5	1.6	4.5	1.6	4.6	ns	Figures 1, 2
	(HIGH to Cutoff)								
t _{PHZ}	DIR to E _n	1.6	4.3	1.6	4.3	1.7	4.5	ns	Figures 1, 2
	(HIGH to Cutoff)								
t _{SET}	T _n to CP	1.1		1.1		1.1		ns	Figures 1, 2
t _{HOLD}	T _n to CP	1.7		1.7		1.9		ns	Figures 1, 2
t _{PW} (H)	Pulse Width CP	2.1		2.1		2.1		ns	Figures 1, 2
t _{TLH}	Transition Time	0.6	1.6	0.6	1.6	0.6	1.6	ns	Figures 1, 2
t_{THL}	20% to 80%, 80% to 20%								

DIP ECL-to-TTL AC Electrical Characteristics

 $\rm V_{EE} = -4.2V$ to $-5.7V,~V_{TTL} = +4.5V$ to $+5.5V,~V_{CC} = V_{CCA} = GND,~C_L = 50~pF$

Symbol	Parameter	T _C =	$T_C = 0$ °C		$T_C = 25^{\circ}C$		T _C = 85°C		Conditions
		Min	Max	Min	Max	Min	Max	Units	Conditions
f _{MAX}	Max Toggle Frequency	125		125		125		MHz	
t _{PLH}	CP to T _n	3.1	7.2	3.1	7.2	3.3	7.7	ns	Figures 3, 4
t_{PHL}									
t _{PZH}	OE to T _n	3.4	8.45	3.7	8.95	4.0	9.7	ns	Figures 3, 5
t_{PZL}	(Enable Time)	3.8	9.2	4.0	9.2	4.3	9.95		
t _{PHZ}	OE to T _n	3.2	8.95	3.3	8.95	3.5	9.2	ns	Figures 3, 5
t_{PLZ}	(Disable Time)	3.0	7.7	3.4	8.7	4.1	9.95	115	rigules 5, 5
t _{PHZ}	DIR to T _n	2.7	8.2	2.8	8.7	3.1	8.95	ns	Figures 3, 6
t_{PLZ}	(Disable Time)	2.8	7.45	3.1	7.95	4.0	9.2	115	rigules 3, 6
t _{SET}	E _n to CP	1.1		1.1		1.1		ns	Figures 3, 4
t _{HOLD}	E _n to CP	2.1		2.1		2.6		ns	Figures 3, 4
t _{PW} (H)	Pulse Width CP	4.1		4.1		4.1		ns	Figures 3, 4

PLCC and TTL-to-ECL AC Electrical Characteristics

 $V_{EE} = -4.2 V$ to -5.7 V, $V_{TTL} = +4.5 V$ to +5.5 V

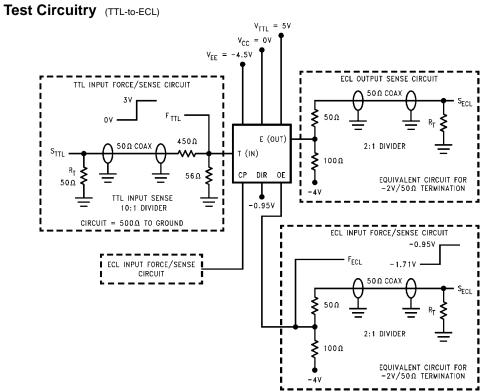
Symbol	Parameter	$T_C = 0$ °C		T _C = 25°C		T _C = 85°C		Units	Conditions
Symbol		Min	Max	Min	Max	Min	Max	Ullits	Conditions
f _{MAX}	Max Toggle Frequency	350		350		350		MHz	
t _{PLH}	CP to E _n	1.7	3.4	1.7	3.5	1.9	3.7	ns	Figures 1, 2
t _{PHL}									
t _{PZH}	OE to E _n	1.3	4.0	1.5	4.2	1.7	4.6	ns	Figures 1, 2
	(Cutoff to HIGH)								
t _{PHZ}	OE to E _n	1.5	4.3	1.6	4.3	1.6	4.4	ns	Figures 1, 2
	(HIGH to Cutoff)								
t _{PHZ}	DIR to E _n	1.6	4.1	1.6	4.1	1.7	4.3	ns	Figures 1, 2
	(HIGH to Cutoff)								
t _{SET}	T _n to CP	1.0		1.0		1.0		ns	Figures 1, 2
t _{HOLD}	T _n to CP	1.7		1.7		1.9		ns	Figures 1, 2
t _{PW} (H)	Pulse Width CP	2.0		2.0		2.0		ns	Figures 1, 2
t _{TLH}	Transition Time	0.6	1.6	0.6	1.6	0.6	1.6	ns	Figures 1, 2
t _{THL}	20% to 80%, 80% to 20%								
toshl	Maximum Skew Common Edge								PLCC Only
	Output-to-Output Variation		200		200		200	ps	(Note 9)
	Data to Output Path								
toslh	Maximum Skew Common Edge								PLCC Only
	Output-to-Output Variation		200		200		200	ps	(Note 9)
	Data to Output Path								
t _{OST}	Maximum Skew Opposite Edge								PLCC Only
	Output-to-Output Variation		650		650		650	ps	(Note 9)
	Data to Output Path								
t _{PS}	Maximum Skew								PLCC Only
	Pin (Signal) Transition Variation		650		650		650	ps	(Note 9)
	Data to Output Path								

Note 9: Output-to-Output Skew is defined as the absolute value of the difference between the actual propagation delay for any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction either HIGH-to-LOW (toshL), or LOW-to-HIGH (tosLH), or in opposite directions both HL and LH (tost). Parameters tost and tops guaranteed by design.

PLCC and ECL-to-TTL AC Electrical Characteristics $V_{\rm EE}$ = -4.2V to -5.7V, $V_{\rm TTL}$ = +4.5V to +5.5V, $C_{\rm L}$ = 50 pF

Symbol	Parameter	$T_C = 0^{\circ}C$		T _C =	$T_C = 25^{\circ}C$		85°C	Units	Conditions
Syllibol		Min	Max	Min	Max	Min	Max	Units	Conditions
f _{MAX}	Max Toggle Frequency	125		125		125		MHz	
t _{PLH}	CP to T _n	3.1	7.0	3.1	7.0	3.3	7.5	ns	Figures 3, 4
t _{PHL}									
t _{PZH}	OE to T _n	3.4	8.25	3.7	8.75	4.0	9.5	ns	Figures 3, 5
t _{PZL}	(Enable Time)	3.8	9.0	4.0	9.0	4.3	9.75		
t _{PHZ}	OE to T _n	3.2	8.75	3.3	8.75	3.5	9.0	ns	Figures 3, 5
t _{PLZ}	(Disable Time)	3.0	7.5	3.4	8.5	4.1	9.75		
t _{PHZ}	DIR to T _n	2.7	8.0	2.8	8.5	3.1	8.75	ns	Figures 3, 6
t _{PLZ}	(Disable Time)	2.8	7.25	3.1	7.75	4.0	9.0		
t _{SET}	E _n to CP	1.0		1.0		1.0		ns	Figures 3, 4
t _{HOLD}	E _n to CP	2.0		2.0		2.5		ns	Figures 3, 4
t _{PW} (H)	Pulse Width CP	4.0		4.0		4.0		ns	Figures 3, 4
t _{OSHL}	Maximum Skew Common Edge								PLCC Only
	Output-to-Output Variation		600		600		600	ps	(Note 10)
	Data to Output Path								
t _{OSLH}	Maximum Skew Common Edge								PLCC Only
	Output-to-Output Variation		850		850		850	ps	(Note 10)
	Data to Output Path								
t _{OST}	Maximum Skew Opposite Edge								PLCC Only
	Output-to-Output Variation		1350		1350		1350	ps	(Note 10)
	Data to Output Path								
t _{PS}	Maximum Skew								PLCC Only
	Pin (Signal) Transition Variation		950		950		950	ps	(Note 10)
	Data to Output Path								

Note 10: Output-to-Output Skew is defined as the absolute value of the difference between the actual propagation delay for any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction either HIGH-to-LOW (t_{OSHL}), or LOW-to-HIGH (t_{OSLH}), or in opposite directions both HL and LH (t_{OST}). Parameters t_{OST} and t_{PS} guaranteed by design.



Note 11: $R_T = 50\Omega$ termination resistive load. When an input or output is being monitored by a scope, R_T is supplied by the scope's 50Ω input resistance. When an input or output is not being monitored, an external 50Ω resistance must be applied to serve as R_T .

Note 12: TTL and ECL force signals are brought to the DUT via 50Ω coax lines.

Note 13: V_{TTL} is decoupled to ground with 0.1 μ F, V_{EE} is decoupled to ground with 0.01 μ F and V_{CC} is connected to ground.

FIGURE 1. TTL-to-ECL AC Test Circuit

Switching Waveforms (TTL-to-ECL) TIL DATA CLOCK DIRECTION CONTROL OUTPUT ENABLE ECL OUTPUT tpD ts | th tpd tpHZ tpHZ tpHZ tpHZ tpHZ tpHZ tpHZ tpHZ tpHZ

FIGURE 2. TTL to ECL Transition—Propagation Delay and Transition Times

Test Circuitry (ECL-to-TTL) $V_{TTL} = 5V$ V_{CC} = 0V ECL INPUT FORCE/SENSE CIRCUIT FECL TTL OUTPUT SENSE CIRCUIT 50Ω COAX LZ/ZL 3-STATE PULL-UP 500Ω E (IN) 450Ω 50Ω COAX **(** 2:1 DIVIDER T (OUT) 100Ω DIR 0E EQUIVALENT CIRCUIT FOR $-2V/50\Omega$ TERMINATION 10:1 DIVIDER -1.69V ECL INPUT FORCE/SENSE CIRCUIT $\mathbf{F}_{\mathsf{ECL}}$ ECL INPUT FORCE/SENSE CIRCUIT O SOO COAX 2:1 DIVIDER 100Ω EQUIVALENT CIRCUIT FOR $-2V/50\,\Omega$ TERMINATION -4V

Note 14: $R_T = 50\Omega$ termination resistive load. When an input or output is being monitored by a scope, R_T is supplied by the scope's 50Ω input resistance. When an input or output is not being monitored, an external 50Ω resistance must be applied to serve as R_T .

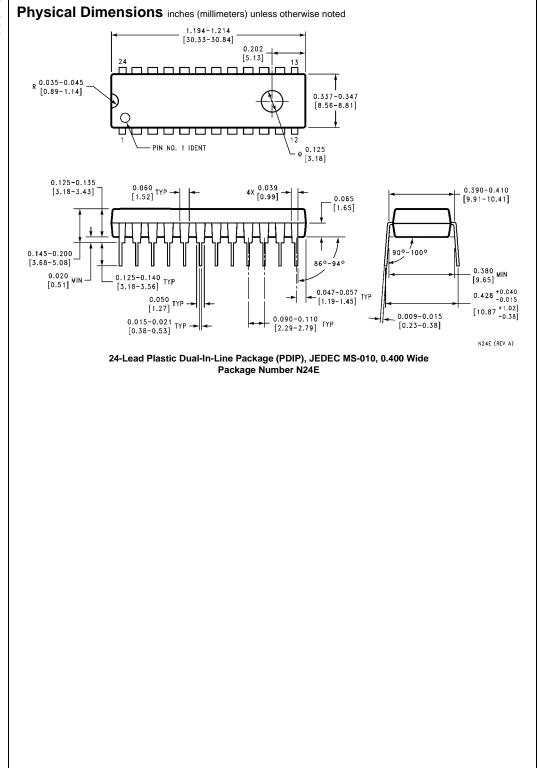
Note 15: The TTL 3-STATE pull-up switch is connected to +7V only for ZL and LZ tests.

Note 16: TTL and ECL force signals are brought to the DUT via 50Ω coax lines.

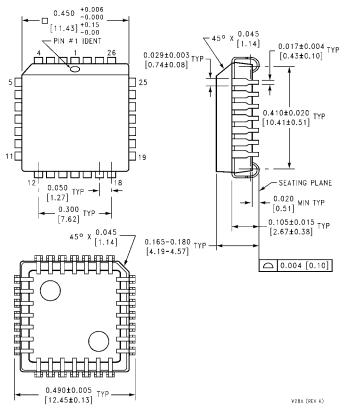
Note 17: V_{TTL} is decoupled to ground with 0.1 μ F, V_{EE} is decoupled to ground with 0.01 μ F and V_{CC} is connected to ground.

FIGURE 3. ECL-to-TTL AC Test Circuit

Switching Waveforms (ECL-to-TTL) ECL DATA CLOCK TTL OUTPUT Note: DIR is LOW, OE is HIGH FIGURE 4. ECL-to-TTL Transition—Propagation Delay and Transition Times OUTPUT ENABLE ${\rm V_{OH}}$ (TTL) TTL OUTPUT t_{PZL}→ ^tPLZ→ | TTL OUTPUT ν_{οL} (πι) Note: DIR is LOW FIGURE 5. ECL-to-TTL Transition, OE to TTL Output, Enable and Disable Times DIRECTION CONTROL ^tPHZ V_{OH} (ΠL) TTL OUTPUT $\mathfrak{t}_{\mathsf{PLZ}}$ TTL OUTPUT V_{OL} (TTL) Note: OE is HIGH FIGURE 6. ECL-to-TTL Transition, DIR to TTL Output, Disable Time



Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



28-Lead Plastic Lead Chip Carrier (PLCC), JEDEC MO-047, 0.450 Square Package Number V28A

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

- Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
- A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.