

MC10H350

PECL* to TTL Translator

(+5 Vdc Power Supply Only)

Description

The MC10H350 is a member of the 10H family of high performance ECL logic. It consists of 4 translators with differential inputs and TTL outputs. The 3-state outputs can be disabled by applying a HIGH TTL logic level on the common OE input.

The MC10H350 is designed to be used primarily in systems incorporating both ECL and TTL logic operating off a common power supply. The separate V_{CC} power pins are not connected internally and thus isolate the noisy TTL V_{CC} runs from the relatively quiet ECL V_{CC} runs on the printed circuit board. The differential inputs allow the MC10H350 to be used as an inverting or noninverting translator, or a differential line receiver. The MC10H350 can also drive CMOS with the addition of a pullup resistor.

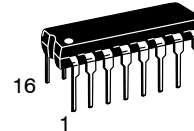
Features

- Propagation Delay, 3.5 ns Typical
- MECL 10K™ Compatible
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant

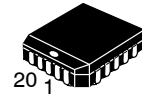


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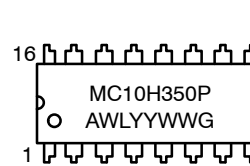


PDIP-16
P SUFFIX
CASE 648-08

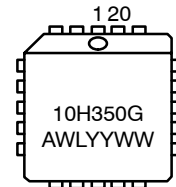


PLLCC-20
FN SUFFIX
CASE 775-02

MARKING DIAGRAMS*



PDIP-16



PLLCC-20

A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G = Pb-Free Package

*For additional marking information, refer to Application Note [AND8002/D](#).

ORDERING INFORMATION

Device	Package	Shipping†
MC10H350FNG	PLLCC-20 (Pb-Free)	46 Units / Tube
MC10H350FNR2G	PLLCC-20 (Pb-Free)	500 Tape & Reel
MC10H350PG	PDIP-16 (Pb-Free)	25 Units / Tube

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

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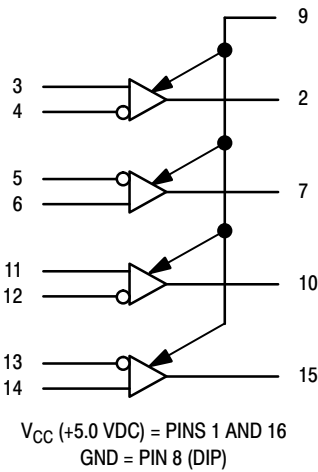
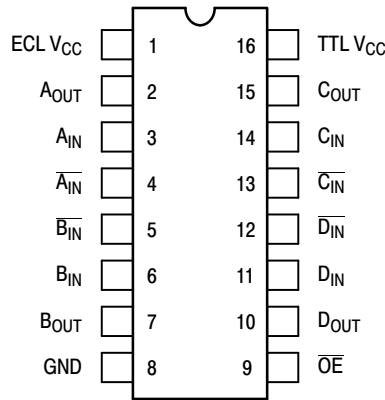


Figure 1. Logic Diagram



Pin assignment is for Dual-in-Line Package.

Figure 2. Dip Pin Assignment

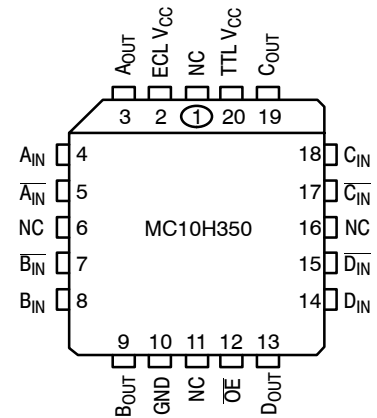


Figure 3. PLCC-20 Pin Assignment

Table 1. MAXIMUM RATINGS

Symbol	Characteristic	Rating	Unit
V_{CC}	Power Supply ($V_{EE} = GND$)	7.0	Vdc
T_A	Operating Temperature Range	0 to +75	°C
T_{stg}	Storage Temperature Range - Plastic	-55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

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Table 2. ELECTRICAL CHARACTERISTICS ($V_{CC} = 5.0 \text{ V} \pm 5\%$) (Note 1)

Symbol	Characteristic	$T_A = 0^\circ\text{C to } 75^\circ\text{C}$		Unit
		Min	Max	
I_{CC}	Power Supply Current TTL ECL	– –	20 12	mA
I_{IH} I_{INH}	Input Current High Pin 9 Others	– –	20 50	μA
I_{IL} I_{INL}	Input Current Low Pin 9 Others	– –	–0.6 50	mA
V_{IH}	Input Voltage High Pin 9	2.0	–	Vdc
V_{IL}	Input Voltage Low Pin 9	–	0.8	Vdc
V_{DIFF}	Differential Input Voltage (Note 1) Pins 3–6, 11–14 (1)	350	–	mV
V_{CM}	Voltage Common Mode Pins 3–6, 11–14	2.8	V_{CC}	Vdc
V_{OH}	Output Voltage High $I_{OH} = 3.0 \text{ mA}$	2.7	–	Vdc
V_{OL}	Output Voltage Low $I_{OL} = 20 \text{ mA}$	–	0.5	Vdc
I_{OS}	Short Circuit Current $V_{OUT} = 0 \text{ V}$	–60	–150	mA
I_{OZH}	Output Disable Current High $V_{OUT} = 2.7 \text{ V}$	–	50	μA
I_{OZL}	Output Disable Current Low $V_{OUT} = 0.5 \text{ V}$	–	–50	μA

*Positive Emitter Coupled Logic

1. Common mode input voltage to pins 3–4, 5–6, 11–12, 13–14 must be between the values of 2.8 V and 5.0 V. This common mode input voltage range includes the differential input swing.
2. For single-ended use, apply 3.75 V (V_{BB}) to either input depending on output polarity required. Signal level range to other input is 3.3 V to 4.2 V.
3. Any unused gates should have the inverting inputs tied to V_{CC} and the noninverting inputs tied to ground to prevent output glitching.

Table 3. AC PARAMETERS ($C_L = 50 \text{ pF}$) ($V_{CC} = 5.0 \pm 5\%$) ($T_A = 0^\circ\text{C to } 75^\circ\text{C}$)

Symbol	Characteristic	$T_A = 0^\circ\text{C to } 75^\circ\text{C}$		Unit
		Min	Max	
t_{pd}	Propagation Delay Data (50% to 1.5 V)	1.5	5.0	ns
t_r	Rise Time (Note 1)	0.3	1.6	ns
t_f	Fall Time (Note 1)	0.3	1.6	ns
t_{pdLZ} t_{pdHZ}	Output Disable Time	2.0 2.0	6.0 6.0	ns
t_{pdZL} t_{pdZH}	Output Enable Time	2.0 2.0	8.0 8.0	ns

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. 1.0 V to 2.0 V w/50 pF into 500 Ω .

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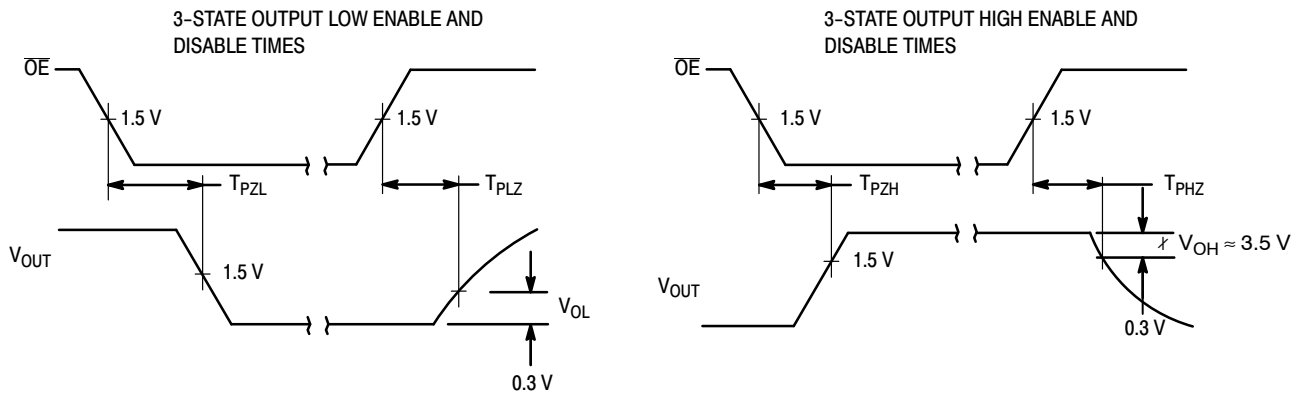
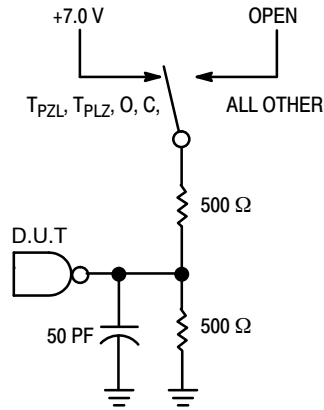


Figure 4. 3-State Switching Waveforms



*INCLUDES JIG AND PROBE CAPACITANCE

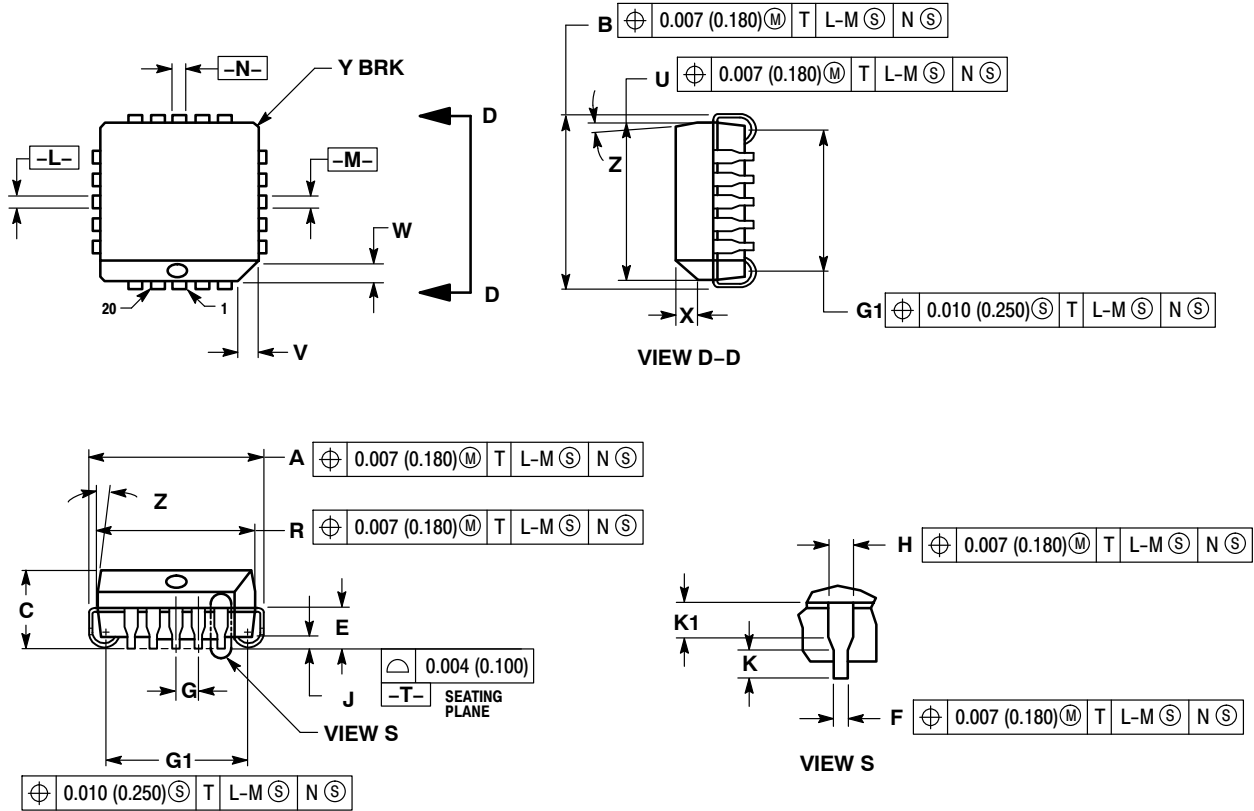
Application Note: Pin 9 is an \overline{OE} and the MC10H350 is disabled when \overline{OE} is at V_{IH} or higher.

Figure 5. Test Load

MC10H350

PACKAGE DIMENSIONS

20 LEAD PLLC
FN SUFFIX
CASE 775-02
ISSUE F



NOTES:

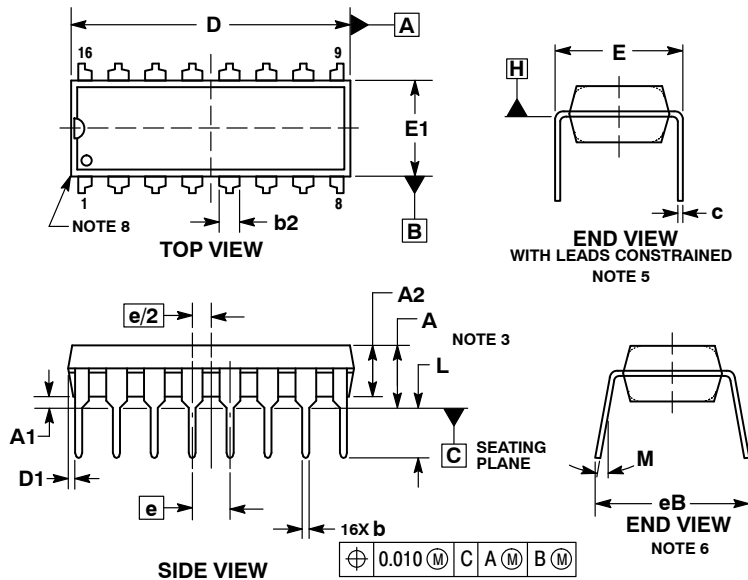
1. DIMENSIONS AND TOLERANCING PER ANSI Y14.5M, 1982.
2. DIMENSIONS IN INCHES.
3. DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
4. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
5. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
6. DIMENSIONS IN THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.385	0.395	9.78	10.03
B	0.385	0.395	9.78	10.03
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.021	0.33	0.53
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	----	0.51	----
K	0.025	----	0.64	----
R	0.350	0.356	8.89	9.04
U	0.350	0.356	8.89	9.04
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	----	0.020	----	0.50
Z	2° 10°		2° 10°	
G1	0.310	0.330	7.88	8.38
K1	0.040	----	1.02	----

MC10H350

PACKAGE DIMENSIONS

PDIP-16
P SUFFIX
CASE 648-08
ISSUE V



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSIONS A, A1 AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS-3.
4. DIMENSIONS D, D1 AND E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS ARE NOT TO EXCEED 0.10 INCH.
5. DIMENSION E IS MEASURED AT A POINT 0.015 BELOW DATUM PLANE H WITH THE LEADS CONSTRAINED PERPENDICULAR TO DATUM C.
6. DIMENSION eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE LEADS, WHERE THE LEADS EXIT THE BODY.
8. PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE CORNERS).

STYLE 1:

- PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. CATHODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE
15. ANODE
16. ANODE

STYLE 2:

- PIN 1. COMMON DRAIN
2. COMMON DRAIN
3. COMMON DRAIN
4. COMMON DRAIN
5. COMMON DRAIN
6. COMMON DRAIN
7. COMMON DRAIN
8. COMMON DRAIN
9. GATE
10. SOURCE
11. GATE
12. SOURCE
13. GATE
14. SOURCE
15. GATE
16. SOURCE

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