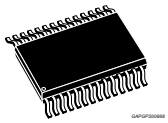
TDA7721

5 band car audio processor

Datasheet - production data



TSSOP28

Features

- Input multiplexer
  - QD1 to QD2: quasi-differential stereo input
  - SE1 to SE3: stereo single-ended input
- InGain
  - 6 dB with 1 dB steps
- Loudness
  - 2nd order frequency response
  - Programmable center frequency (400 Hz / 800 Hz / 2400 Hz)
  - 15 dB with 1 dB steps
  - Selectable high frequency boost
  - Selectable flat-mode (constant attenuation)
- Volume
  - +23 dB to -79 dB with 1 dB step resolution
  - SoftStep control with programmable blend times
- EQ1
  - 2nd order frequency response
  - Center frequency programmable in 4 steps (63 Hz / 80 Hz/ 100 Hz /125 Hz)
  - Q programmable in 4 steps (1.0/1.25/1.5/2.0)
  - -15 to 15 dB range with 1 dB resolution
- EQ2
  - 2nd order frequency response
  - Center frequency programmable in 4 steps (200 Hz/ 250 Hz/ 315 Hz/ 400 Hz)
  - Q programmable in 4 steps (1.0/1.25/1.5/2.0)
  - -15 to 15 dB range with 1 dB resolution
- EQ3
  - 2nd order frequency response
  - Center frequency programmable in 4 steps (630 Hz/ 800 Hz/ 1 kHz/ 1.25 kHz)
  - Q programmable in 4 steps (0.75/1.0/1.25/2)
  - -15 to 15 dB range with 1 dB resolution
- EQ4
  - 2nd order frequency response
  - Center frequency programmable in 4 steps (2 kHz/ 2.5 kHz/ 3.15 kHz/ 4 kHz)
  - Q programmable in 4 steps (0.75/1.0/1.25/2)
  - -15 to 15 dB range with 1 dB resolution
- EQ5
  - 2nd order frequency response
  - Center frequency programmable in 4 steps (6.3 kHz/ 8 kHz / 10 kHz/ 12.5 kHz)
  - Q programmable in 4 steps (0.75/1.0/1.25/2)
  - -15 to 15 dB range with 1 dB resolution
- Highpass
  - 2nd order frequency response
  - Center frequency programmable in 5 steps (63 Hz / 100 Hz / 120 Hz / 150 Hz/ 180 Hz)
- Subwoofer
  - 2nd order low pass filter
  - Programmable cut off frequency
  - (55 Hz / 85 Hz / 120 Hz / 160 Hz)
- Speaker
  - 6 independent soft step speaker controls
  - +15 dB to -79 dB with 1 dB steps
  - Three selectable output DC level
  - Direct mute
- Mute functions
  - Direct mute
  - Digitally controlled SoftMute with 4 programmable mute-times
  - (0.48 ms / 0.96 ms / 8 ms / 16 ms)
- Offset detection
  - Offset voltage detection circuit for on-board power amplifier failure diagnosis

Table 1. Device summary

Order code	Package	Packing
TDA7721	TSSOP28	Tube
TDA7721TR	TSSOP28	Tape and reel

Contents

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1 Description and block diagram

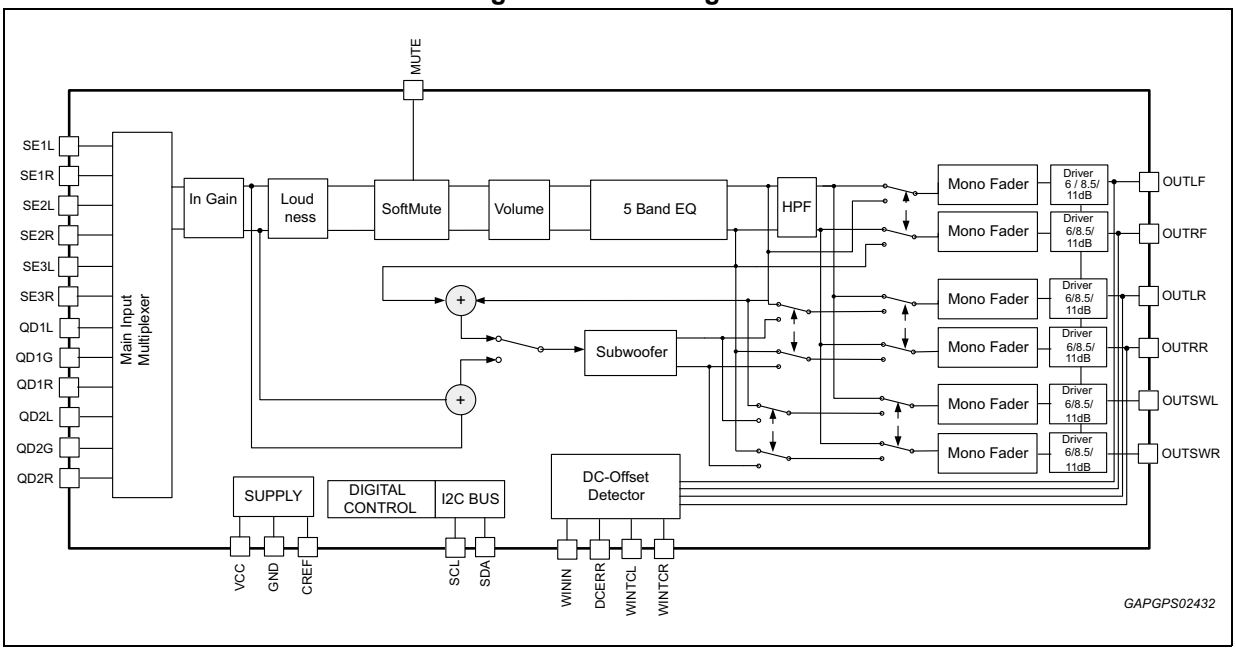
1.1 Description

The TDA7721 is a high performance signal processor specifically designed for car radio applications.

The device includes a high performance audio processor with fully integrated audio filters and new SoftStep architecture. The digital control allows programming in a wide range of filter characteristics.

1.2 Block diagram

Figure 1. Block diagram



2 Pin connections and description

2.1 Pin connections

Figure 2. Pin connections (top view)

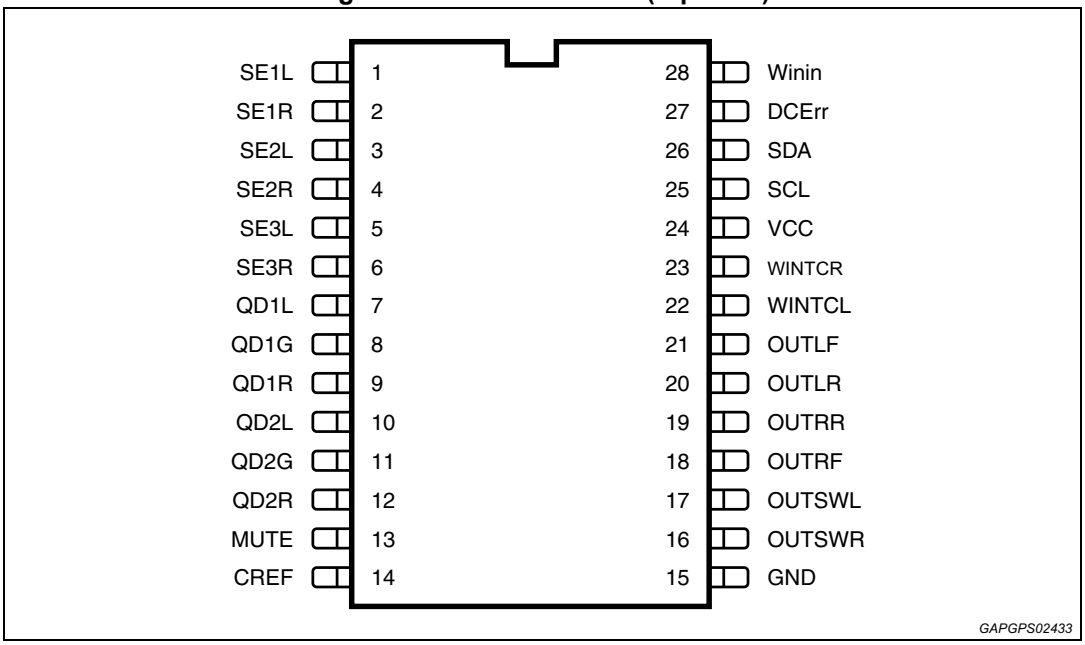


Table 2. Pin description

N#	Pin name	Description	I/O
1	SE1L	Single-end input left	I
2	SE1R	Single-end input right	I
3	SE2L	Single-end input left	I
4	SE2R	Single-end input right	I
5	SE3L	Single-end input left	I
6	SE3R	Single-end input right	I
7	QD1L	Quasi-differential stereo inputs left	I
8	QD1G	Quasi-differential stereo inputs common	I
9	QD1R	Quasi-differential stereo inputs right	I
10	QD2L	Quasi-differential stereo inputs left	I
11	QD2G	Quasi-differential stereo inputs common	I
12	QD2R	Quasi-differential stereo inputs right	I
13	MUTE	External mute pin	I
14	CREF	Reference capacitor	O
15	GND	Ground	S

Table 2. Pin description (continued)

N#	Pin name	Description	I/O
16	OUTSWR	Subwoofer right output	O
17	OUTSWL	Subwoofer left output	O
18	OUTRF	Front right output	O
19	OUTRR	Rear right output	O
20	OUTLR	Rear left output	O
21	OUTLF	Front left output	O
22	WINTCL	DC offset detector filter output left channel	O
23	WINTCR	DC offset detector filter output right channel	O
24	VCC	Supply	S
25	SCL	I^2C bus clock	I
26	SDA	I^2C bus data	I/O
27	DCERR	DC offset detector output	O
28	WININ	DC offset detector input	I

3 Electrical specifications

3.1 Thermal data

Table 3. Thermal data

Symbol	Description	Value	Unit
$R_{th\text{-}jamb}$	Thermal resistance junction-to-ambient	114	°C/W

3.2 Absolute maximum ratings

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_S	Operating supply voltage	13	V
V_{in_max}	Maximum voltage for signal input pins	7	V
T_{amb}	Operating ambient temperature	-40 to 85	°C
T_{stg}	Storage temperature range	-55 to 150	°C

3.3 Electrical characteristics

V_s =11.5 V; T_{amb} = 25 °C; R_L = 10 kΩ; all gains = 0 dB; f = 1 kHz; Output gain = 6 dB; Input = SE1; unless otherwise specified

Table 5. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Supply						
Vs	Supply voltage	-	4.5	8.5	13	V
Is	Supply current	-	33	40	47	mA
Input selector						
R_{in}	Input resistance clipping level	All single ended inputs	70	100	130	kΩ
V_{CL}		Input gain = 0dB, when $V_{CC} \geq 5$ V THD = 1%	0.9	1.06	-	V_{RMS}
		Input gain = 0dB, when V_{CC} = 4.5 V THD = 1%	0.6	0.707		V_{RMS}
S_{IN}	Input separation	-	80	100		dB
V_{ib}	Input bias voltage	All single-ended and differential stereo inputs	2.3	2.5	2.7	V
Differential stereo inputs						
R_{in}	Input resistance	Differential	70	100	-	kΩ

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
CMRR	Common mode rejection ratio for main source	V_{CM} = 1 V_{RMS} @ 1 kHz	46	60	-	dB
		V_{CM} = 1 V_{RMS} @ 10 kHz	46	60	-	dB
Loudness control						
A_{MAX}	Max attenuation	-	14	15	16	dB
A_{STEP}	Step resolution	-	0.5	1	1.5	dB
f_{Peak}	Peak frequency(1)	f_{P1}	-	400	-	Hz
		f_{P2}	-	800	-	Hz
		f_{P3}	-	2400	-	Hz
IN gain						
G_{MAX}	Max Gain(2)	-	5	6	7	dB
A_{STEP}	Step resolution	-	0.5	1	1.5	dB
E_T	Tracking error	-			2	dB
V_{DC}	DC steps	Adjacent gain steps	-5	0.5	5	mV
Volume control						
G_{MAX}	Max gain(2)	-	21	23	25	dB
A_{MAX}	Max attenuation	-	-83	-79	-75	dB
A_{STEP}	Step resolution	-	0.5	1	1.5	dB
E_A	Attenuation set error	G = -20 to +23 dB	-0.75	0	+0.75	dB
		G = -20 to -79 dB	-4	0	3	dB
E_T	Tracking error	-			2	dB
V_{DC}	DC steps	Adjacent attenuation steps	-3	0.1	3	mV
		Adjacent gain step from +23dB to +15dB	-15	-	15	mV
		Adjacent gain step From +15dB to 0dB	-5	-	5	mV
Soft mute						
A_{MUTE}	Mute attenuation	-	80	100	-	dB
T_D	Delay time	T_1	0.36	0.48	0.6	ms
		T_2	0.84	0.96	1.08	ms
		T_3	0.3	7.6	7.9	ms
		T_4	14	15.3	16.8	ms
V_{TH_Low}	Low threshold for MUTE pin(3)	-	-	-	1	V
V_{TH_High}	High threshold for MUTE pin(3)	-	2.5	-	-	V
RPU	Internal pull-up resistor for MUTE pin(3)	-	32	45	58	k

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
VPU	Internal pull-up Voltage for MUTE Pin(3)	-	-	3.3	-	V
EQ1 control						
C_{RANGE}	Control range(2)	-	14	15	16	dB
A_{STEP}	Step resolution	-	0.5	1	1.5	dB
F_c	Center frequency(1)	f_{C1}	-	63	-	Hz
		f_{C2}	-	80	-	Hz
		f_{C3}	-	100	-	Hz
		f_{C4}	-	125	-	Hz
Q1	Quality factor(1)	Q1	-	1.0	-	-
		Q2	-	1.25	-	-
		Q3	-	1.5	-	-
		Q4		2	-	-
EQ2 control						
C_{RANGE}	Control range(2)	-	14	15	16	dB
A_{STEP}	Step resolution	-	0.5	1	1.5	dB
F_c	Center frequency(1)	f_{C1}	-	200	-	Hz
		f_{C2}	-	250	-	Hz
		f_{C3}	-	315	-	Hz
		f_{C4}	-	400	-	Hz
Q2	Quality factor(1)	Q1	-	1.0	-	-
		Q2	-	1.25	-	-
		Q3	-	1.5	-	-
		Q4	-	2	-	-
EQ3 control						
C_{RANGE}	Control range(2)	-	14	15	16	dB
A_{STEP}	Step resolution	-	0.5	1	1.5	dB
F_c	Center frequency(1)	f_{C1}	-	630	-	Hz
		f_{C2}	-	800	-	Hz
		f_{C3}	-	1	-	kHz
		f_{C4}	-	1.25	-	kHz

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Q3	Quality factor(1)	Q1	-	0.75	-	-
		Q2	-	1.0	-	
		Q3	-	1.25	-	-
		Q4	-	2.0	-	-
EQ4 control						
C_{RANGE}	Control range(2)	-	14	15	16	dB
A_{STEP}	Step resolution(1)	-	0.5	1	1.5	dB
F_c	Center frequency(1)	f_{C1}	-	2	-	kHz
		f_{C2}	-	2.5	-	kHz
		f_{C3}	-	3.15	-	kHz
		f_{C4}	-	4	-	kHz
Q_4	Quality factor	Q1	-	0.75	-	-
		Q2	-	1.0	-	-
		Q3	-	1.25	-	-
		Q4	-	2.0	-	-
EQ5 control						
C_{RANGE}	Control range(2)	-	14	15	16	dB
A_{STEP}	Step resolution	-	0.5	1	1.5	dB
F_c	Center frequency(1)	f_{C1}	-	6.3	-	kHz
		f_{C2}	-	8	-	kHz
		f_{C3}	-	10	-	kHz
		f_{C4}	-	12.5	-	kHz
Q_5	Quality factor(1)	Q1	-	0.75	-	-
		Q2	-	1.0	-	-
		Q3	-	1.25	-	-
		Q4	-	2.0	-	-
Speaker attenuators						
G_{MAX}	Max gain(2)	-	14	15	16	dB
A_{MAX}	Max attenuation	-	-83	-79	-75	dB
A_{STEP}	Step resolution	-	0.5	1	1.5	dB
A_{MUTE}	Mute attenuation	-	80	90		dB
E_A	Attenuation set error	G = -20 to +15 dB	-0.75	0	+0.75	dB
		G = -20 to -79 dB	-4	0	3	dB

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{DC}	DC Steps	Adjacent attenuation steps	-5	0.1	5	mV
		Adjacent gain steps	-10	0.5	10	
HPF						
F_{HP}	Highpass corner frequency(1)	f_{HP1}	-	63	-	Hz
		f_{HP2}	-	100	-	Hz
		f_{HP3}	-	120	-	Hz
		f_{HP4}	-	150	-	Hz
		f_{HP5}	-	180	-	Hz
Audio outputs						
V_{CL}	Clipping level	THD = 1%; V_{CC} = 6 V option1	1.9	2.0	-	V_{RMS}
		THD = 1%; V_{CC} = 8.2 V option2	2.5	2.6	-	V_{RMS}
		THD = 1%; V_{CC} = 11.5 V option3	3.3	3.6	-	V_{RMS}
		THD = 1%; V_{CC} = 4.5 V option1	0.8	0.92	-	V_{RMS}
		THD = 1%; V_{CC} = 4.5 V option2	0.15	0.21	-	V_{RMS}
R_{OUT}	Output impedance	-	-	30	100	Ω
R_L	Output load resistance	-	2	-	-	kΩ
C_L	Output load capacitor	-	-	-	10	nF
V_{DC}	Output DC level	Option1: Output level = 3 V	2.85	3	3.15	V
		Option2: Output level = 4 V	3.8	4	2	V
		Option3: Output level = 5.75 V; V_{CC} > 6.5 V	5.5	5.75	6	V
G_{OUT}	Output gain	Option1:Output level/gain = 3 V/6 dB	5	6	7	dB
		Option2: Output level/gain = 4 V/8.5 dB	7.5	8.5	9.5	dB
		Option3: Output level/gain = 5.75V/11dB	10	11	12	dB
Subwoofer lowpass						
f_{LP}	Lowpass corner frequency(1)	f_{LP1}	-	55	-	Hz
		f_{LP2}	-	85	-	Hz
		f_{LP3}	-	120	-	Hz
		f_{LP4}	-	160	-	Hz
DC offset detection circuit						
V_{th}	Zero comp window size	V_1	±15	±30	±45	mV
		V_2	±20	±45	±65	mV
		V_3	±30	±60	±90	mV
		V_4	±60	±90	±120	mV

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition		Min.	Typ.	Max.	Unit
τ_{sp}	Max rejected spike length	-		-	11	-	µs
		-		-	22	-	µs
		-		-	33	-	µs
		-		-	44	-	µs
$I_{CHDCErr}$	DCErr charge current	-		3.5	5	6.5	µA
$I_{DISDCErr}$	DCErr discharge current	-		3.5	5	8	mA
V_{OutH}	DCErr high voltage	-		3.1	3.3	3.5	V
V_{OutH}	DCErr low voltage	-		0	100	300	mV
V_{TH_Low}	Low threshold for WinIn Pin(3)	-		-	-	1	V
V_{TH_High}	High threshold for WinIn Pin(3)	-		2.5	-	-	V
RPU	Internal pull-up resistor for WinIn Pin	-		35	50	65	kΩ
VPU	Internal pull-up voltage for WinIn Pin	-		3.1	3.3	3.5	V
General							
e_{NO}	Output Noise	BW = 20 Hz-20 kHz A-Weighted, all gain = 0 dB, HPF = OFF, Input = SE/QD	Output level/gain = 3 V/6 dB	-	20	25	µV
			Output level/gain = 4 V/8.5 dB	-	27	30	µV
			Output level/gain = 5.75 V/11 dB	-	36	40	µV
		BW = 20 Hz-20kHz A-Weighted, Output muted	Output level/gain = 3 V/6 dB	-	6.6	10	µV
			Output level/gain = 4 V /8.5 dB	-	8	12	µV
			Output level/gain =5.75V/11dB	-	10	15	µV
S/N	Signal to noise ratio	all gain = 0dB, A-weighted;	Output level/gain = 3 V/6 dB	98	100	-	dB
			Output level/gain = 4 V/8.5 dB	98	100	-	dB
			Output level/gain=5.75V/11dB	98	100	-	dB

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition		Min.	Typ.	Max.	Unit
D	Distortion	VIN=0.5$V_{RMS;}$ all gain = 0dB, HPF=OFF	Output level/gain=3V/6dB(5V)	-	0.01	0.1	%
			Output level/gain=4V/8.5dB(6V)	-	0.01	0.1	%
			Output level/gain=5.75V/11dB(8.5V)	-	0.01	0.1	%
S_C	Channel separation left/right	-		75	90	-	dB

1. Value guaranteed by measuring correlated parameter.
2. Measure performed in DC.
3. Verified only in characterization.

4 Description of audioprocessor

4.1 Input stage

Two quasi-differential stereo input and three single-ended inputs are available.

4.1.1 Single-ended stereo input (SE1, SE2, SE3)

The input-impedance at each input is 100 kΩ.

4.1.2 Quasi-differential stereo Input (QD1,QD2)

The QD input is implemented as a buffered quasi-differential stereo stage with 100 kΩ input-impedance at each input. There is 0 dB attenuation at QD input stage.

4.1.3 Fast charge

Each differential input pin features a "fast-charge" switch allowing to quickly charge any external large coupling capacitors upon power-on of the device. When the device is powered-on, the "fast-charge" switches are automatically turned on, for normal operations these switches need to be released by any programming of byte_0. After that, the "fast-charge" switches can be turned on/off by setting "fast charge = on/off".

4.2 Input gain

A 0~6dB input gain is selectable to compensate the different input signal.

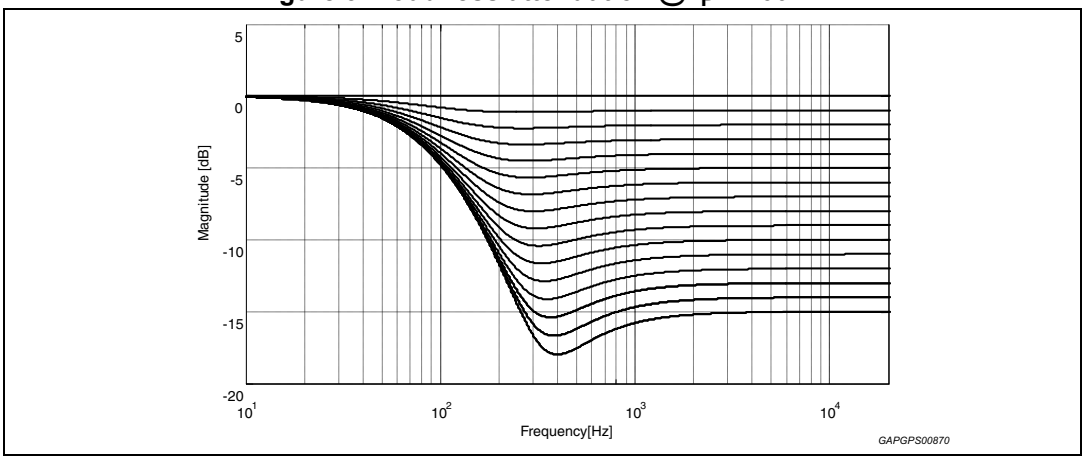
4.3 Loudness

There are four parameters programmable in the loudness stage.

4.3.1 Loudness attenuation

Figure 3 shows the attenuation as a function of frequency at f_P = 400 Hz

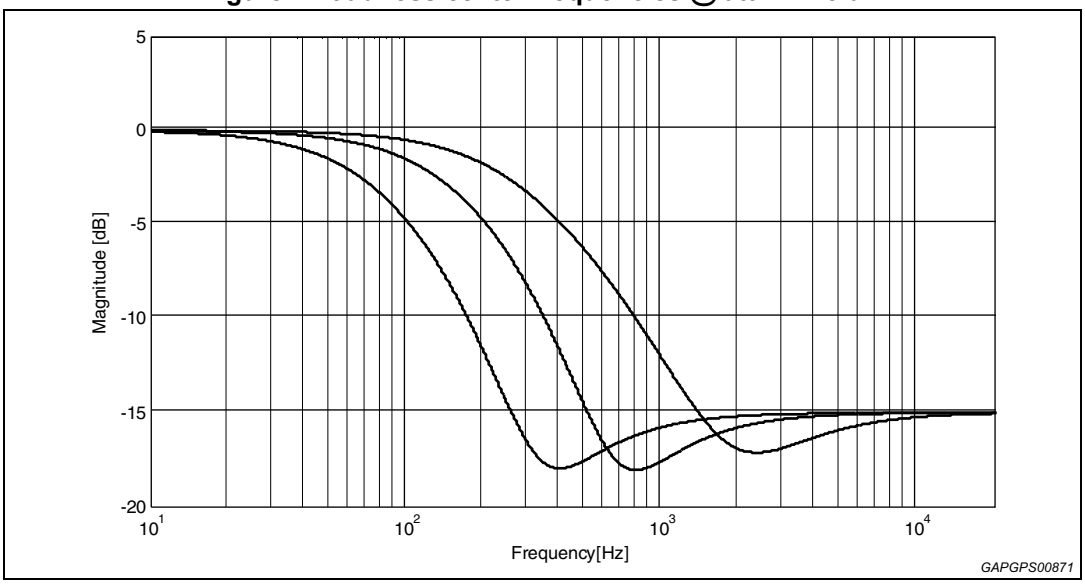
Figure 3. Loudness attenuation @ f_P = 400 Hz



4.3.2 Peak frequency

Figure 4 shows the four possible peak-frequencies at 400, 800 and 2400 Hz

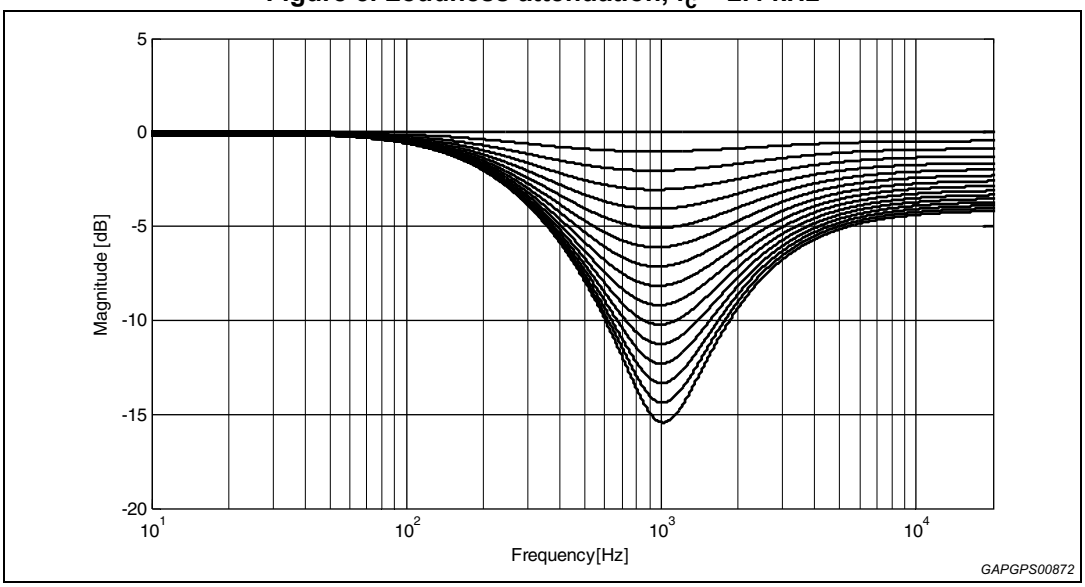
Figure 4. loudness center frequencies @ attn. = 15 dB



4.3.3 High frequency boost

Figure 5 shows the different loudness shapes in low & high frequency boost.

Figure 5. Loudness attenuation, f_c = 2.4 kHz



4.3.4 Flat mode

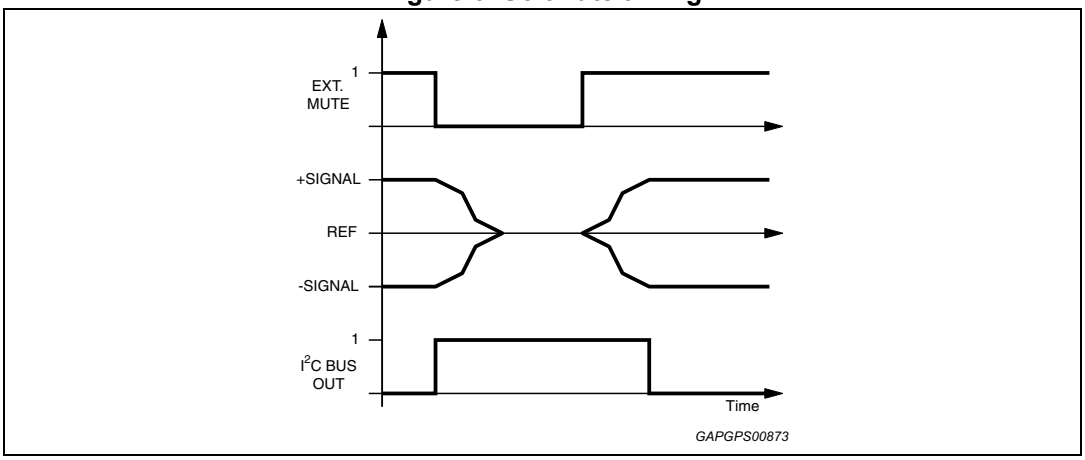
In flat mode the loudness stage works as a 0 dB to -15 dB attenuator.

4.4 SoftMute

The digitally controlled SoftMute stage allows muting/demuting the signal with a I^2C bus programmable slope. The mute process can be activated either by the SoftMute pin or by the I^2C bus. This slope is realized in a special S-shaped curve to mute slow in the critical regions (see *Figure 6*).

For timing purposes the Bit0 of the I^2C bus output register is set to 1 from the start of muting until the end of demuting.

Figure 6. SoftMute timing



Note: Please notice that a started Mute-action is always terminated and could not be interrupted by a change of the mute -signal.

4.5 Volume

When the volume-level is changed audible clicks could appear at the output. The root cause of those clicks could be either a DC-Offset before the volume-stage or the sudden change in the envelope of the audio signal. With the SoftStep-feature both kinds of clicks could be reduced to a minimum and are no more audible. The blend-time from one step to the next is programmable as 5 ms or 10 ms. The SoftStep control is described in detail in *Section 4.13*.

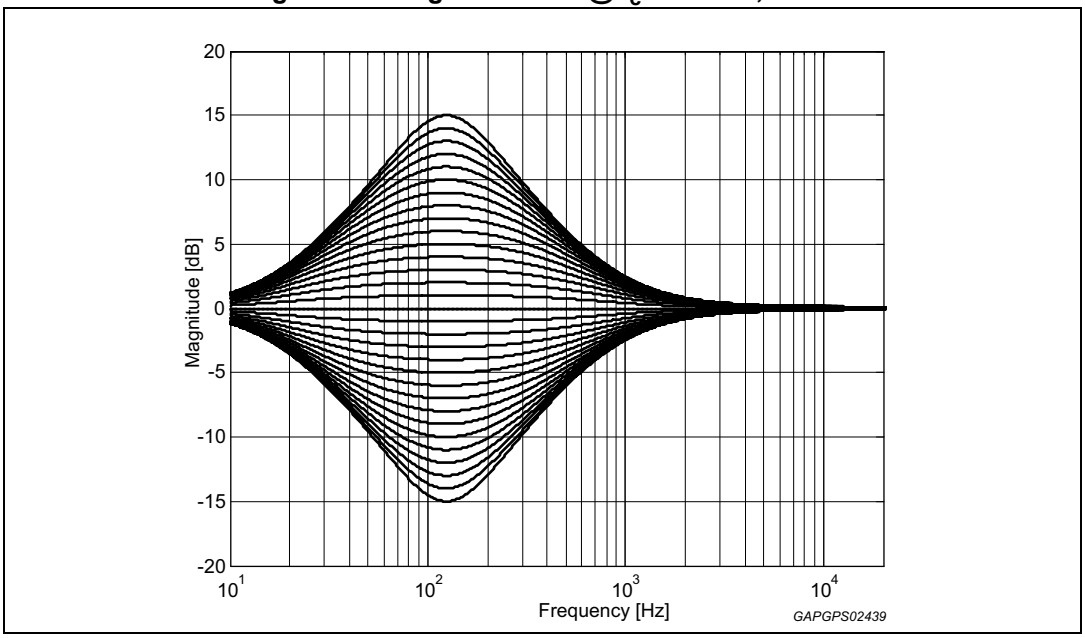
4.6 EQ1

There are three parameters programmable in the EQ1 stage.

4.6.1 EQ1 attenuation

Figure 7 shows the attenuation as a function of frequency at 125 Hz.

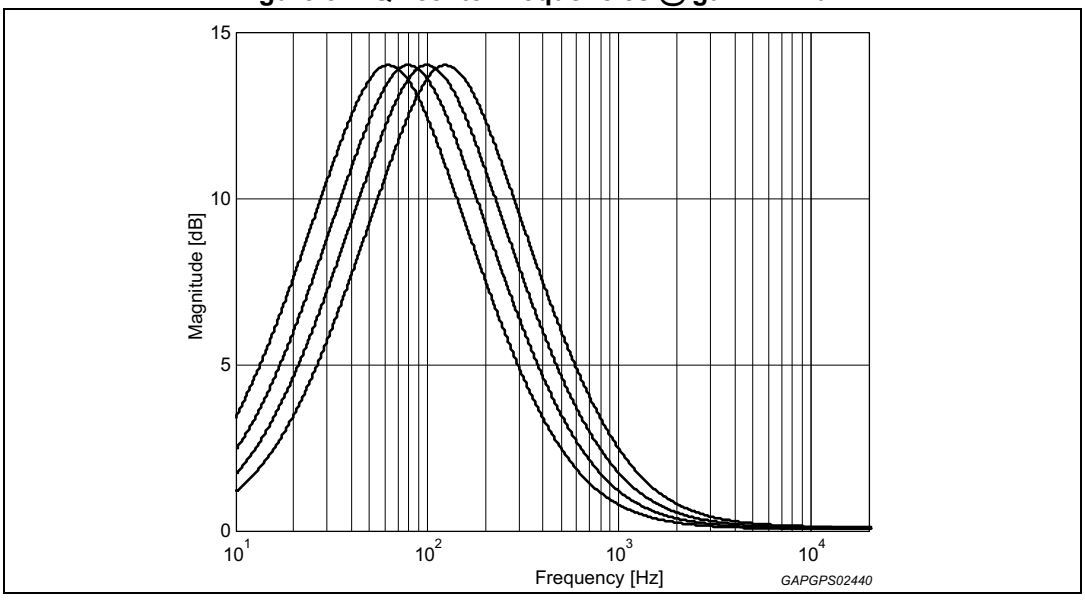
Figure 7. EQ1 gain control @ f_c = 125 Hz, Q = 1



4.6.2 Center frequency

Figure 8 shows the four possible center frequencies 63 Hz/ 80 Hz / 100 Hz/ 125 Hz.

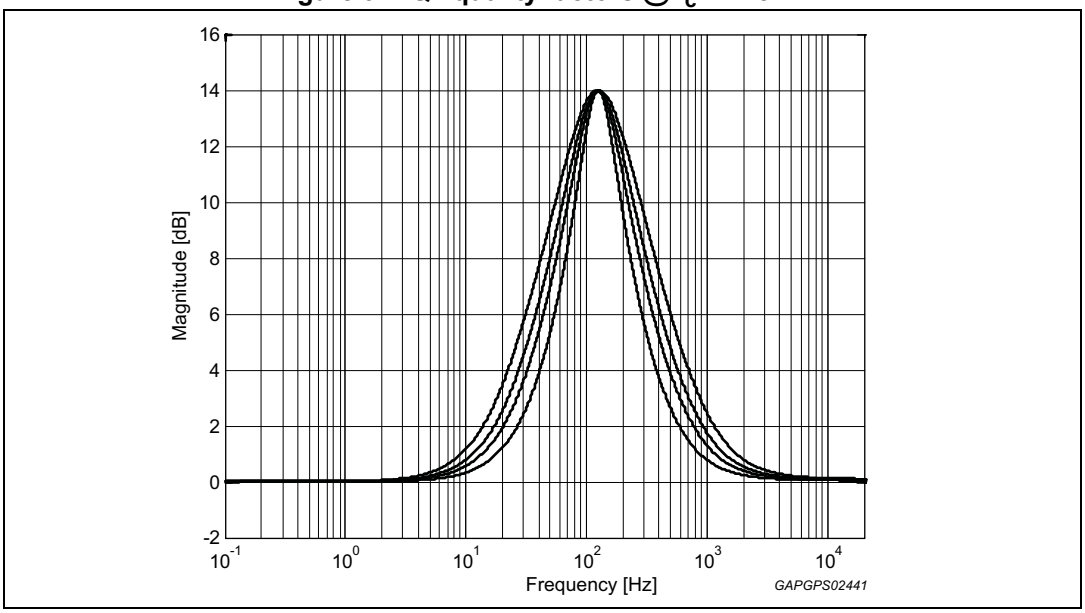
Figure 8. EQ1 center frequencies @ gain = 14 dB



4.6.3 EQ1 quality factor

Figure 9 shows the four possible quality factors (1.0/1.25/1.5/2) when f_c is 125 Hz.

Figure 9. EQ1 quality factors @ f_c = 125 Hz



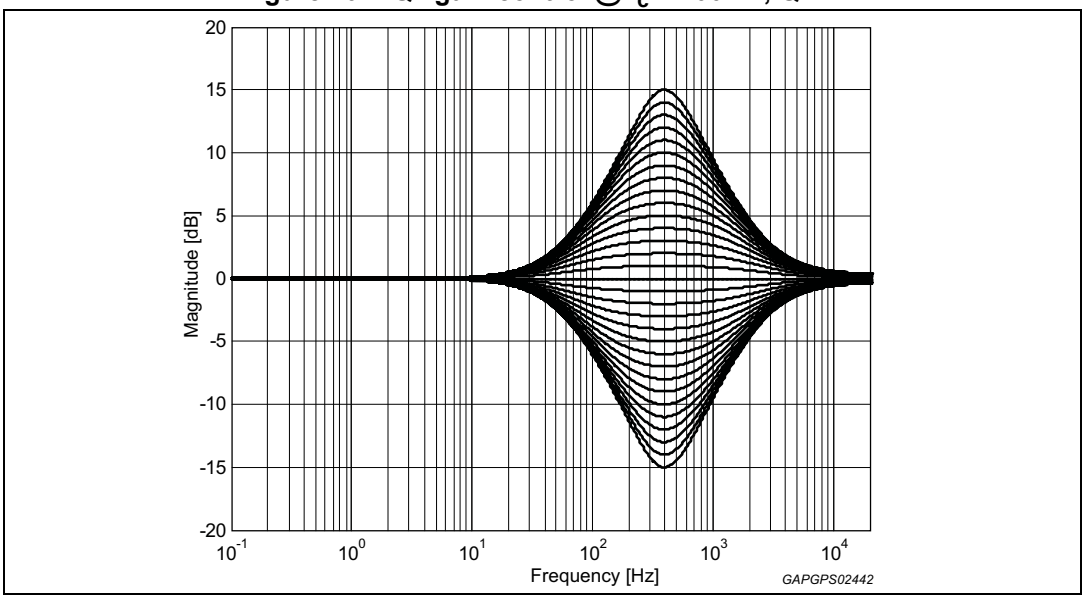
4.7 EQ2

There are three parameters programmable in the EQ2 stage.

4.7.1 EQ2 attenuation

Figure 10 shows the attenuation as a function of frequency at 400 Hz when Q = 1.

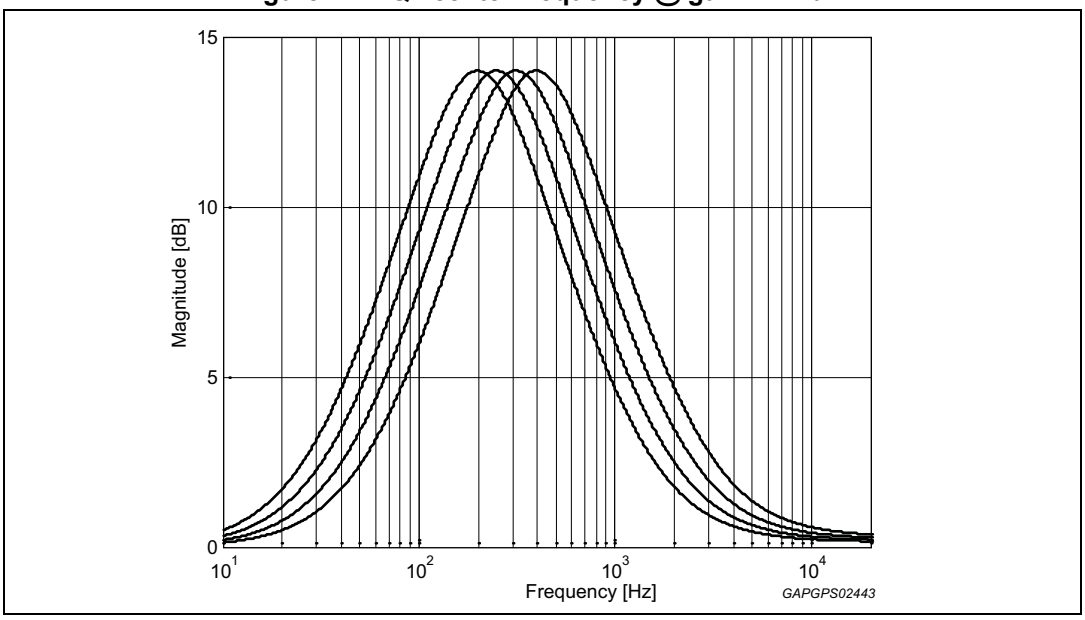
Figure 10. EQ2 gain control @ f_c = 400 Hz, Q = 1



4.7.2 EQ2 center frequency

Figure 11 shows the four possible center frequencies 200/250/315/400 Hz.

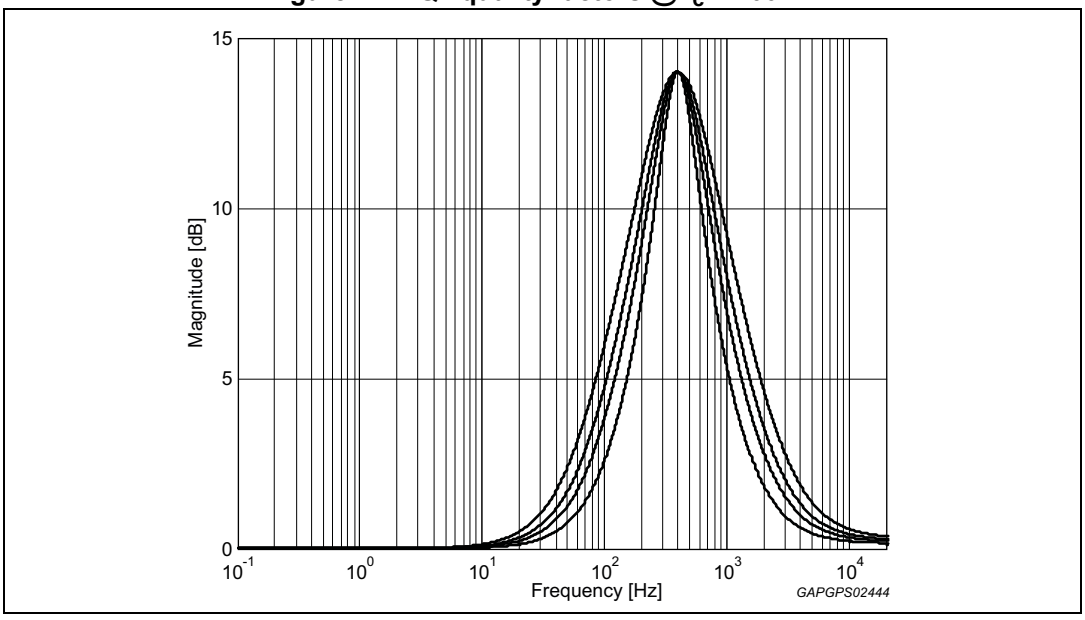
Figure 11. EQ2 center frequency @ gain = 14 dB



4.7.3 EQ2 quality factor

Figure 12 shows the four possible quality factors (1.0/1.25/1.5/2) when f_c is 400 Hz.

Figure 12. EQ2 quality factors @ f_c = 400 Hz



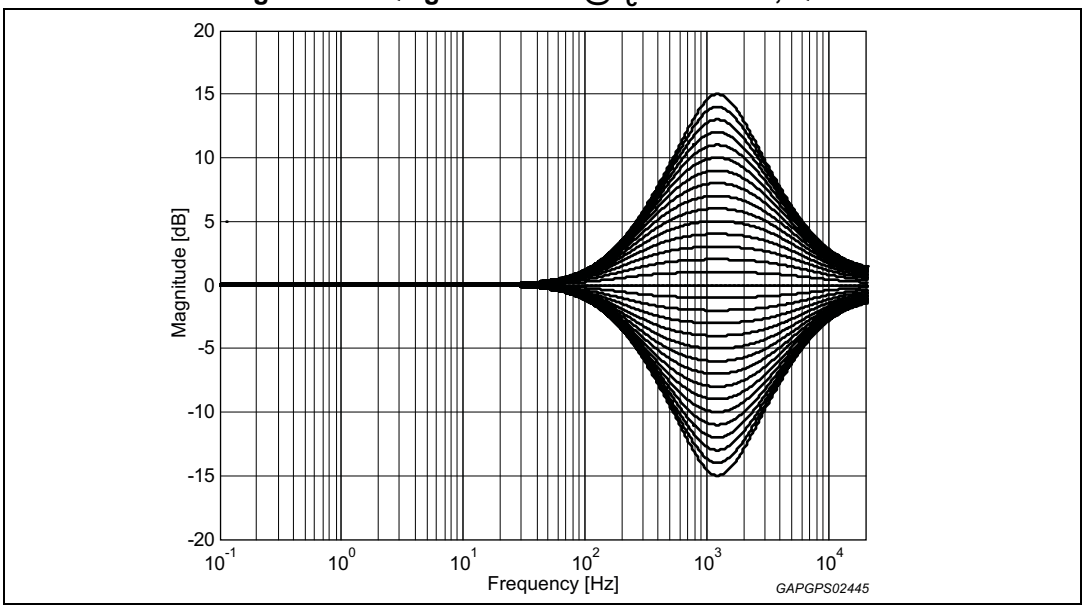
4.8 EQ3

There are three parameters programmable in the EQ3 stage.

4.8.1 EQ3 attenuation

Figure 13 shows the attenuation as a function of frequency at a center frequency of 1.25kHz.

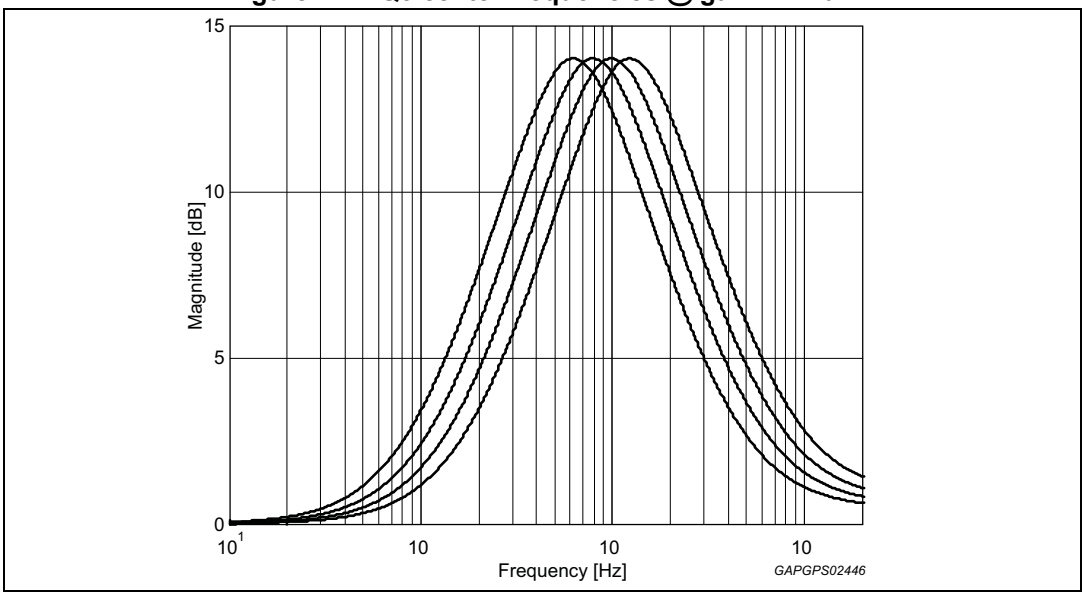
Figure 13. EQ3 gain control @ f_c = 1.25 kHz, Q = 1



4.8.2 Center frequency

Figure 14 shows the four possible center frequencies 630 Hz, 800 Hz, 1 kHz, 1.25 kHz.

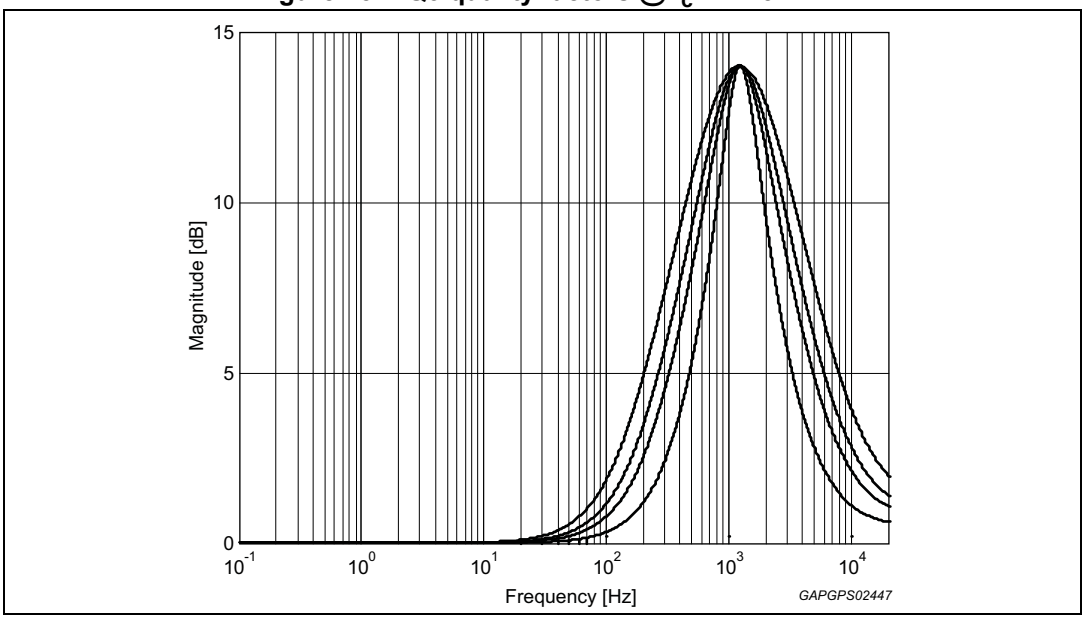
Figure 14. EQ3 center frequencies @ gain = 14 dB



4.8.3 EQ3 quality factor

Figure 15 shows the four possible quality factors (0.75/1.0/1.25/2.0) when f_c is1.25 kHz.

Figure 15. EQ3 quality factors @ f_c = 1.25 kHz



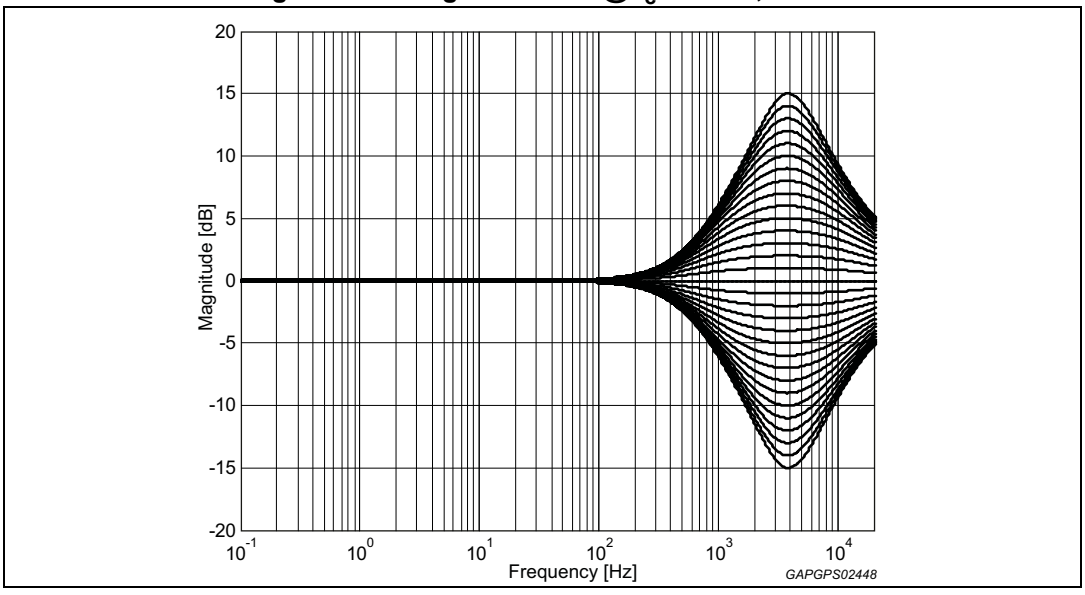
4.9 EQ4

There are three parameters programmable in the EQ4 stage.

4.9.1 EQ4 attenuation

Figure 16 shows the attenuation as a function of frequency at a center frequency of 4 kHz.

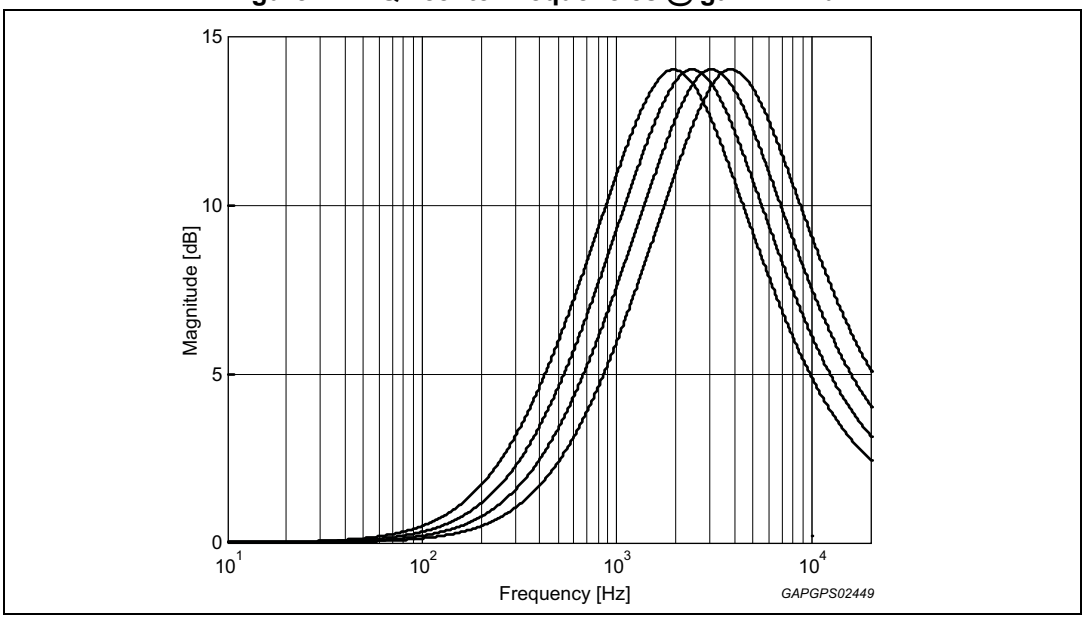
Figure 16. EQ4 gain control @ f_c = 4 kHz, Q = 1



4.9.2 Center frequency

Figure 17 shows the four possible center frequencies 2/2.5/3.15/4kHz.

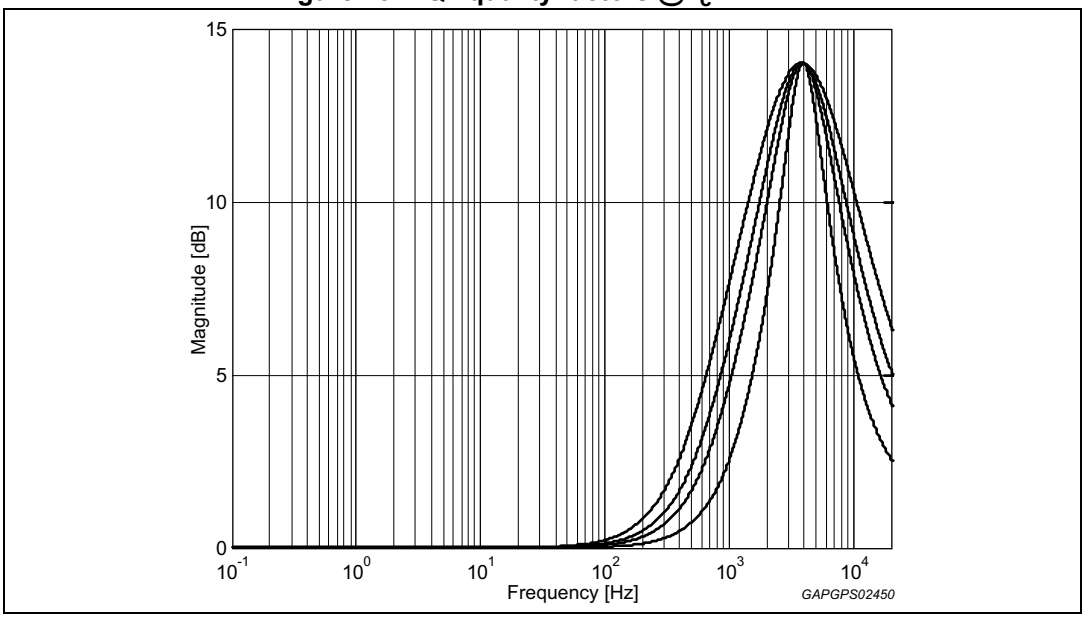
Figure 17. EQ4 center frequencies @ gain = 14 dB



4.9.3 EQ4 quality factor

Figure 18 shows the four possible quality factors(0.75/1.0/1.25/2) when f_c is 4 kHz.

Figure 18. EQ4 quality factors @ f_c = 4 kHz



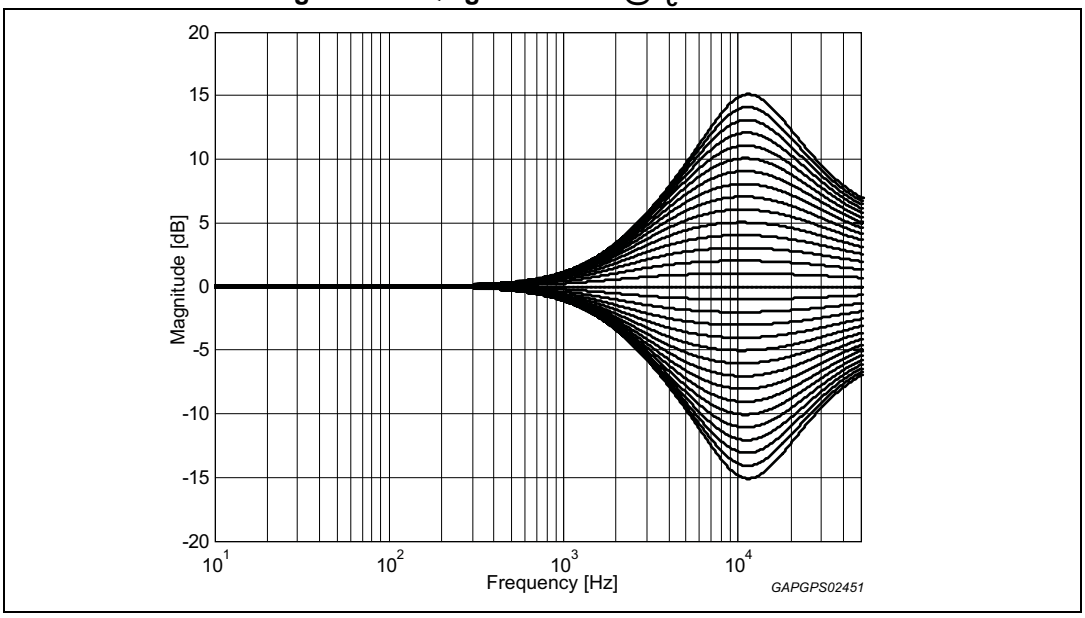
4.10 EQ5

There are three parameters programmable in the EQ5 stage.

4.10.1 EQ5 attenuation

Figure 19 shows the attenuation as a function of frequency at a center frequency of 12.5 kHz.

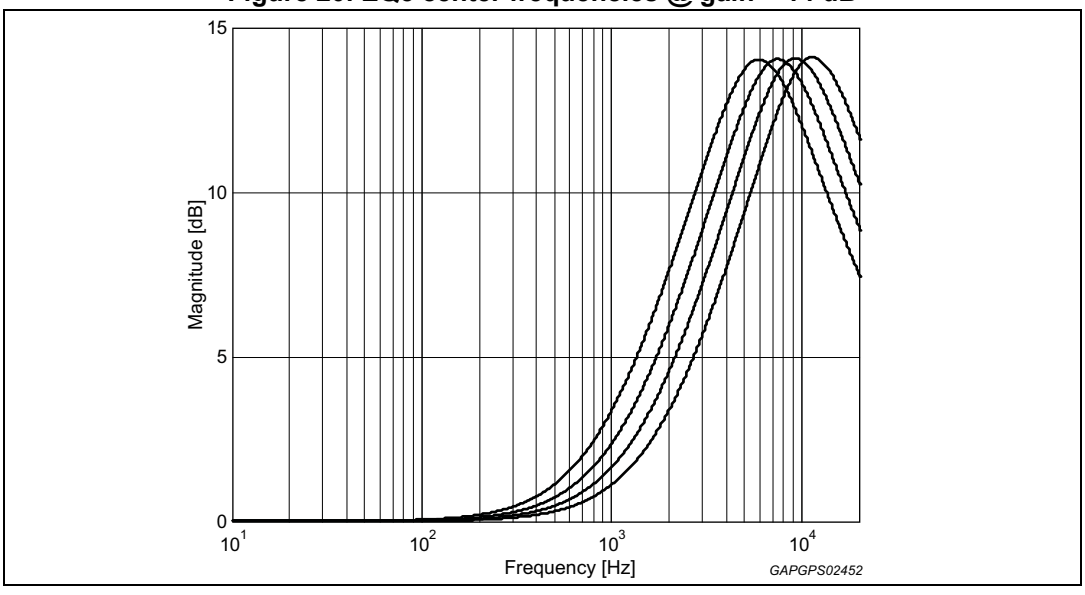
Figure 19. EQ5 gain control @ f_c = 12.5 kHz



4.10.2 Center frequency

Figure 20 shows the four possible center frequencies 6.3/8/10/12.5 kHz.

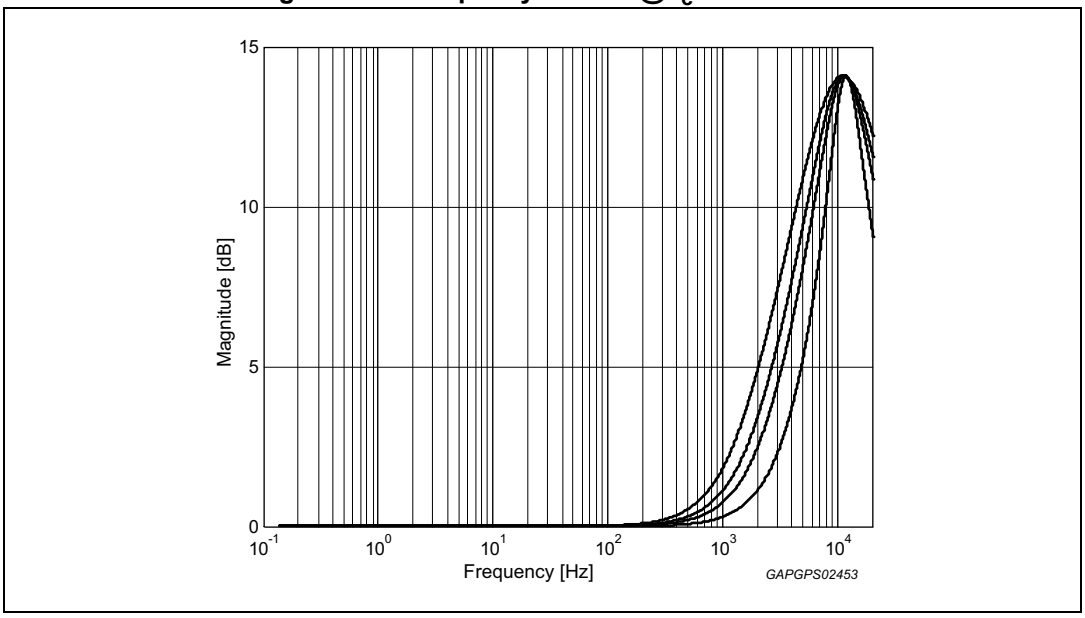
Figure 20. EQ5 center frequencies @ gain = 14 dB



4.10.3 EQ5 quality factor

Figure 21 shows the four possible quality factors(0.75/1.0/1.25/2) when f_c is12.5 kHz.

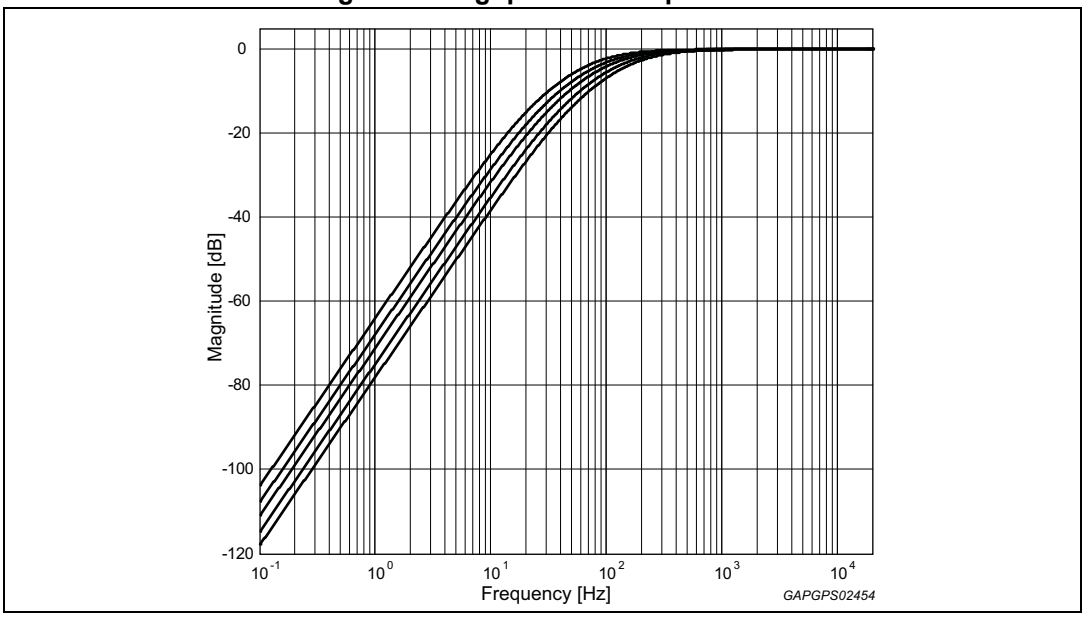
Figure 21. EQ5 quality factors @ f_c = 12.5 kHz



4.11 Highpass filter

The 2nd order high pass filter has the programmable cut-off frequencies (63/100/120/150/180Hz).

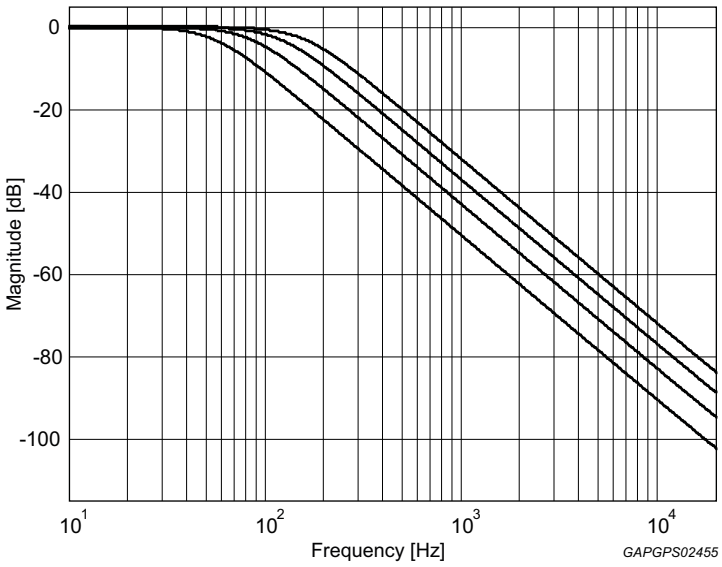
Figure 22. Highpass cut frequencies



4.12 Subwoofer filter

The subwoofer lowpass filter has Butterworth characteristics with programmable cut-off frequency (55 Hz / 85 Hz/ 120 Hz/ 160 Hz). The output phase can be selected between 0 deg and 180 deg. The input of subwoofer takes signal from EQ filter output or output of input MUX.

Figure 23. Subwoofer cut frequencies



4.13 SoftStep control

In this device, the SoftStep function is available for volume, speaker, loudness, EQ block. With SoftStep function, the audible noise of DC offset or the sudden change of signal can be avoided when adjusting gain setting of the block.

For each block, the SoftStep function is controlled by SoftStep on/off control bit in the control table. The SoftStep transient time selection (5 ms or 10 ms) is common for all blocks and it is controlled by SoftStep time control bit. The SoftStep operation of all blocks has a common centralized control. In this case, a new SoftStep operation will not be started before the completion of previous SoftStep.

There are two different modes to activate the SoftStep operation. The SoftStep operation can be started right after I^2C data sending, or the SoftStep can be activated in parallel after data sending of several different blocks. The two modes are controlled by the 'act bit' (it is normally bit7 of the byte) of each byte. When act bit is '0', which means action, the SoftStep is activated right after the date byte is sent. When the act bit is '1', which means wait, the block goes to wait for SoftStep status. In this case, the block will wait for some other block to activate the operation. The SoftStep operation of all blocks in wait status will be done together with the block which activate the SoftStep. With this mode, all specific blocks can do the SoftStep in parallel. This avoids waiting when the SoftStep is operated one by one. Be noticed that if a block is set to 'gain1' with act bit = 1, later this block is set to 'gain2' with act bit = 0, in this case the block will do a SoftStep from present gain to 'gain2' but not from present gain to 'gain1' then to 'gain2'.

Chip Addr	Sub Addr	0xxxxxxx

|← Soft-step start here

Chip Addr	Sub Addr	1xxxxxxx	1xxxxxxx	.....	0xxxxxxx

|← SoftStep start here for all

4.14 DC offset detector

Using the DC offset detection circuit (*Figure 24*) an offset voltage difference between the audio power amplifier and the APR's Front and Rear outputs can be detected, preventing serious damage to the loudspeakers. The circuit compares whether the signal crosses the zero level inside the audio power at the same time as in the speaker cell. The output of the zero-window-comparator of the power amplifier must be connected with the WinIn-input of the APR. The WinIn-input has a 50 kΩ internal pull-up resistor connected to 3.3 V. It is recommended to drive this pin with open-collector outputs only.

To compensate for errors at low frequencies the WinTC-pin is implemented, with external capacitors introducing the same delay τ = 22.5 kΩ * C_{ext} as the AC-coupling introduced between the APR and the power amplifier. For the zero window comparators, the time constant for spike rejection as well as the threshold are programmable.

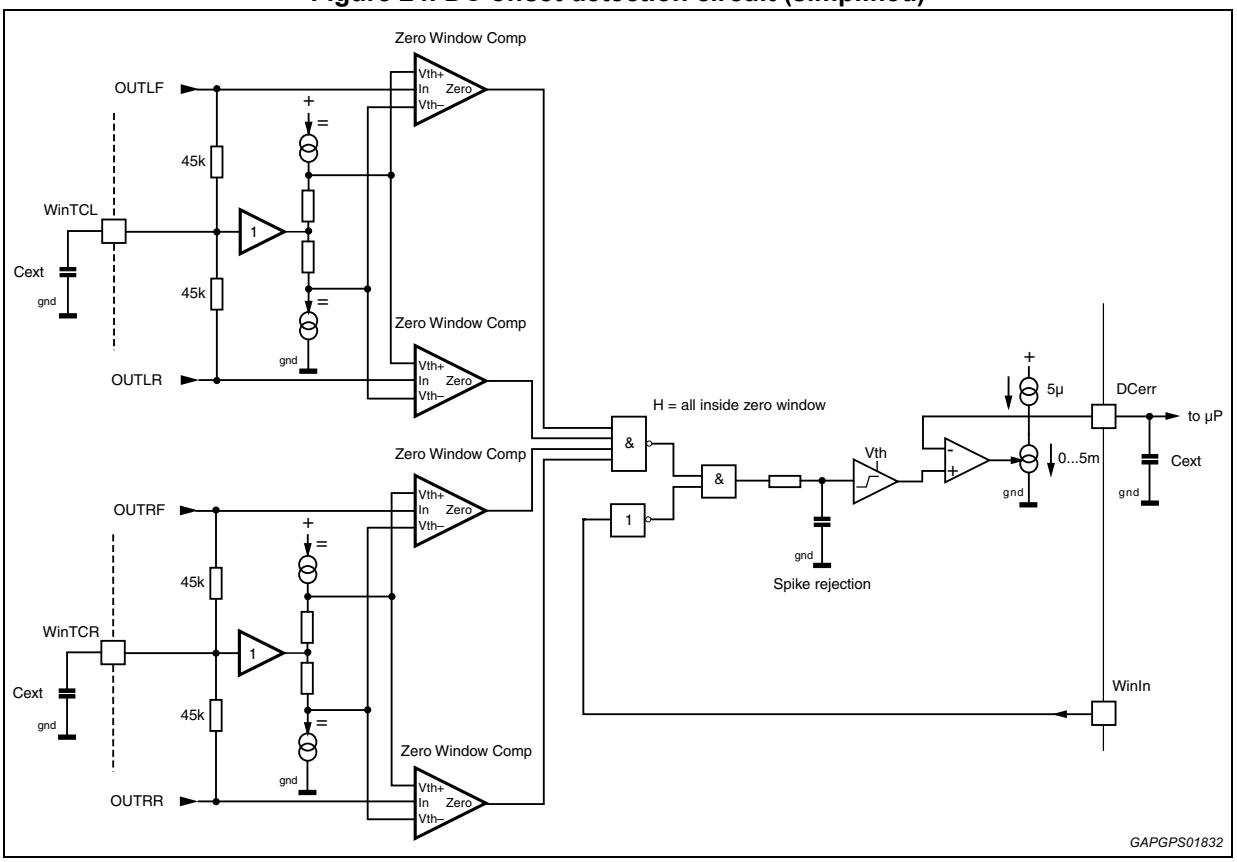
A low-active DC-offset error signal appears at the DCErr output if the next conditions are both true:

a) Front and rear outputs are inside zero crossing windows.

b) The Input voltage V_{winin} is logic low whenever at least one output of the power amplifier is outside the zero crossing windows.

After power-on, the external attached capacitor is rapidly charged (fast-charge) to overcome a false indication.

Figure 24. DC offset detection circuit (simplified)



4.15 Output stage

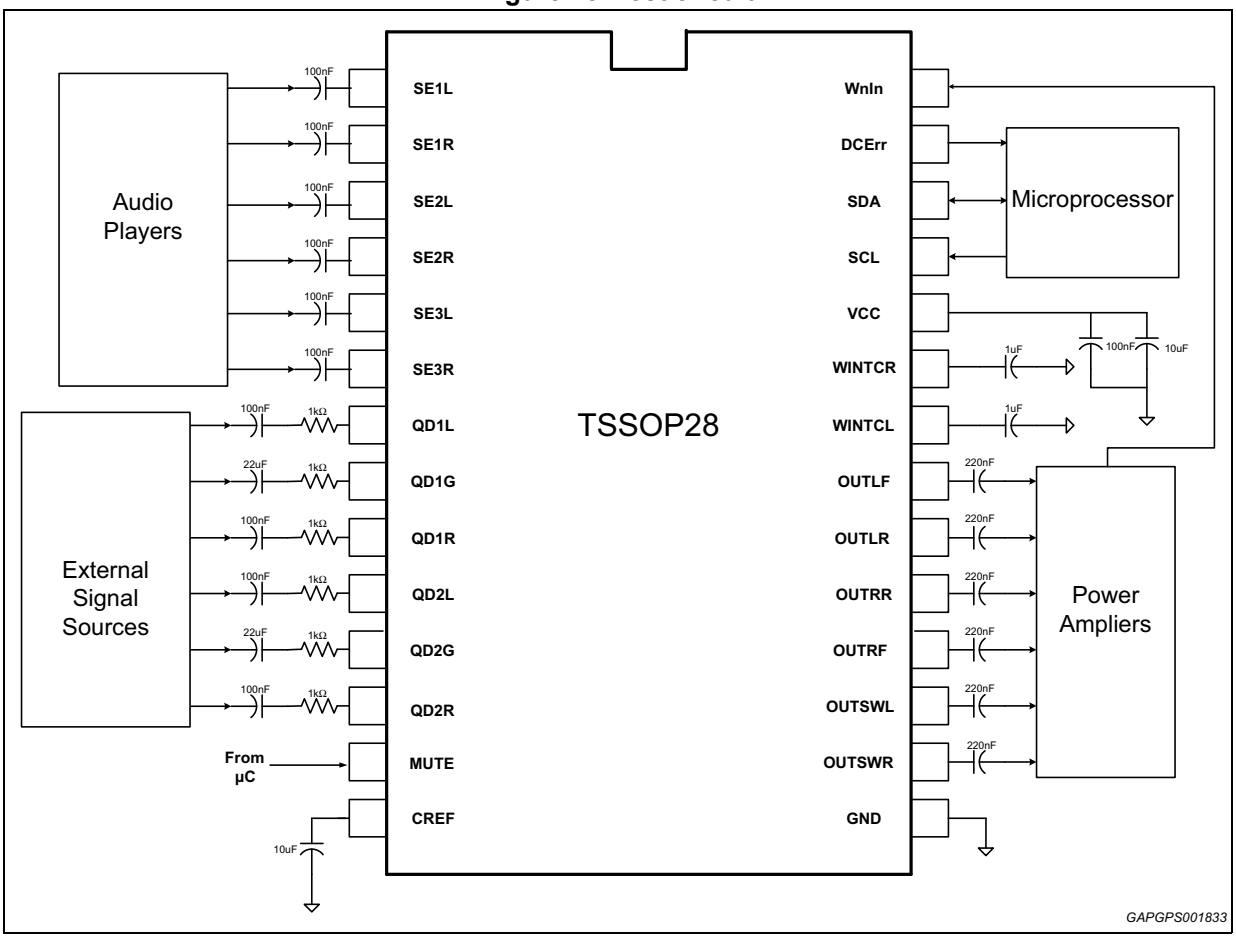
The output gain and output DC voltage are configurable by I^2C to fit different application. The configuration is as follows:

- AC Gain = 6 dB, DC level = 3 V
- AC Gain = 8.5 dB, DC level = 4 V
- AC Gain = 11 dB, DC level = 5.75 V

4.16 Audioprocessor testing

In the test mode, which can be activated by setting bit D7 of the I^2C subaddress byte and bit D0 of the testing audioprocessor byte, several internal signals are available at the QD2G pin. In this mode, the input resistance of 100 kΩ is disconnected from the pin. Internal signals available for testing are listed in the data-byte specification.

Figure 25. Test circuit



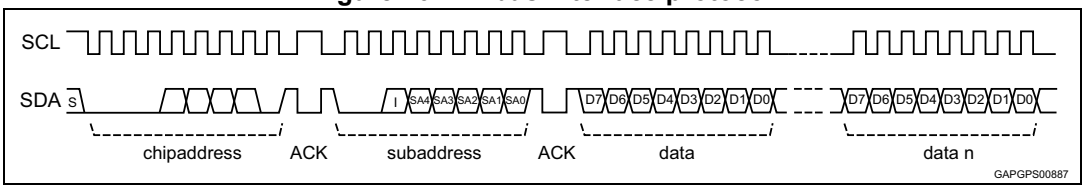
5 I²C bus specification

5.1 Interface protocol

The interface protocol comprises:

- a start condition (S)
- a chip address byte (the LSB determines read/write transmission)
- a subaddress byte
- a sequence of data (N-bytes + acknowledge)
- a stop condition (P)
- the max. clock speed is 400kbits/s
- 3.3 V logic compatible

Figure 26. I²C bus interface protocol



S = Start

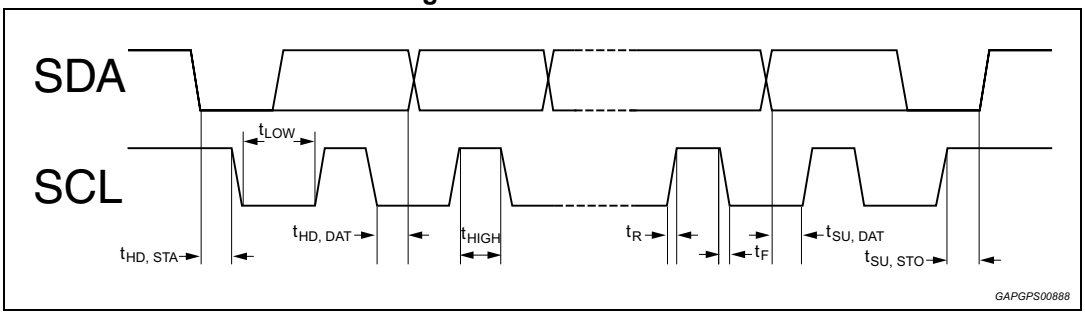
ACK = Acknowledge

5.2 I²C bus electrical characteristics

Table 6. I²C bus electrical characteristics

Symbol	Parameter	Min	Max	Unit
f_{SCL}	SCL clock frequency	-	400	kHz
V_{IH}	High level input voltage	2.4	-	V
V_{IL}	Low level input voltage	-	0.8	V
$t_{HD,STA}$	Hold time for START	0.6	-	µs
$t_{SU,STO}$	Setup time for STOP	0.6	-	µs
t_{LOW}	Low period for SCL clock	1.3	-	µs
t_{HIGH}	High period for SCL clock	0.6	-	µs
t_F	Fall time for SCL/SDA	-	300	ns
t_R	Rise time for SCL/SDA	-	300	ns
$t_{HD,DAT}$	Data hold time	0	-	ns
$t_{SU,DAT}$	Data setup time	100	-	ns

Figure 27. I²C bus data



5.2.1 Receive mode

S	1	0	0	0	1	0	0	R/W	ACK	TS	X	AI	A4	A3	A2	A1	A0	ACK	DATA	ACK	P

S = Start

R/W = "0" → Receive mode (Chip can be programmed by µP)

"1" → Transmission mode (Data could be received by µP)

ACK = Acknowledge

P = Stop

TS = Testing mode

AI = Auto increment

5.2.2 Transmission mode

S	1	0	0	0	1	0	0	R/W	ACK	X	X	X	X	X	X	BZ	SM	ACK	P

SM = SoftMute activated for main channel

BZ = SoftStep busy (‘0’ = Busy)

X = Not used

The transmitted data is automatically updated after each ACK. Transmission can be repeated without new chip address.

5.2.3 Reset condition

A power-on-reset is invoked if the supply voltage is below than 3.5 V. After that the registers are initialized to the default data written in following tables.

Table 7. Subaddress (receive mode)

MSB							LSB	Function
I2	I1	I0	A4	A3	A2	A1	A0	
0 1	-	-	-	-	-	-	-	**Testing mode** Off On
-	x	-	-	-	-	-	-	**Not used**
-	-	0 1	-	-	-	-	-	**Auto increment mode** Off On
-	-	-	0	0	0	0	0	Main selector/others
-	-	-	0	0	0	0	1	Output level / Highpass / EQ5
-	-	-	0	0	0	1	0	EQ2
-	-	-	0	0	0	1	1	EQ4
-	-	-	0	0	1	0	0	Soft-mute / others
-	-	-	0	0	1	0	1	SoftStep I
-	-	-	0	0	1	1	0	SoftStep II / DC-detector
-	-	-	0	0	1	1	1	Loudness
-	-	-	0	1	0	0	0	Volume / output gain
-	-	-	0	1	0	0	1	EQ5
-	-	-	0	1	0	1	0	EQ3
-	-	-	0	1	0	1	1	EQ1
-	-	-	0	1	1	0	0	Subwoofer / EQ3 / EQ1
-	-	-	0	1	1	0	1	Speaker attenuator left front
-	-	-	0	1	1	1	0	Speaker attenuator right front
-	-	-	0	1	1	1	1	Speaker attenuator left rear
-	-	-	1	0	0	0	0	Speaker attenuator right rear
-	-	-	1	0	0	0	1	Subwoofer attenuator left
-	-	-	1	0	0	1	0	Subwoofer attenuator right
-	-	-	1	0	0	1	1	Testing audio processor 1
-	-	-	1	0	1	0	0	Testing audio processor 2
-	-	-	1	0	1	0	1	Testing audio processor 3
-	-	-	1	0	1	1	0	InGain/EQ2/EQ4

5.3 Data byte specification

Table 8. Main selector (0)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
-	-	-	-	-				**Main source selector**
					0	0	0	SE1
					0	0	1	SE3
					0	1	0	QD1
					0	1	1	QD2
					1	0	0	SE2
					1	0	1	Mute
					1	1	0	Mute
					1	1	1	Mute
-	-	-	-		-	-	-	**EQ2 SoftStep**
				0				On
				1				Off
-	-	-		-	-	-	-	**EQ4 SoftStep**
			0					On
			1					Off
-	-		-	-	-	-	-	**Subwoofer flat**
		0						Off
		1						On
-		-	-	-	-	-	-	**Subwoofer input source**
	0							Input MUX
	1							EQ output
	-	-	-	-	-	-	-	**Rear input source**
0								Subwoofer output
1								EQ /HPF (depends on Byte1D4)

Table 9. Output level / Highpass / EQ5 (1)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
-	-	-	-	-	-			**Output DC level**
						0	0	3 V (AC Gain = 6dB)
						0	1	4 V (AC Gain = 8.5dB)
						1	x	5.75 V (AC Gain = 11dB)
-	-	-		-	-	-	-	**Highpass enable**
			0					Off (bypass)
			1					On
-	-					-	-	**Highpass frequency**
		0		0	0			100Hz
		0	-	0	1			120Hz
		0		1	0			150Hz
		0		1	1			180Hz
		1		x	x			63Hz
								EQ5 quality factor
0	0							0.75
0	1	-	-	-	-	-	-	1.0
1	0							1.25
1	1							2

Table 10. EQ2 (2)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
								Gain/Attenuation
			0	0	0	0	0	-15dB
			0	0	0	0	1	-14dB
			:	:	:	:	:	:
			0	1	1	1	0	-1dB
-	-	-	0	1	1	1	1	0dB
			1	1	1	1	1	0dB
			1	1	1	1	0	+1dB
			:	:	:	:	:	:
			1	0	0	0	1	+14dB
			1	0	0	0	0	+15dB
								EQ2 center frequency
	0	0						200Hz
-	0	1	-	-	-	-	-	250Hz
	1	0						315Hz
	1	1						400Hz
								Soft step action
0	-	-	-	-	-	-	-	act
1								wait

Table 11. EQ4 (3)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
								Gain/Attenuation
			0	0	0	0	0	-15dB
			0	0	0	0	1	-14dB
			:	:	:	:	:	:
			0	1	1	1	0	-1dB
-	-	-	0	1	1	1	1	0dB
			1	1	1	1	1	0dB
			1	1	1	1	0	+1dB
			:	:	:	:	:	:
			1	0	0	0	1	+14dB
			1	0	0	0	0	+15dB
								EQ4 center frequency
		0						2kHz
-	-	1	-	-	-	-	-	2.5kHz
		0						3.15kHz
		1						4kHz
								SoftStep action
0	-	-	-	-	-	-	-	act
1								wait

Table 12. SoftMute / others (4)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
-	-	-	-	-	-	-		**SoftMute**
							0	On
							1	Off
-	-	-	-	-	-		-	**Pin influence for mute**
						0		Pin and IIC
						1		IIC
-	-	-	-			-	-	**SoftMute Time**
				0	0			0.48ms
				0	1			0.96ms
				1	0			7.68ms
				1	1			15.36ms
-	-			-	-	-	-	**Speaker-Ls/Rs input selection (OUTSWL & OUTSWR)**
		0	0					High Pass filter
		0	1					Subwoofer filter
		1	0					High Pass filter
		1	1					EQ filter
-		-	-	-	-	-	-	**Fast charge**
	0							On
	1							Off
	-	-	-	-	-	-	-	**Anti-alias filter**
0								On
1								Off (bypass)

Table 13. SoftStep I (5)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
-	-	-	-	-	-	-	0 1	**Loudness SoftStep** On Off
-	-	-	-	-	-	0 1	-	**Volume SoftStep** On Off
-	-	-	-	-	0 1	-	-	**EQ5 SoftStep** On Off
-	-	-	-	0 1	-	-	-	**EQ3 SoftStep** On Off
-	-	-	0 1		-	-	-	**EQ1 SoftStep** On Off
-	-	0 1	-	-	-	-	-	**Speaker LF SoftStep** On Off
-	0 1	-	-	-	-	-	-	**Speaker RF SoftStep** On Off
0 1	-	-	-	-	-	-	-	**Speaker LR SoftStep** On Off

Table 14. SoftStep II / DC-detector (6)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
-	-	-	-	-	-	-	0 1	**Speaker RR SoftStep** On Off
-	-	-	-	-	-	0 1	-	**Subwoofer left SoftStep** On Off
-	-	-	-	-	0 1	-	-	**Subwoofer right SoftStep** On Off
-	-	-	-	0 1	-	-	-	**SoftStep time** 5 ms 10 ms
-	-	0 0 1 1	0 1 0 1	-	-	-	-	**Zero-comparator window size** ± 90 mV ± 60 mV ± 45 mV ± 30 mV
0 0 1 1	0 1 0 1	-	-	-	-	-	-	**Spike rejection time constant** 11µs 22 µs 33 µs 44 µs

Table 15. Loudness (7)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
-	-	-	-	0 0 : 1 1	0 0 : 1 1	0 0 : 1 1	0 1 : 0 1	**Attenuation** 0dB -1dB : -14dB -15dB
-	-	0 0 1 1	0 1 0 1	-	-	-	-	**Center frequency** Flat 400Hz 800Hz 2400Hz
-	0 1	-	-	-	-	-	-	**High boost** On Off
0 1	-	-	-	-	-	-	-	**SoftStep action** act wait

Table 16. Volume (8)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
								Gain/attenuation
	0	0	0	0	0	0	0	+0dB
	0	0	0	0	0	0	1	+1dB
	0	:	:	:	:	:	:	:
	0	0	0	1	1	1	1	+15dB
	0	0	1	0	0	0	0	+16dB
	0	:	:	:	:	:	:	:
	0	0	1	0	1	1	1	+23dB
	0	0	1	1	0	0	0	Not used
	0	:	:	:	:	:	:	:
	0	0	1	1	1	1	1	Not used
	0	1	0	0	0	0	0	-0dB
-	0	:	:	:	:	:	:	:
	0	1	0	1	1	1	1	-15dB
	0	:	:	:	:	:	:	:
	0	1	1	1	1	1	0	-30dB
	0	1	1	1	1	1	1	-31dB
	1	0	0	0	0	0	0	-32dB
	1	0	0	0	0	0	1	-33dB
	1	:	:	:	:	:	:	:
	1	0	1	1	1	1	1	-63dB
	1	1	0	0	0	0	0	-64dB
	:	:	:	:	:	:	:	:
	1	1	0	1	1	1	1	-79dB
	1	1	1	x	x	x	x	Mute
								SoftStep action
0	-	-	-	-	-	-	-	act
1								wait

Table 17. EQ5 (9)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
								Gain/attenuation
			0	0	0	0	0	-15dB
			0	0	0	0	1	-14dB
			:	:	:	:	:	:
			0	1	1	1	0	-1dB
-	-	-	0	1	1	1	1	0dB
			1	1	1	1	1	0dB
			1	1	1	1	0	+1dB
			:	:	:	:	:	:
			1	0	0	0	1	+14dB
			1	0	0	0	0	+15dB
								EQ5 center frequency
	0	0						6.3kHz
-	0	1	-	-	-	-	-	8kHz
	1	0						10.0kHz
	1	1						12.5kHz
								SoftStep action
0	-	-	-	-	-	-	-	act
1								wait

Table 18. EQ3 (10)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
								Gain/attenuation
			0	0	0	0	0	-15dB
			0	0	0	0	1	-14dB
			:	:	:	:	:	:
			0	1	1	1	0	-1dB
-	-	-	0	1	1	1	1	0dB
			1	1	1	1	1	0dB
			1	1	1	1	0	+1dB
			:	:	:	:	:	:
			1	0	0	0	1	+14dB
			1	0	0	0	0	+15dB
								EQ3 Quality factor
	0	0						0.75
-	0	1	-	-	-	-	-	1.0
	1	0						1.25
	1	1						2
								SoftStep action
0	-	-	-	-	-	-	-	act
1								wait

Table 19. EQ1 (11)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
								Gain/attenuation
			0	0	0	0	0	-15dB
			0	0	0	0	1	-14dB
			:	:	:	:	:	:
			0	1	1	1	0	-1dB
-	-		0	1	1	1	1	0dB
			1	1	1	1	1	0dB
			1	1	1	1	0	+1dB
			:	:	:	:	:	:
			1	0	0	0	1	+14dB
			1	0	0	0	0	+15dB
								EQ1 quality factor
	0	0						1.0
-	0	1	-	-	-	-	-	1.25
	1	0						1.5
	1	1						2
								SoftStep action
0	-	-	-	-	-	-	-	act
1								wait

Table 20. Subwoofer / EQ3/ EQ1 (12)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
-	-	-	-	-	-	0 0 1 1	0 1 0 1	**Subwoofer cut-off frequency** 55Hz 85Hz 120Hz 160Hz
-	-	-	-	-	0 1	-	-	**Subwoofer output phase** 180 deg 0 deg
-	-	-	0 0 1 1	0 1 0 1	-	-	-	**EQ3 Center Frequency** 630Hz 800Hz 1000Hz 1250Hz
-	0 0 1 1	0 1 0 1	-	-	-	-	-	**EQ1 Center Frequency** 63Hz 80Hz 100Hz 125Hz
0 1	-	-	-	-	-	-	-	**EQ Flat mode** on off

Table 21. Speaker attenuation (FL/FR/RL/RR/SWL/SWR) (13-18)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
-	0 0 : 0 0 0 : 1 1 1	0 0 : 0 0 0 : 0 0 1	0 0 : 0 1 1 : 1 1 x	0 0 : 1 0 0 : 1 1 x	0 0 : 1 0 0 : 1 1 x	0 0 : 1 0 0 : 1 1 x	0 1 : 1 0 1 : 0 1 x	**Gain/attenuation** +0dB +1dB : +15dB -0dB -1dB : -78dB -79dB mute
0 1	-	-	-	-	-	-	-	**SoftStep action** act wait

Table 22. Testing audio processor 1 (19)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
-	-	-	-	-	-	-	0 1	**Audio processor testing mode** Off On
-	-	-	0 0 0 0 0 0 0 0	0 0 0 0 1 1 1 1	0 0 1 1 0 0 1 1	0 1 0 1 0 1 0 1	-	**Test multiplexer at QD2G (1)** SSCLK SMCLK Clk200 SDCLK REQ_Test VDDa VDDd V2V
-	-	-	1 1 1 1 1 1 1 1	0 0 0 0 1 1 1 1	0 0 1 1 0 0 1 1	0 1 0 1 0 1 0 1	-	**Test multiplexer DCO (1)** Vref Vref Vref Vref Vthp ref Vthn ref IntZeroErr Vref
-	-	0 1	-	-	-	-	-	**Clock fast mode (2)** On Off
-	0 1	-	-	-	-	-	-	**Clock source(2)** External (MUTE Pin) Internal (200kHz)
0 1	-	-	-	-	-	-	-	**Attenuators gain clock control (2)** On Off

1. The control bit needs both I²C test mode on & sub-address test mode on.
2. The control bit does not depend on test mode.

Table 23. Testing audio processor 2 (20)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
-	-	-	-	-	-	-	0 1	**Test architecture**(1) Normal Split
-	-	-	-	-	-	0 1	-	**Oscillator clock** (2) 400kHz 800kHz
-	-	-	-	-	0 1	-	-	**SoftStep curve**(2) S-Curve Linear curve
-	-	-	0 0 1 1	0 1 0 1	-	-	-	**Manual set busy signal** (1) Auto Auto 0 1
-	-	-	0 0 1 1	0 1 0 1	-	-	-	**Request for clk generator** (1) Allow Allow Stopped Stopped
-	-	0 1	-	-	-	-	-	**No DCO spike rejection** (2) On Off
-	x	-	-	-	-	-	-	**Not used**
0 1	-	-	-	-	-	-	-	**EQ flat function** Disable Enable

1. The control bit needs sub-address test mode on.
2. The control bit does not depend on test mode.

Table 24. Testing audio processor 3 (21)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
-	-	-	-	-	-	-	0 1	**Enable Clock for FL/FR/RL/RR/SWL/SWR** On Off
-	-	-	-	-	-	0 1	-	**Enable clock for InGain&EQ1** On Off
-	-	-	-	-	0 1	-	-	**Enable clock for volume&EQ2** On Off
-	-	-	-	0 1	-	-	-	**Enable clock for EQ3** On Off
-	-	-	0 1	-	-	-	-	**Enable clock for EQ4** On Off
-	-	0 1	-	-	-	-	-	**Enable clock for EQ5** On Off
-	0 1	-	-	-	-	-	-	**Enable test for InGain** On Off
x		-	-	-	-	-	-	**Not used**

Table 25. InGain & EQ2, EQ4 (22)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
-	-	-	-	0 0 : 0 0 1	0 0 : 1 1 x	0 1 : 1 1 x	0 0 : 0 1 x	**InGain** +0dB +1dB : +6dB Not used Not used
-	-	0 0 1 1	0 1 0 1	-	-	-	-	**EQ2 quality factor** 1.0 1.25 1.5 2.0
0 0 1 1	0 1 0 1	-	-	-	-	-	-	**EQ4 quality factor** 0.75 1.0 1.25 2

6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*.

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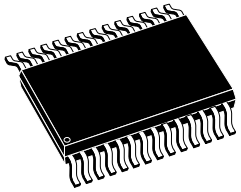
Figure 28. TSSOP28 mechanical data and package dimensions

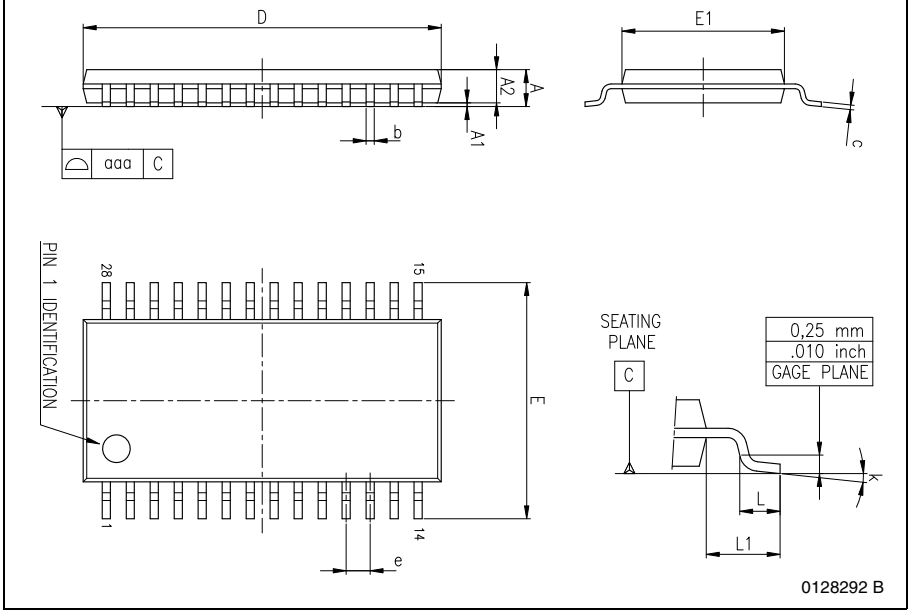
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.200			0.047
A1	0.050		0.150	0.002		0.006
A2	0.800	1.000	1.050	0.031	0.039	0.041
b	0.190		0.300	0.007		0.012
c	0.090		0.200	0.004		0.008
D (1)	9.600	9.700	9.800	0.378	0.382	0.386
E	6.200	6.400	6.600	0.244	0.252	0.260
E1 (1)	4.300	4.400	4.500	0.170	0.173	0.177
e		0.650			0.026	
L	0.450	0.600	0.750	0.018	0.024	0.030
L1		1.000			0.039	
k	0° (min.), 8° (max.)					
aaa			0.100			0.004

Note: 1. D and E1 does not include mold flash or protrusions. Mold flash or po trusions shall not exceed 0.1 5mm (.006inch) per side.

OUTLINE AND MECHANICAL DAT A



TSSOP28
Thin Shrink Small Outline Package
JEDEC MO-153-AC



GAPGPS00889

7 Revision history

Table 26. Document revision history

Date	Revision	Changes
24-Oct-2013	1	Initial release.
20-Dec-2013	2	Updated *Figure 1: Block diagram on page 6*; Modified *Table 5: Electrical characteristics* on page 11 and 12 (only C_{RANGE} parameter name).
08-Jan-2014	3	Updated *Features on page 1*.

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