AR0237CS

AR0237CS
1/2.7-inch 2.1 Mp/Full HD Digital Image Sensor

The AR0237CS from ON Semiconductor is a 1/2.7-inch CMOS digital image sensor with an active-pixel array of 1928 (H) × 1088 (V). It captures images in either linear or high dynamic range modes, with a rolling-shutter readout. It includes sophisticated camera functions such as in-pixel binning, windowing and both video and single frame modes. It is designed for both low light and high dynamic range scene performance. It is programmable through a simple two-wire serial interface. The AR0237 produces extraordinarily clear, sharp digital pictures, and its ability to capture both continuous video and single frames makes it the perfect choice for a wide range of applications, including surveillance and HD video.

Table 1. KEY PERFORMANCE PARAMETERS

Parameter	Value
Optical Format	1/2.7-inch (6.6 mm)
Active Pixels	1928 (H) × 1088 (V) (16:9 Mode)
Pixel Size	3.0 μm × 3.0 μm
Color Filter Array	RGB Bayer, RGB−IR
Shutter Type	Electronic Rolling Shutter and GRR
Input Clock Range	6–48 MHz
Output Clock Maximum	148.5 Mp/s (4-lane HiSPi) 74.25 Mp/s (Parallel)
Output Serial Parallel	 HiSPi 10-, 12-, 14-, 16-, or 20-bit 10-, 12-bit
Frame Rate 1080p	60 fps Linear HiSPi 30 fps Linear Parallel 30 fps Line Interleaved HiSPi 15 fps Line Interleaved Parallel
Responsivity	4.0 V/lux−sec
SNR_{MAX}	41 dB
Max Dynamic Range	Up to 96 dB
Supply Voltage I/O Digital Analog HiSPi	 1.8 or 2.8 V 1.8 V 2.8 V 0.3−0.6 V (SLVS), 1.7−1.9 V (HiV_{CM})
Power Consumption (Typical)	< 300 mW Line Interleaved 1080p30 < 190 mW 1080p30 Linear Mode
Operating Temperature	–30°C to +85°C Ambient
Package Options	10 × 10 mm 80-pin iBGA 11.43 × 11.43 mm 48-pin mPLCC

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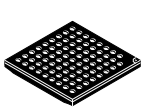
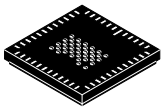
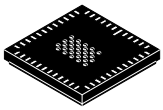


IBGA80
CASE 503BA



PLCC48
CASE 776AQ



PLCC48
CASE 776AS

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

Features

- Superior Low-light Performance
- Latest 3.0 μm pixel with ON Semiconductor DR−Pix™ Technology with Dual Conversion Gain
- Full HD Support at Up to 1080p 60 fps for Superior Video Performance
- Linear or High Dynamic Range Capture
- Supports Line Interleaved T1/T2 Readout to Enable HDR Processing in ISP Chip
- Support for External Mechanical Shutter
- On-chip Phase-locked Loop (PLL) Oscillator
- Integrated Position-based Color and Lens Shading Correction
- Slave Mode for Precise Frame-rate Control
- Stereo/3D Camera Support
- Statistics Engine
- Data Interfaces: Four-lane Serial High-speed Pixel Interface (HiSPi) Differential Signaling (SLVS and HiV_{CM}), or Parallel
- Auto Black Level Calibration
- High-speed Configurable Context Switching
- Temperature Sensor

Applications

- Video Surveillance
- 1080p60 (Surveillance) Video Applications
- High Dynamic Range Imaging

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ORDERING INFORMATION

Table 2. AVAILABLE PART NUMBERS

Part Number	Product Description	Orderable Product Attribute Description
AR0237CSSC00SUEA0−DR	2 Mp 1/2.7″ Image Sensor, RGB, 0° CRA, iBGA Package, Multi Output	Drypack
AR0237CSSC00SHRA0−DR	2 Mp 1/2.7″ Image Sensor, RGB, 0° CRA, mPLCC Package, HiSPi Output	Drypack
AR0237CSSC00SPRA0−DR	2 Mp 1/2.7″ Image Sensor, RGB, 0° CRA, mPLCC Package, Parallel Output	Drypack
AR0237CSSC12SHRA0−DR	2 Mp 1/2.7″ Image Sensor, RGB, 12° CRA, mPLCC Package, HiSPi Output	Drypack
AR0237CSSC12SPRA0−DR	2 Mp 1/2.7″ Image Sensor, RGB, 12° CRA, mPLCC Package, Parallel Output	Drypack
AR0237IRSH12SHRA0−DR−E	2 Mp 1/2.7″ Image Sensor, RGB−IR, 12° CRA, mPLCC Package, HiSPi Output	Drypack
AR0237IRSH12SPRA0−DR−E	2 Mp 1/2.7″ Image Sensor, RGB−IR, 12° CRA, mPLCC Package, Parallel Output	Drypack
AR0237CSSC00SUEAH3−GEVB	RGB, 0° CRA, iBGA Package, Multi Output, Headboard	Headboard
AR0237CSSC00SHRAH3−GEVB	RGB, 0° CRA, mPLCC Package, HiSPi Output, Headboard	Headboard
AR0237CSSC00SPRAH3−GEVB	RGB, 0° CRA, mPLCC Package, Parallel Output, Headboard	Headboard
AR0237CSSC12SHRAH3−GEVB	RGB, 12° CRA, mPLCC Package, HiSPi Output, Headboard	Headboard
AR0237CSSC12SPRAH3−GEVB	RGB, 12° CRA, mPLCC Package, Parallel Output, Headboard	Headboard
AR0237IRSH12SHRAH3−GEVB	RGB−IR, 12° CRA, mPLCC Package, HiSPi Output, Headboard	Headboard
AR0237IRSH12SPRAH3−GEVB	RGB−IR, 12° CRA, mPLCC Package, Parallel Output, Headboard	Headboard

See the ON Semiconductor Device Nomenclature document (TND310/D) for a full description of the naming convention used for image sensors. For reference documentation, including information on evaluation kits, please visit our web site at www.onsemi.com.

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GENERAL DESCRIPTION

The AR0237CS from ON Semiconductor can be operated in its default mode or programmed for frame size, exposure, gain, and other parameters. The default mode output is a 1080p-resolution image at 60 frames per second (fps) through the HiSPi port. In linear mode, it outputs 12-bit or 10-bit A−Law compressed raw data, using either the parallel or serial (HiSPi) output ports. In high dynamic range mode, it outputs two exposure values that the ISP will combine into an HDR image. The device may be operated in video (master) mode or in single frame trigger mode.

FRAME_VALID and LINE_VALID signals are output on dedicated pins, along with a synchronized pixel clock in parallel mode.

The AR0237 includes additional features to allow application-specific tuning: windowing and offset, auto black level correction, and on-board temperature sensor. Optional register information and histogram statistic information can be embedded in the first and last 2 lines of the image frame.

The AR0237CS is designed to operate over a wide temperature range of −30°C to +85°C ambient.

FUNCTIONAL OVERVIEW

The AR0237CS is a progressive-scan sensor that generates a stream of pixel data at a constant frame rate. It uses an on-chip, phase-locked loop (PLL) that can be optionally enabled to generate all internal clocks from a single master input clock running between 6 and 48 MHz. The maximum output pixel rate is 148.5 Mp/s, corresponding to a clock rate of 74.25 MHz. Figure 1 shows a block diagram of the sensor configured in linear mode, and in HDR mode.

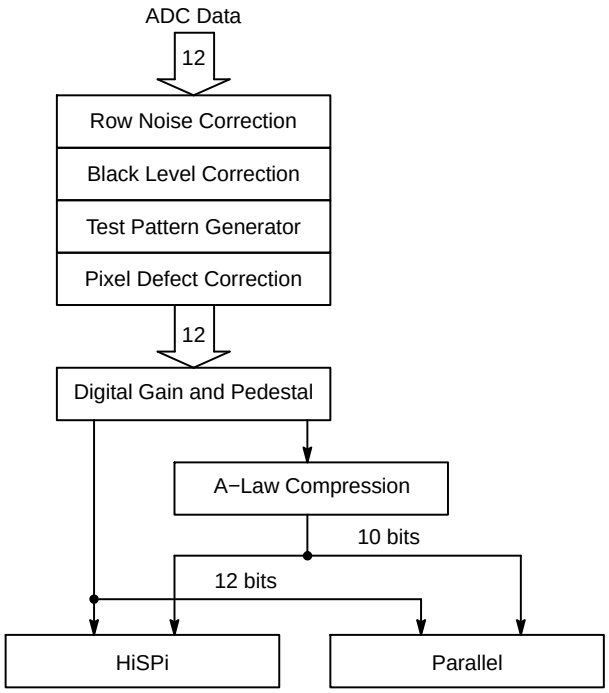

Figure 1. Block Diagram of AR0237CS

User interaction with the sensor is through the two-wire serial bus, which communicates with the array control, analog signal chain, and digital signal chain. The core of the sensor is a 2.1 Mp Active-Pixel Sensor array. The timing and control circuitry sequences through the rows of the array, resetting and then reading each row in turn. In the time interval between resetting a row and reading that row, the pixels in the row integrate incident light. The exposure is controlled by varying the time interval between reset and readout. Once a row has been read, the data from the columns is sequenced through an analog signal chain (providing offset correction and gain), and then through an analog-to-digital converter (ADC). The output from the ADC is a 12-bit value for each pixel in the array. The ADC output passes through a digital processing signal chain (which provides further data path corrections and applies digital gain). The sensor also offers a high dynamic range mode of operation where two images and taken using different exposures. These images are output in from the sensor and the ISP must combine them into one high dynamic range image.

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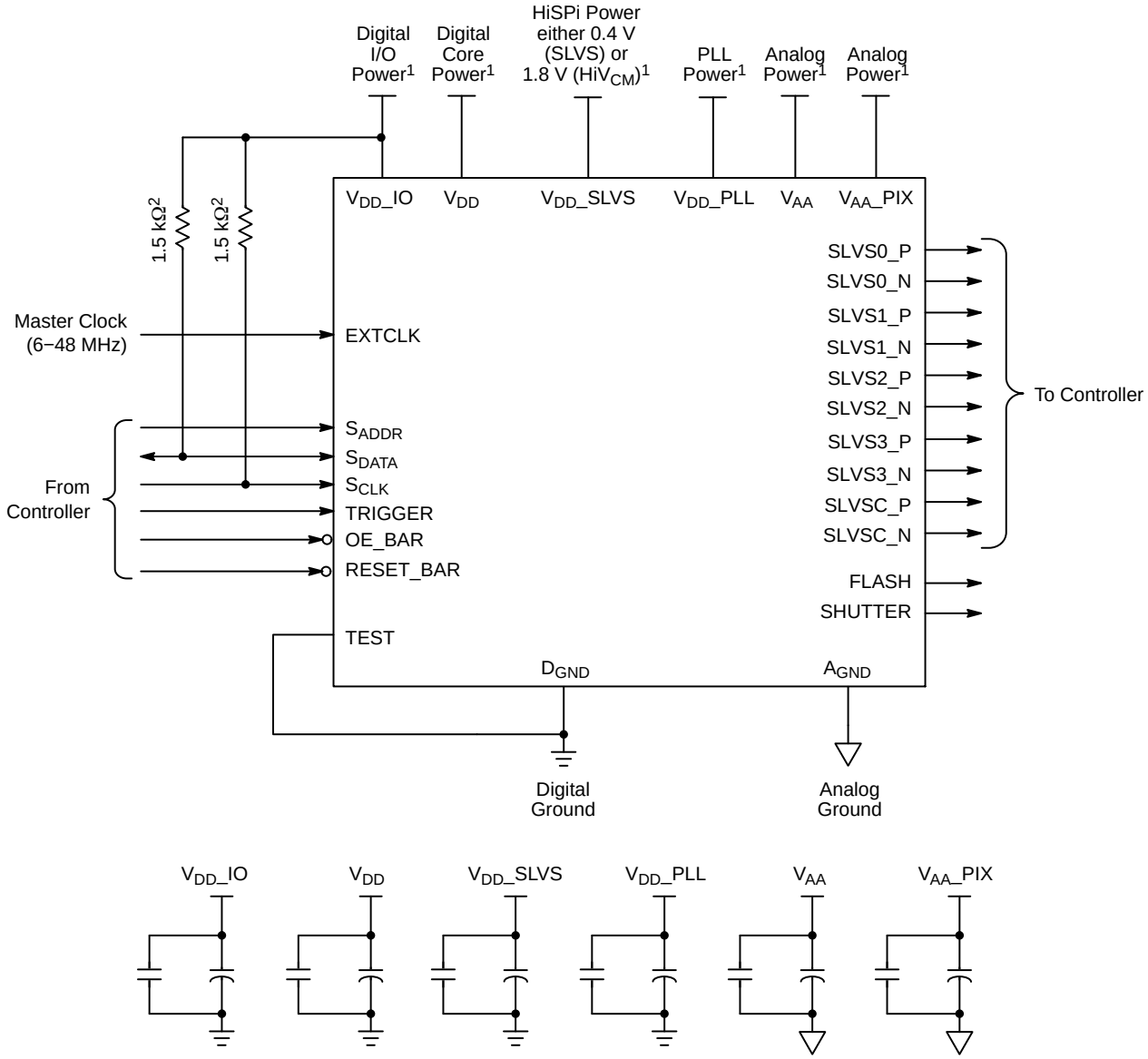
TYPICAL CONFIGURATIONS



Notes:

1. All power supplies must be adequately decoupled.
2. ON Semiconductor recommends a resistor value of 1.5 kΩ, but a greater value may be used for slower two-wire speed.
3. The parallel interface output pads can be left unconnected if the serial output interface is used.
4. ON Semiconductor recommends that 0.1 μF and 10 μF decoupling capacitors for each power supply are mounted as close as possible to the pad. Actual values and results may vary depending on the layout and design considerations. Refer to the AR0237 demo headboard schematics for circuit recommendations.
5. ON Semiconductor recommends that analog power planes are placed in a manner such that coupling with the digital power planes is minimized.
6. I/O signals voltage must be configured to match V_{DD}_IO voltage to minimize any leakage currents.

Figure 2. Serial 4-lane HiSPi Interface

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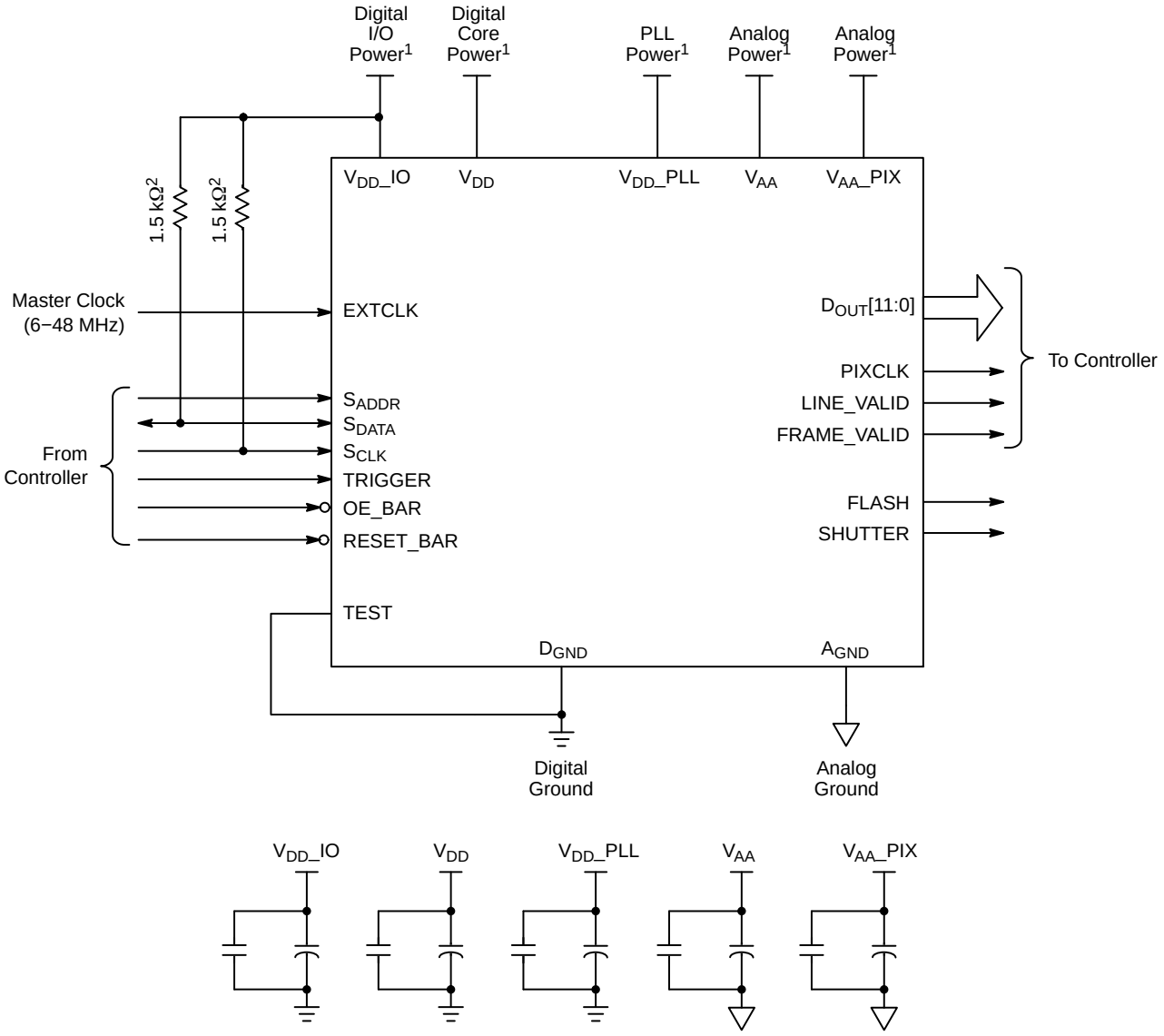

Notes:

1. All power supplies must be adequately decoupled.
2. ON Semiconductor recommends a resistor value of 1.5 kΩ, but a greater value may be used for slower two-wire speed.
3. The serial interface output pads can be left unconnected if the parallel output interface is used.
4. ON Semiconductor recommends that 0.1 μF and 10 μF decoupling capacitors for each power supply are mounted as close as possible to the pad. Actual values and results may vary depending on the layout and design considerations. Refer to the AR0237 demo headboard schematics for circuit recommendations.
5. ON Semiconductor recommends that analog power planes are placed in a manner such that coupling with the digital power planes is minimized.
6. I/O signals voltage must be configured to match V_{DD}_IO voltage to minimize any leakage currents.
7. The EXTCLK input is limited to 6−48 MHz.

Figure 3. Parallel Pixel Data Interface

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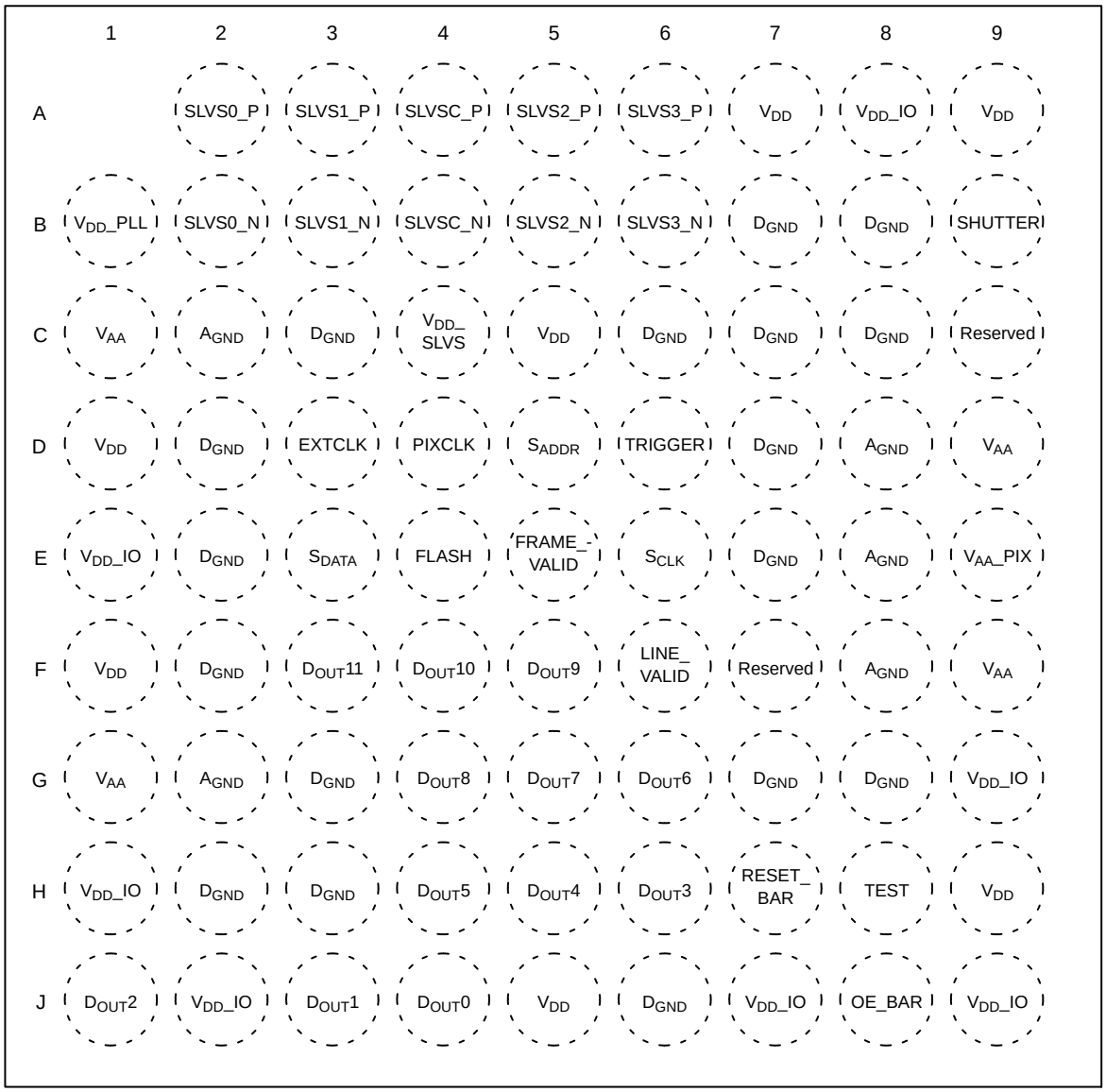
PIN DESCRIPTIONS



Top View
(Ball Down)

Figure 4. 80-ball iBGA Package

Table 3. PIN DESCRIPTIONS, 80-BALL IBGA

Name	iBGA Pin	Type	Description
SLVS0_P	A2	Output	HiSPi serial data, lane 0, differential P
SLVS1_P	A3	Output	HiSPi serial data, lane 1, differential P
SLVSC_P	A4	Output	HiSPi serial DDR clock differential P
SLVS2_P	A5	Output	HiSPi serial data, lane 2, differential P
SLVS3_P	A6	Output	HiSPi serial data, lane 3, differential P
V_{DD}_PLL	B1	Power	PLL power
SLVS0_N	B2	Output	HiSPi serial data, lane 0, differential N

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Table 3. PIN DESCRIPTIONS, 80-BALL IBGA (continued)

Name	iBGA Pin	Type	Description
SLVS1_N	B3	Output	HiSPi serial data, lane 1, differential N
SLVSC_N	B4	Output	HiSPi serial DDR clock differential N
SLVS2_N	B5	Output	HiSPi serial data, lane 2, differential N
SLVS3_N	B6	Output	HiSPi serial data, lane 3, differential N
SHUTTER	B9	Output	Control for external mechanical shutter. Can be left floating if not used
V_{AA}	C1, G1, D9, F9	Power	Analog power
A_{GND}	C2, G2, D8, E8, F8	Power	Analog ground
V_{DD}_SLVS	C4	Power	SLVS power 0.4 V/1.8 V depending on how R0x306E[9] is set. 0 = 0.4 V; 1 = 1.8 V
V_{DD}	C5, J5, A9, H9, A7, D1, F1	Power	Digital power
Reserved	C9, F7		
D_{GND}	B7, C7, D7, E7, G7, B8, C8, G8, D2, E2, F2, H2, C3, G3, H3, C6, J6	Power	Digital ground
EXTCLK	D3	Input	External input clock
PIXCLK	D4	Output	Pixel clock out. D_{OUT} is valid on rising edge of this clock
S_{ADDR}	D5	Input	Two-wire Serial address select. 0: 0x20. 1: 0x30
TRIGGER	D6	Input	Exposure synchronization input
V_{AA}_PIX	E9	Power	Pixel power
V_{DD}_IO	E1, H1, J2, J7, A8, G9, J9	Power	I/O supply power
S_{DATA}	E3	I/O	Two-wire Serial data I/O
FLASH	E4	Output	Flash control output
FRAME_VALID	E5	Output	Asserted when D_{OUT} frame data is valid
S_{CLK}	E6	Input	Two-wire Serial clock input
D_{OUT}11	F3	Output	Parallel pixel data output (MSB)
D_{OUT}10	F4	Output	Parallel pixel data output
D_{OUT}9	F5	Output	Parallel pixel data output
LINE_VALID	F6	Output	Asserted when D_{OUT} line data is valid
D_{OUT}8	G4	Output	Parallel pixel data output
D_{OUT}7	G5	Output	Parallel pixel data output
D_{OUT}6	G6	Output	Parallel pixel data output
D_{OUT}5	H4	Output	Parallel pixel data output
D_{OUT}4	H5	Output	Parallel pixel data output
D_{OUT}3	H6	Output	Parallel pixel data output
RESET_BAR	H7	Input	Asynchronous reset (active LOW). All settings are restored to factory default
TEST	H8	Input	Manufacturing test enable pin (connect to D_{GND})
D_{OUT}2	J1	Output	Parallel pixel data output
D_{OUT}1	J3	Output	Parallel pixel data output
D_{OUT}0	J4	Output	Parallel pixel data output (LSB)
OE_BAR	J8	Input	Output enable (active LOW)

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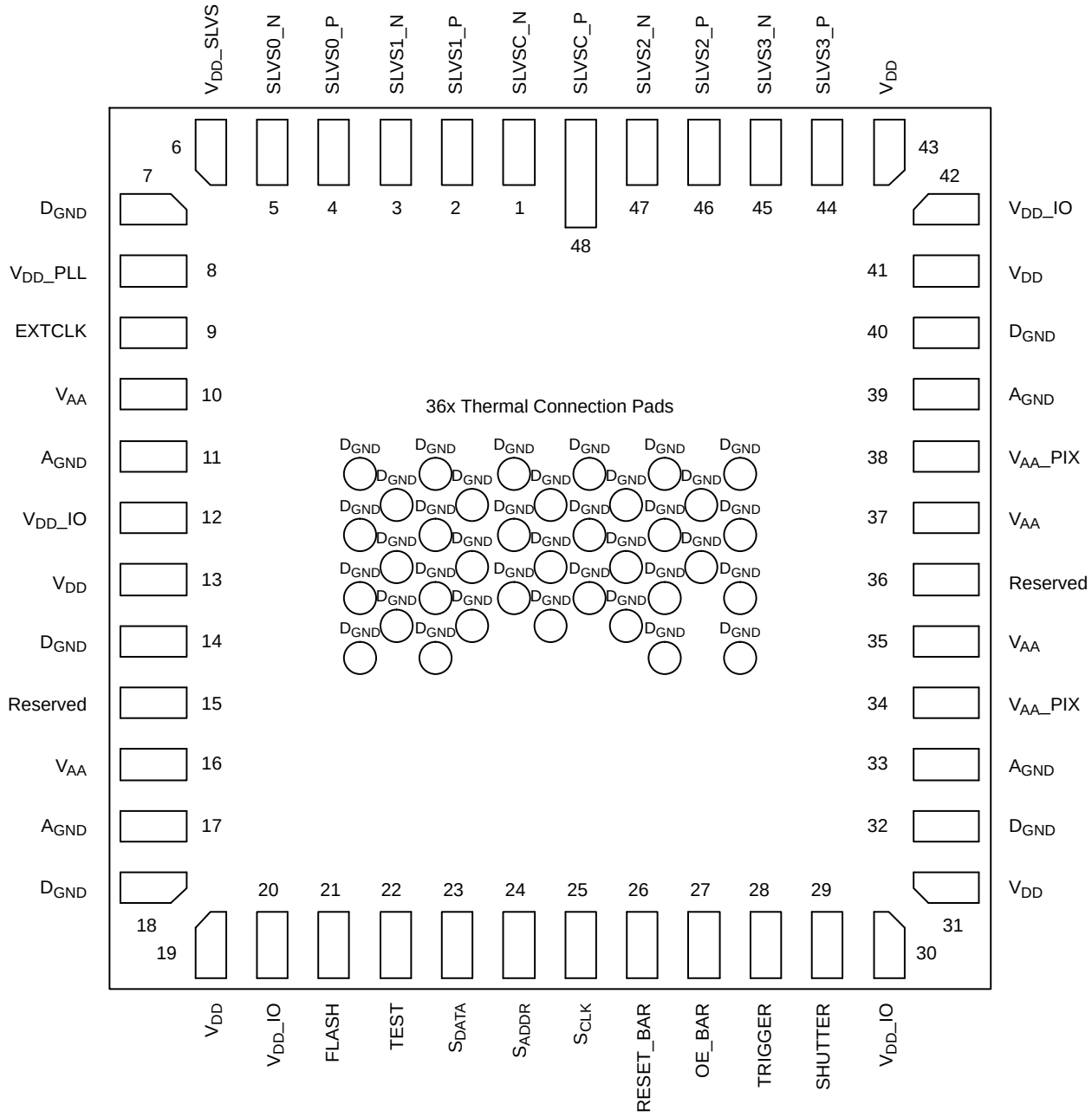

Figure 5. 48-pin mPLCC Package HiSPi (Top Side View)

Table 4. PIN DESCRIPTIONS, 48-PIN MPLCC HISPI

Pin	Name	Type	Description
1	SLVSC_N	Output	HiSPi serial DDR clock differential N
2	SLVS1_P	Output	HiSPi serial data, lane 1, differential P
3	SLVS1_N	Output	HiSPi serial data, lane 1, differential N
4	SLVS0_P	Output	HiSPi serial data, lane 0, differential P
5	SLVS0_N	Output	HiSPi serial data, lane 0, differential N
6	V_{DD}_SLVS	Power	SLVS Power 0.4 V/1.8 V depending on how R0x306E[9] is set. 0 = 0.4 V; 1 = 1.8 V
7	D_{GND}	Power	Digital ground

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Table 4. PIN DESCRIPTIONS, 48-PIN MPLCC HISPI (continued)

Pin	Name	Type	Description
8	V_{DD}_PLL	Power	PLL power
9	EXTCLK	Input	External input clock
10	V_{AA}	Power	Analog Power
11	A_{GND}	Power	Analog Ground
12	V_{DD}_IO	Power	I/O Power Supply
13	V_{DD}	Power	Digital Power
14	D_{GND}	Power	Digital ground
15	Reserved		
16	V_{AA}	Power	Analog Power
17	A_{GND}	Power	Analog Ground
18	D_{GND}	Power	Digital ground
19	V_{DD}	Power	Digital Power
20	V_{DD}_IO	Power	I/O Power Supply
21	FLASH	Output	Flash control output
22	TEST	Input	Manufacturing test enable pin (connect to D_{GND})
23	S_{DATA}	I/O	Two-wire Serial data I/O
24	S_{ADDR}	Input	Two-wire Serial address select. 0: 0x20, 1: 0x30
25	S_{CLK}	Input	Two-wire Serial clock input
26	RESET_BAR	Input	Asynchronous reset (active LOW). All settings are restored to factory default
27	OE_BAR	Input	Output enable (active LOW)
28	TRIGGER	Input	Exposure synchronization input
29	SHUTTER	Output	Control for external mechanical shutter. Can be left floating if not used.
30	V_{DD}_IO	Power	I/O Power Supply
31	V_{DD}	Power	Digital Power
32	D_{GND}	Power	Digital ground
33	A_{GND}	Power	Analog Ground
34	V_{AA}_PIX	Power	Pixel Power
35	V_{AA}	Power	Analog Power
36	Reserved		
37	V_{AA}	Power	Analog Power
38	V_{AA}_PIX	Power	Pixel Power
39	A_{GND}	Power	Analog Ground
40	D_{GND}	Power	Digital ground
41	V_{DD}	Power	Digital Power
42	V_{DD}_IO	Power	I/O Power Supply
43	V_{DD}	Power	Digital Power
44	SLSV3_P	Output	HiSPi serial data, lane 3, differential P
45	SLVS3_N	Output	HiSPi serial data, lane 3, differential N
46	SLVS2_P	Output	HiSPi serial data, lane 2, differential P
47	SLVS2_N	Output	HiSPi serial data, lane 2, differential N
48	SLVSLC_P	Output	HiSPi serial DDR clock differential P

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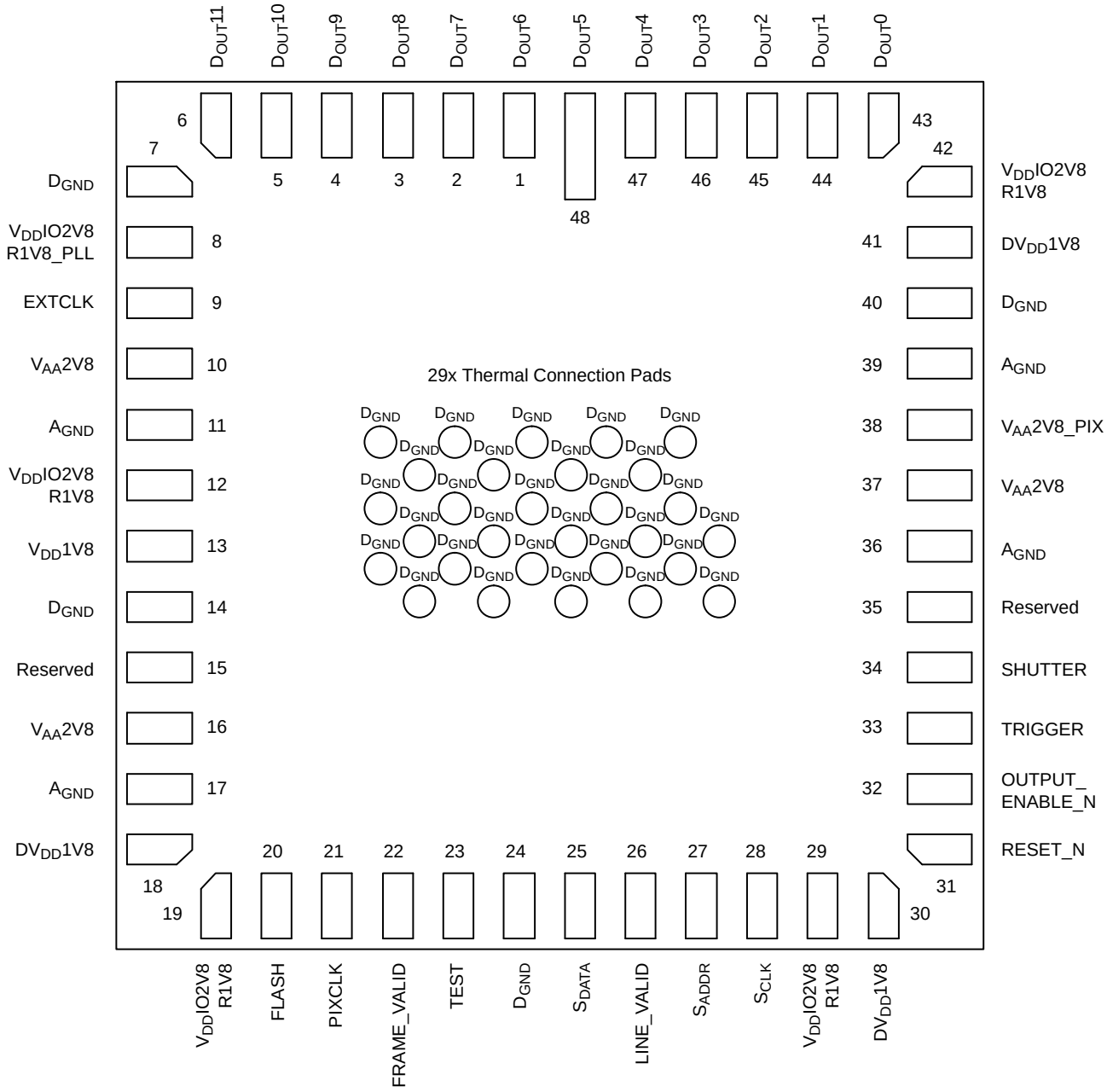

Figure 6. 48-pin mPLCC Package Parallel (Top Side View)

Table 5. PIN DESCRIPTIONS, 48-PIN MPLCC HISPI

Pin	Name	Type	Description
1	$D_{OUT}6$	Output	Data output 6
2	$D_{OUT}7$	Output	Data output 7
3	$D_{OUT}8$	Output	Data output 8
4	$D_{OUT}9$	Output	Data output 9
5	$D_{OUT}10$	Output	Data output 10
6	$D_{OUT}11$	Power	Data output 11
7	D_{GND}	Power	Digital ground
8	V_{DD}_PLL	Power	PLL power

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Table 5. PIN DESCRIPTIONS, 48-PIN MPLCC HISPI (continued)

Pin	Name	Type	Description
9	EXTCLK	Input	External input clock
10	V_{AA}	Power	Analog Power
11	A_{GND}	Power	Analog Ground
12	V_{DD}_IO	Power	I/O Power Supply
13	V_{DD}	Power	Digital Power
14	D_{GND}	Power	Digital ground
15	Reserved		
16	V_{AA}	Power	Analog Power
17	A_{GND}	Power	Analog Ground
18	V_{DD}	Power	Digital Power
19	V_{DD}_IO	Power	I/O Power Supply
20	FLASH	Power	Flash control output
21	PIXCLK	Output	Pixel Clock
22	FRAME_VALID	Output	Frame Valid
23	TEST	Input	Manufacturing test enable pin (connect to D_{GND})
24	D_{GND}	Power	Digital Ground
25	S_{DATA}	I/O	Two-wire Serial data I/O
26	LINE_VALID	Output	Line Valid
27	S_{ADDR}	Input	Two-wire Serial address select. 0: 0x20, 1: 0x30
28	S_{CLK}	Input	Two-wire Serial clock input
29	V_{DD}_IO	Power	I/O Power Supply
30	V_{DD}	Power	Digital Power
31	RESET_BAR	Input	Asynchronous reset (active LOW). All settings are restored to factory default
32	OE_BAR	Input	Output enable (active LOW)
33	TRIGGER	Input	Exposure synchronization input
34	SHUTTER	Output	Control for external mechanical shutter. Can be left floating if not used.
35	Reserved	Input	
36	A_{GND}	Power	Analog Ground
37	V_{AA}_2V8	Power	Analog Power
38	V_{AA}_PIX	Power	Pixel Power
39	A_{GND}	Power	Analog Ground
40	D_{GND}	Power	Digital ground
41	V_{DD}	Power	Digital Power
42	V_{DD}_IO	Power	I/O Power Supply
43	D_{OUT}0	Output	Data Output 0
44	D_{OUT}1	Output	Data Output 1
45	D_{OUT}2	Output	Data Output 2
46	D_{OUT}3	Output	Data Output 3
47	D_{OUT}4	Output	Data Output 4
48	D_{OUT}5	Output	Data Output 5

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PIXEL DATA FORMAT

Pixel Array Structure

While the sensor's format is 1928×1088, additional active columns and active rows are included for use when horizontal or vertical mirrored readout is enabled, to allow readout to start on the same pixel. The pixel adjustment is always performed for monochrome or color versions. The active area is surrounded with optically transparent dummy pixels to improve image uniformity within the active area. Not all dummy pixels or barrier pixels can be read out.

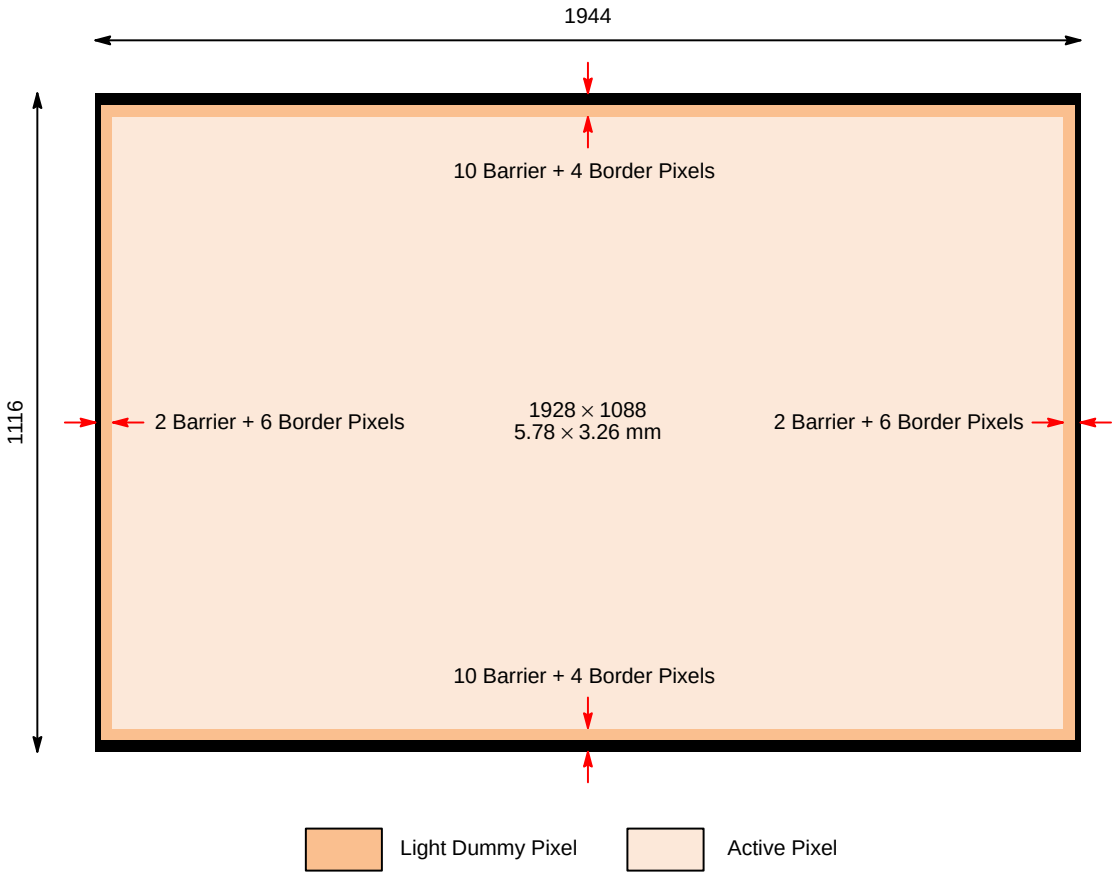

Figure 7. Pixel Array Description

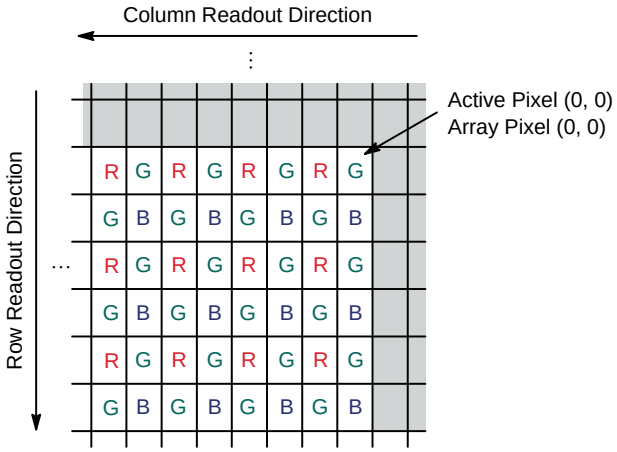

Figure 8. Pixel Color Pattern Detail (RGB) (Top Right Corner)

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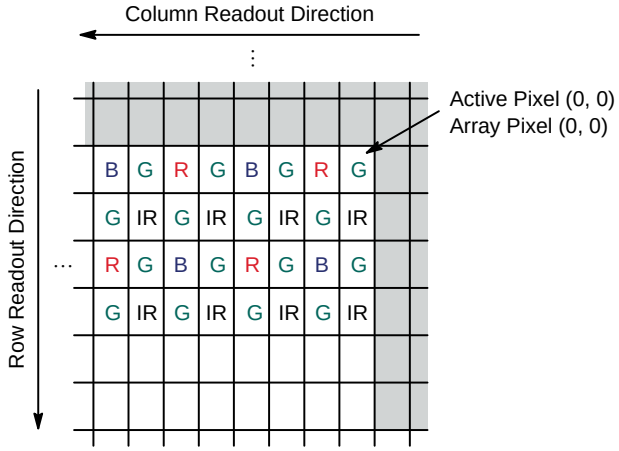

Figure 9. Pixel Color Pattern Detail (RGB−IR) (Top Right Corner)

Default Readout Order

By convention, the sensor core pixel array is shown with pixel (0,0) in the top right corner (see Figure 8). This reflects the actual layout of the array on the die. Also, the first pixel data read out of the sensor in default condition is that of pixel (10, 14).

When the sensor is imaging, the active surface of the sensor faces the scene as shown in Figure 10. When the image is read out of the sensor, it is read one row at a time, with the rows and columns sequenced as shown in Figure 10.

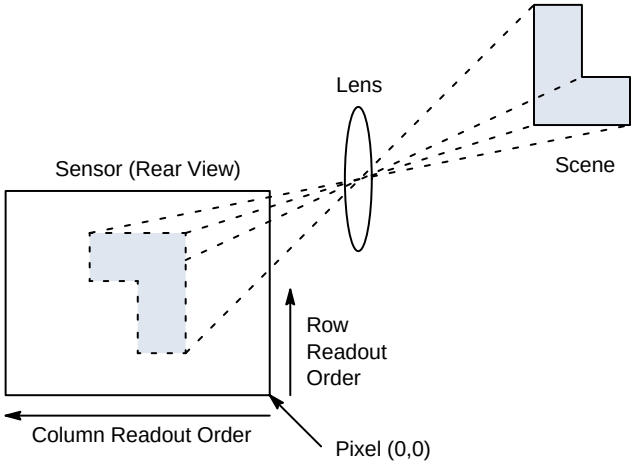

Figure 10. Imaging a Scene

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FEATURES OVERVIEW

For a complete description, recommendations, and usage guidelines for product features, refer to the AR0237 Developer Guide.

3.0 μm Dual Conversion Gain Pixel

To improve the low light performance and keep the high dynamic range, a large (3.0 μm) dual conversion gain pixel is implemented for better image optimization. With a dual conversion gain pixel, the conversion gain of the pixel may be dynamically changed to better adapt the pixel response based on dynamic range of the scene.

HDR

By default, the sensor powers up in Linear Mode. One can change to HDR Mode. The HDR scheme used is multi-exposure HDR. This allows the sensor to handle up to 96 dB of dynamic range. In HDR mode, the sensor sequentially captures two exposures by maintaining two separate read and reset pointers that are interleaved within the rolling shutter readout. The exposure ratio may be set to 4×, 8×, 16×, or 32×. Sensor also provides flexibility to choose any exposure ratio by setting number of t_2 exposure rows independent of the t1 exposure. The data will be output as line interleaved data as described in the T1/T2 Line Interleaved Mode section. There is also an option to output either T1 only or T2 only.

Resolution

The active array supports a maximum of 1928×1088 pixels to support 1080p resolution. Utilizing a 3.0um pixel will result in an optical format of 1/2.7-inch (approximately 6.6 mm diagonal).

Frame Rate

At full (1080p) resolution, the AR0237 is capable of running up to 60 fps in linear mode and 30 fps in line interleaved mode.

Image Acquisition Mode

The AR0237 supports two image acquisition modes:

- Electronic Rolling Shutter (ERS) Mode:
  This is the normal mode of operation. When the AR0237 is streaming, it generates frames at a fixed rate, and each frame is integrated (exposed) using the ERS. When ERS mode is in use, timing and control logic within the sensor sequences through the rows of the array, resetting and then reading each row in turn. In the time interval between resetting a row and subsequently reading that row, the pixels in the row integrate incident light. The integration (exposure) time is controlled by varying the time between row reset and row readout. For each row in a frame, the time between row reset and row readout is the same, leading to a uniform integration time across the frame. When the integration time is changed (by using the two-wire serial interface to change register settings), the timing and control logic controls the transition from old to new integration time in such a way that the stream of output frames from the AR0237 switches cleanly from the old integration time to the new while only generating frames with uniform integration. See “Changes to Integration Time” in the AR0237 Register Reference.
- Global Reset Mode:
  This mode can be used to acquire a single image at the current resolution. In this mode, the end point of the pixel integration time is controlled by an external electromechanical shutter, and the AR0237 provides control signals to interface to that shutter. The benefit of using an external electromechanical shutter is that it eliminates the visual artifacts associated with ERS operation. Visual artifacts arise in ERS operation, particularly at low frame rates, because an ERS image effectively integrates each row of the pixel array at a different point in time.

Embedded Data and Statistics

The AR0237 has the capability to output image data and statistics embedded within the frame timing. There are two types of information embedded within the frame readout.

- Embedded Data:
  If enabled, these are displayed on the two rows immediately before the first active pixel row is displayed.
- Embedded Statistics:
  If enabled, these are displayed on the two rows immediately after the last active pixel row is displayed.

Multi-Camera Synchronization

The AR0237 supports advanced line synchronization controls for multi-camera (stereo) support.

Slave Mode

The slave mode feature of the AR0237 supports triggering the start of a frame readout from an input signal that is supplied from an external ASIC. The slave mode signal allows for precise control of frame rate and register change updates.

Context Switching and Register Updates

The user has the option of using the highly configurable context memory, or a simplified implementation in which only a subset of registers is available for switching. The AR0237 supports a highly configurable context switching RAM of size 256×16. Within this Context Memory, changes to any register may be stored. The register set for each context must be the same, but the number of contexts and registers per context are limited only by the size of the context memory.

Alternatively, the user may switch between two predefined register sets A and B by writing to a context switch change bit. When the context switch is configured to

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context A the sensor will reference the context A registers. If the context switch is changed from A to B during the readout of frame n, the sensor will then reference the context B coarse_integration_time registers in frame n+1 and all other context B registers at the beginning of reading frame n+2. The sensor will show the same behavior when changing from context B to context A. The registers listed in Table 6 are context-switchable:

Table 6. LIST OF CONFIGURABLE RESISTORS FOR CONTEXT A AND CONTEXT B

Context A Register Description	Context B Register Description
coarse_integration_time	coarse_integration_time_cb
line_length_pck	line_length_pck_cb
frame_length_lines	frame_length_lines_cb
row_bin	row_bin_cb
col_bin	col_bin_cb
fine_gain	fine_gain_cb
coarse_gain	coarse_gain_cb
coarse_integration_time2	coarse_integration_time2_cb
dcg_manual_set	dcg_manual_set_cb
dcg_manual_set_t1	dcg_manual_set_t1_cb
bypass_pix_comb	bypass_pix_cb
coarse_gain_t1	coarse_gain_t1_cb
fine_gain_t1	fine_gain_t1_cb
x_addr_start	x_addr_start_cb
y_addr_start	y_addr_start_cb
x_addr_end	x_addr_end_cb
y_addr_end	y_addr_end_cb
y_odd_inc	y_odd_inc_cb
x_odd_inc	x_odd_inc_cb
green1_gain	green1_gain_cb
blue_gain	blue_gain_cb
red_gain	red_gain_cb
green2_gain	green2_gain_cb
global_gain	global_gain_cb
operation_mode_ctrl	operation_mode_ctrl_cb
bypass_pix_comb	bypass_pix_comb_cb

Analog/Digital Gains

A programmable analog gain of 1.0× to 16× (linear and HDR) applied simultaneously to all color channels will be featured along with a digital gain of 1× to 16× that may be configured on a per color channel basis. Note that with the RGB IR sensor digital gain should only be applied to all color channels equally since with the 4 × 4 kernel the gains will not be applied to the proper color channel. Analog gain can be applied per exposure in line interleaved mode.

Skipping/Binning Modes

The AR0237 supports subsampling. Subsampling allows the sensor to read out a smaller set of active pixels by either skipping, binning, or summing pixels within the readout window. Horizontal binning is achieved in the digital readout. The sensor will sample the combined 2× adjacent pixels within the same color plane. Vertical row binning is applied in the pixel readout. Row binning can be configured as 2× rows within the same color plane. Pixel skipping can be configured up to 2× in both the x-direction and y-direction. Skipping pixels in the x-direction will not reduce the row time. Skipping pixels in the y direction will reduce the number of rows from the sensor effectively reducing the frame time. Skipping will introduce image artifacts from aliasing.

The AR0237 supports row wise vertical binning. Row wise vertical summing is only supported in monochrome sensors.

Binning and summing is not supported with RGB IR sensors.

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Clocking Options

The sensor contains a phase-locked loop (PLL) that is used for timing generation and control. The required VCO clock frequency is attained through the use of a pre-PLL clock divider followed by a multiplier. The PLL multiplier should be an even integer. If an odd integer (M) is programmed, the PLL will default to the lower (M−1) value to maintain an even multiplier value. The multiplier is followed by a set of dividers used to generate the output clocks required for the sensor array, the pixel analog and digital readout paths, and the output parallel and serial interfaces. Use of the PLL is required when using the HiSPi interface.

Temperature Sensor

The AR0237 sensor has a built-in PTAT-based temperature sensor, accessible through registers, that is capable of measuring die junction temperature. The value read out from the temperature sensor register is an ADC output value that needs to be converted downstream to a final temperature value in degrees Celsius. Since the PTAT device characteristic response is quite linear in the temperature range of operation required, a simple linear function can be used to convert the ADC output value to the final temperature in degrees Celsius.

A single reference point will be made available via register read as well as a slope for back-calculating the junction temperature value. An error of ±5% or better over the full specified operating range of the sensor is to be expected.

Silicon/Firmware/Sequencer Revision Information

A revision register will be provided to read out (via I^2C) silicon and sequencer/OTPM revision information. This will be helpful to distinguish among different lots of material if there are future OTPM or sequencer revisions.

Lens Shading Correction

The latest lens shading correction algorithm will be included for potential low Z height applications.

Compression

When the AR0237 is configured for linear mode operation, the sensor can optionally compress 12-bit data to 10-bit using A−law compression. The A−law compression is disabled by default.

Packaging

The AR0237 will be offered in a 10×10 80-iBGA package (parallel and HiSPi) and a 11.43×1143 48 pin mPLCC (HiSSPi) package.

Parallel Interface

The parallel pixel data interface uses these output−only signals:

- FRAME_VALID
- LINE_VALID
- PIXCLK
- D_{OUT}[11:0]

The parallel pixel data interface is disabled by default at power up and after reset. It can be enabled by programming R0x301A. When the parallel pixel data interface is in use, the serial data output signals can be left unconnected.

High Speed Serial Pixel (HiSPi) Interface

The HiSPi interface supports three protocols, Streaming−S, Streaming−SP, and Packetized SP. The streaming protocols conform to a standard video application where each line of active or intra-frame blanking provided by the sensor is transmitted at the same length. The Packetized SP protocol will transmit only the active data ignoring line-to-line and frame-to-frame blanking data.

The HiSPi interface building block is a unidirectional differential serial interface with four data and one double data rate (DDR) clock lanes. One clock for every four serial data lanes is provided for phase alignment across multiple lanes. The AR0237 supports serial data widths of 10 or 12 bits on one, two, or four lanes. The specification includes a DLL to compensate for differences in group delay for each data lane. The DLL is connected to the clock lane and each data lane, which acts as a control master for the output delay buffers. Once the DLL has gained phase lock, each lane can be delayed in 1/8 unit interval (UI) steps. This additional delay allows the user to increase the setup or hold time at the receiver circuits and can be used to compensate for skew introduced in PCB design. Delay compensation may be set for clock and/or data lines in the hispi_timing register R0x31C0. If the DLL timing adjustment is not required, the data and clock lane delay settings should be set to a default code of 0x0000 to reduce jitter, skew, and power dissipation.

Sensor Control Interface

The two-wire serial interface bus enables read/write access to control and status registers within the AR0237. The interface protocol uses a master/slave model in which a master controls one or more slave devices. The sensor acts as a slave device. The master generates a clock (S_{CLK}) that is an input to the sensor and is used to synchronize transfers.

Data is transferred between the master and the slave on a bidirectional signal (S_{DATA}). S_{DATA} is pulled up to V_{DD}_IO off-chip by a 1.5 kΩ resistor. Either the slave or master device can drive S_{DATA} LOW − the interface protocol determines which device is allowed to drive S_{DATA} at any given time. The two-wire serial interface can run at 100 kHz or 400 kHz.

T1/T2 Line Interleaved Mode

The AR0237 outputs the T1 and T2 exposures separately, in a line interleaved format. The purpose of this is to enable off chip HDR linear combination and processing. See the AR0237 Developer Guide for more information.

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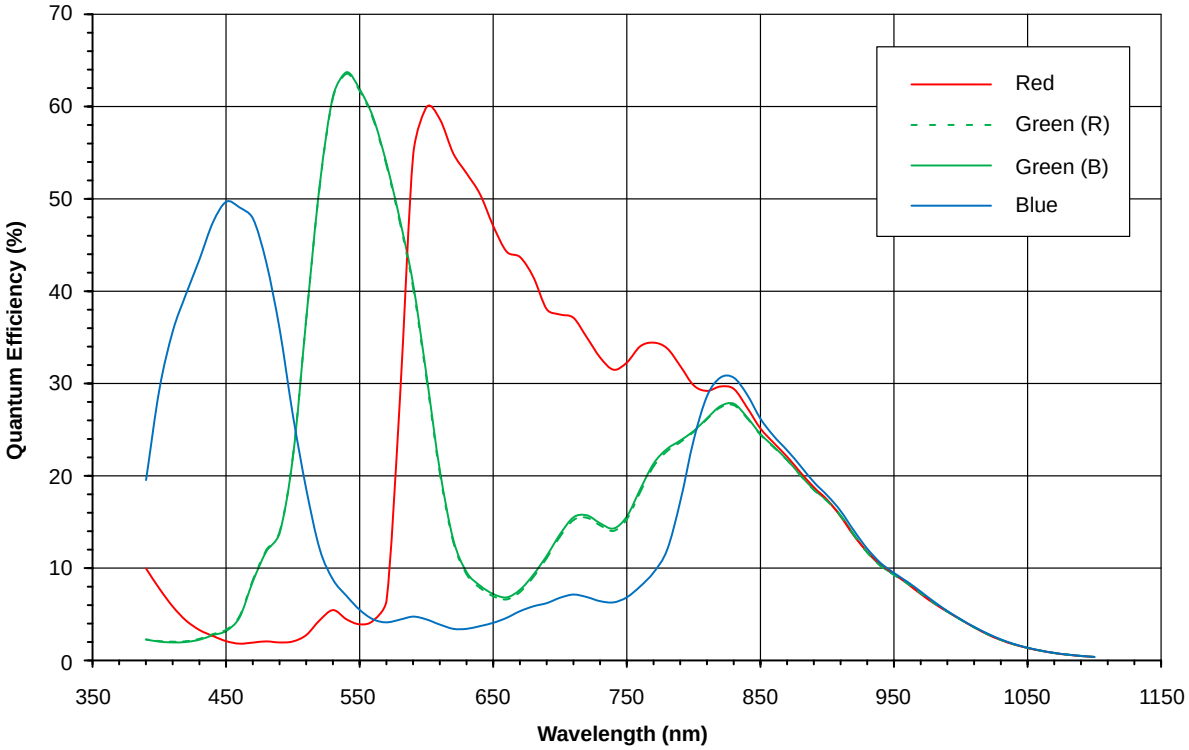

Figure 11. Quantum Efficiency − RGB Packaged Part

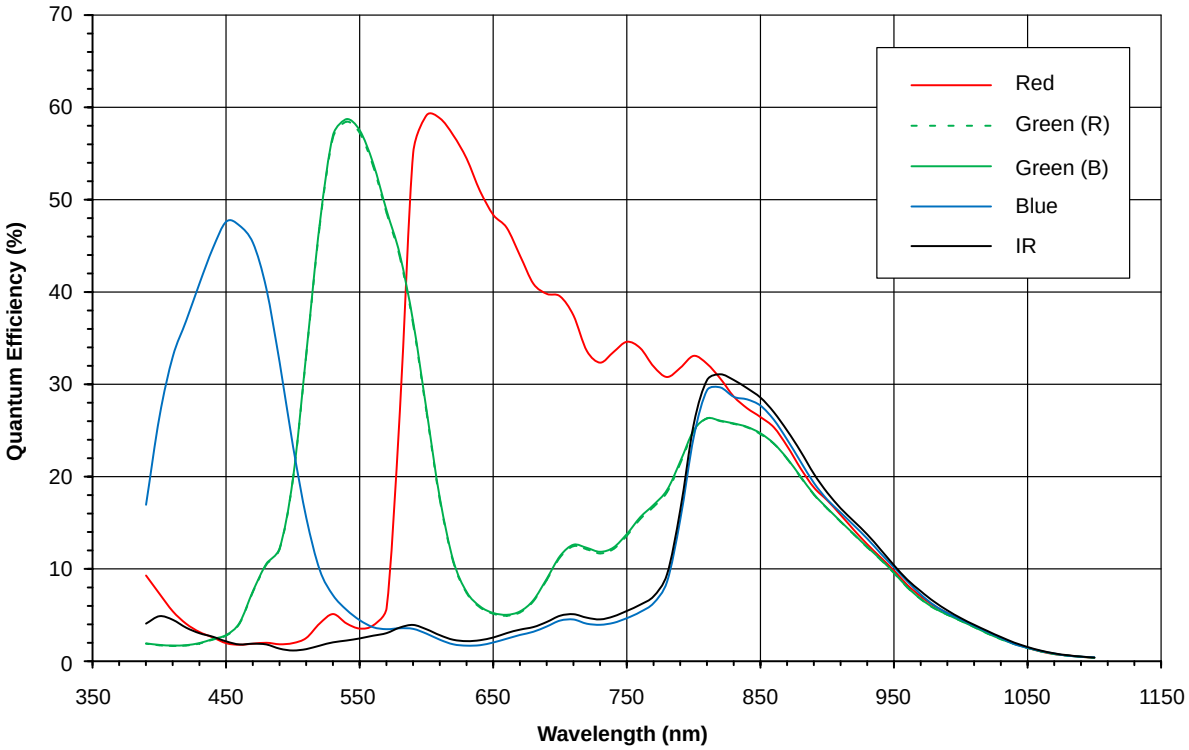

Figure 12. Quantum Efficiency − RGB−IR Packaged Part

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CRA vs. Image Height Plot

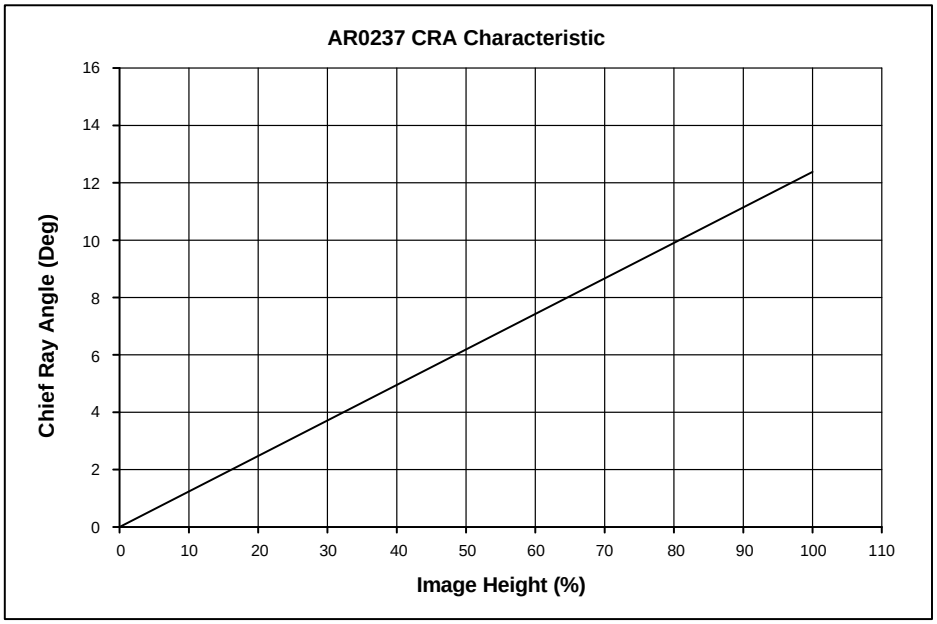

Figure 13. Chief Ray Angle Characteristics

Image Height		CRA
(%)	(mm)	(deg)
0	0	0
5	0.166	0.62
10	0.332	1.24
15	0.498	1.86
20	0.664	2.48
25	0.830	3.10
30	0.996	3.72
35	1.162	4.34
40	1.328	4.96
45	1.494	5.58
50	1.660	6.20
55	1.826	6.82
60	1.992	7.44
65	2.158	8.06
70	2.324	8.68
75	2.491	9.30
80	2.657	9.92
85	2.823	10.54
90	2.989	11.16
95	3.155	11.78
100	3.321	12.40

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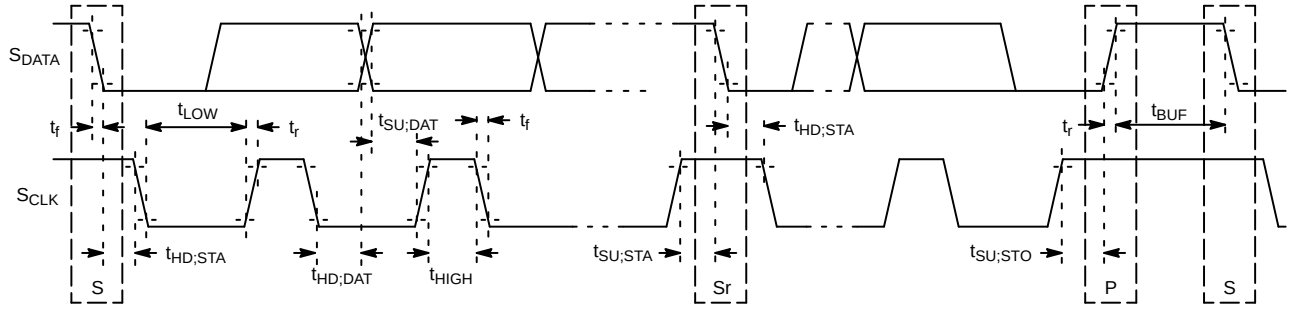
ELECTRICAL SPECIFICATIONS

Unless otherwise stated, the following specifications apply under the following conditions:

V_{DD} = 1.8 V – 0.10/+0.15;
V_{DD}_IO = V_{DD}_PLL = V_{AA} = V_{AA}_PIX = 2.8 V ± 0.3 V;
V_{DD}_SLVS = 0.4 V – 0.1/+0.2;
T_A = −30°C to +85°C−40°C to +105°C;
Output load = 10 pF;
Frequency = 74.25 MHz;
HiSPi off.

Two-Wire Serial Register Interface

The electrical characteristics of the two-wire serial register interface (S_{CLK}, S_{DATA}) are shown in Figure 14 and Table 7.



NOTE: Read sequence: For an 8-bit READ, read waveforms start after WRITE command and register address are issued.

Figure 14. Two-Wire Serial Bus Timing Parameters

Table 7. TWO-WIRE SERIAL BUS CHARACTERISTICS
(f_{EXTCLK} = 27 MHz; V_{DD} = 1.8 V; V_{DD}_IO = 2.8 V; V_{AA} = 2.8 V; V_{AA}_PIX = 2.8 V; V_{DD}_PLL = 2.8 V; T_A = 25°C)

Parameter	Symbol	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
S_{CLK} Clock Frequency	f_{SCL}	0	100	0	400	kHz
Hold Time (Repeated) START Condition. After this Period, the First Clock Pulse is Generated	$t_{HD;STA}$	4.0	–	0.6	–	μs
LOW Period of the S_{CLK} Clock	t_{LOW}	4.7	–	1.3	–	μs
HIGH Period of the S_{CLK} Clock	t_{HIGH}	4.0	–	0.6	–	μs
Set-up Time for a Repeated START Condition	$t_{SU;STA}$	4.7	–	0.6	–	μs
Data Hold Time	$t_{HD;DAT}$	0 (Note 4)	3.45 (Note 5)	0 (Note 6)	0.9 (Note 5)	μs
Data Set-up Time	$t_{SU;DAT}$	250	–	100 (Note 6)	–	ns
Rise Time of both S_{DATA} and S_{CLK} Signals	t_r	–	1000	20 + 0.1 Cb (Note 7)	300	ns
Fall Time of both S_{DATA} and S_{CLK} Signals	t_f	–	300	20 + 0.1 Cb (Note 7)	300	ns
Set-up Time for STOP Condition	$t_{SU;STO}$	4.0	–	0.6	–	μs
Bus Free Time between a STOP and START Condition	t_{BUF}	4.7	–	1.3	–	μs
Capacitive Load for each Bus Line	Cb	–	400	–	400	pF
Serial Interface Input Pin Capacitance	CIN_SI	–	3.3	–	3.3	pF

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Table 7. TWO-WIRE SERIAL BUS CHARACTERISTICS (continued)
(f_{EXTCLK} = 27 MHz; V_{DD} = 1.8 V; V_{DD}_IO = 2.8 V; V_{AA} = 2.8 V; V_{AA}_PIX = 2.8 V; V_{DD}_PLL = 2.8 V; T_A = 25°C)

Parameter	Symbol	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
S_{DATA} Max Load Capacitance	CLOAD_SD	–	30	–	30	pF
S_{DATA} Pull-up Resistor	RSD	1.5	4.7	1.5	4.7	kΩ

1. This table is based on I²C standard (v2.1 January 2000). Philips Semiconductor.
2. Two-wire control is I²C-compatible.
3. All values referred to V_{IHmin} = 0.9 V_{DD} and V_{ILmax} = 0.1 V_{DD} levels. Sensor EXCLK = 27 MHz.
4. A device must internally provide a hold time of at least 300 ns for the S_{DATA} signal to bridge the undefined region of the falling edge of S_{CLK}.
5. The maximum $t_{HD;DAT}$ has only to be met if the device does not stretch the LOW period (t_{LOW}) of the S_{CLK} signal.
6. A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system, but the requirement $t_{SU;DAT}$ = 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the S_{CLK} signal. If such a device does stretch the LOW period of the S_{CLK} signal, it must output the next data bit to the S_{DATA} line $t_{r\,max}$ + $t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the Standard-mode I²C-bus specification) before the S_{CLK} line is released.
7. Cb = total capacitance of one bus line in pF.

I/O Timing

By default, the AR0237 launches pixel data, FV, and LV with the falling edge of PIXCLK. The expectation is that the user captures D_{OUT}[11:0], FV, and LV using the rising edge of PIXCLK.

See Figure 15 below and Table 8 for I/O timing (AC) characteristics.

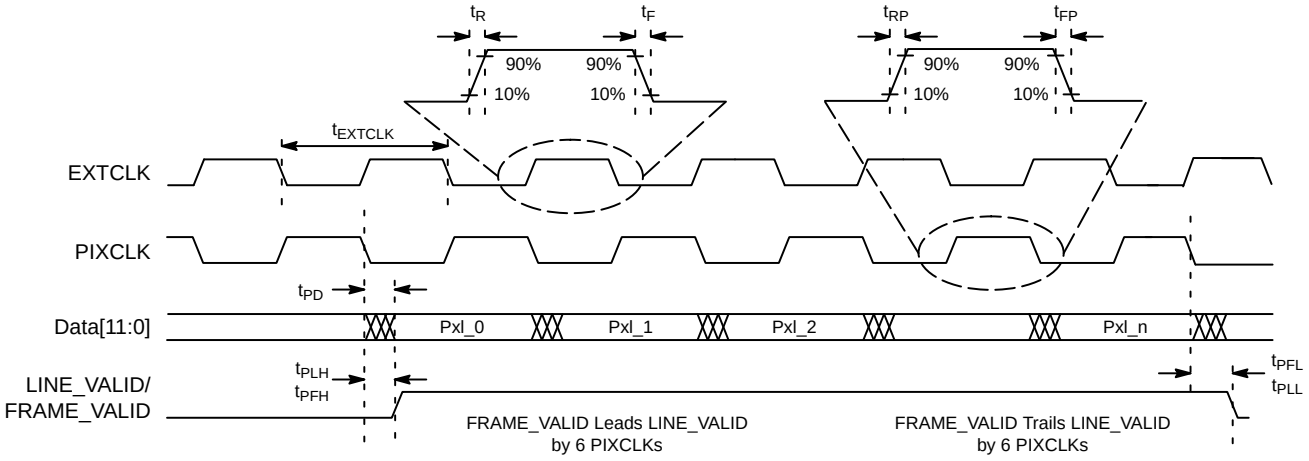

Figure 15. I/O Timing Diagram

Table 8. I/O TIMING CHARACTERISTICS
(I/O timing characteristics are measured under the following conditions: Temperature is 25°C Ambient; 10 pF Load; 1.8 V I/O Supply Voltage)

Symbol	Definition	Condition	Min	Typ	Max	Unit
$f_{EXTCLK1s}$	Input Clock Frequency		6	–	48	MHz
$t_{EXTCLK1}$	Input Clock Period		20.8	–	166	ns
t_R	Input Clock Rise Time		–	3	–	ns
t_F	Input Clock Fall Time		–	3	–	ns
t_{RP}	Pixclk Rise Time		2	3.5	5	ns
t_{FP}	Pixclk Fall Time		2	3.5	5	ns
	Clock Duty Cycle		45	50	55	%
t_{CP}	EXTCLK to PIXCLK Propagation Delay	Nominal Voltages, PLL Disabled	10	14	18	ns
f_{PIXCLK}	PIXCLK Frequency	Default, Nominal Voltages	6	–	74.25	MHz

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Table 8. I/O TIMING CHARACTERISTICS (continued)
(I/O timing characteristics are measured under the following conditions: Temperature is 25°C Ambient; 10 pF Load; 1.8 V I/O Supply Voltage)

Symbol	Definition	Condition	Min	Typ	Max	Unit
t_{PD}	PIXCLK to Data Valid	Default, Nominal Voltages	0	2.5	5	ns
t_{PFH}	PIXCLK to FV HIGH	Default, Nominal Voltages	−2	3	6	ns
t_{PLH}	PIXCLK to LV HIGH	Default, Nominal Voltages	−2	3	6	ns
t_{PFL}	PIXCLK to FV LOW	Default, Nominal Voltages	−2	2.5	6	ns
t_{PLL}	PIXCLK to LV LOW	Default, Nominal Voltages	−2	2.5	6	ns
C_{LOAD}	Output Load Capacitance		–	< 10	–	pF
C_{IN}	Input Pin Capacitance		–	2.5	–	pF

DC Electrical Characteristics

The DC electrical characteristics are shown in the tables below.

Table 9. DC ELECTRICAL CHARACTERISTICS

Symbol	Definition	Condition	Min	Typ	Max	Unit
V_{DD}	Core Digital Voltage		1.7	1.8	1.95	V
V_{DD_IO}	I/O Digital Voltage		1.7/2.5	1.8/2.8	1.9/3.1	V
V_{AA}	Analog Voltage		2.5	2.8	3.1	V
V_{AA_PIX}	Pixel Supply Voltage		2.5	2.8	3.1	V
V_{DD_PLL}	PLL Supply Voltage		2.5	2.8	3.1	V
V_{DD_SLVS}	HiSPi Supply Voltage		0.3	0.4	0.6	V
V_{IH}	Input HIGH Voltage		$V_{DD_IO} \times 0.7$	–	–	V
V_{IL}	Input LOW Voltage		–	–	$V_{DD_IO} \times 0.3$	V
I_{IN}	Input leakage Current	No Pull-up Resistor; $V_{IN} = V_{DD_IO}$ or D_{GND}	20	–	–	μA
V_{OH}	Output HIGH Voltage		$V_{DD_IO} - 0.3$	–	–	V
V_{OL}	Output LOW Voltage		–	–	0.4	V
I_{OH}	Output HIGH Current	At Specified V_{OH}	−22	–	–	mA
I_{OL}	Output LOW Current	At Specified V_{OL}	–	–	22	mA

Table 10. ABSOLUTE MAXIMUM RATINGS

Symbol	Definition	Condition	Min	Max	Unit
V_{DD_MAX}	Core Digital Voltage		–0.3	2.4	V
$V_{DD_IO_MAX}$	I/O Digital Voltage		–0.3	4	V
V_{AA_MAX}	Analog Voltage		–0.3	4	V
V_{AA_PIX}	Pixel Supply Voltage		–0.3	4	V
V_{DD_PLL}	PLL Supply Voltage		–0.3	4	V
$V_{DD_SLVS_MAX}$	HiSPi I/O Digital Voltage		–0.3	2.4	V
t_{ST}	Storage Temperature		–40	85	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

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Table 11. 1080p30 LINEAR 74 MHZ PARALLEL 2.8 V

(Operating currents are measured in mA at the following conditions: V_{AA} = V_{AA}_PIX = V_{DD}_PLL = V_{DD}_IO = 2.8 V; V_{DD} = 1.8 V; PLL Enabled and PIXCLK = 74.25 MHz; Low power mode enabled; T_A = 25°C)

Definition	Condition	Symbol	Voltage	Min	Typ	Max	Unit
Digital Operating Current	Streaming 1080p30	I_{DD}	1.8	20	34	50	mA
I/O Digital Operating Current	Streaming 1080p30	I_{DD}_IO	2.8	15	28	50	mA
Analog Operating Current	Streaming 1080p30	I_{AA}	2.8	15	26	50	mA
Pixel Supply Current	Streaming 1080p30	I_{AA}_PIX	2.8	1	3	7	mA
PLL Supply Current	Streaming 1080p30	I_{DD}_PLL	2.8	5.5	6.4	7	mA
			Power	138.2	238.72	409.2	mW

Table 12. 1080p30 LINEAR 74 MHZ PARALLEL 1.8 V

(Operating currents are measured in mA at the following conditions: V_{AA} = V_{AA}_PIX = V_{DD}_PLL = 2.8 V; V_{DD} = V_{DD}_IO = 1.8 V; PLL Enabled and PIXCLK = 74.25 MHz; Low power mode enabled; T_A = 25°C Dark Image, 8× Analog Gain, HCG, 20 ms integration time)

Definition	Condition	Symbol	Voltage	Min	Typ	Max	Unit
Digital Operating Current	Streaming 1080p30	I_{DD}	1.8	20	34	50	mA
I/O Digital Operating Current	Streaming 1080p30	I_{DD}_IO	1.8	10	14	30	mA
Analog Operating Current	Streaming 1080p30	I_{AA}	2.8	15	26	50	mA
Pixel Supply Current	Streaming 1080p30	I_{AA}_PIX	2.8	1	3	7	mA
PLL Supply Current	Streaming 1080p30	I_{DD}_PLL	2.8	5.5	6.4	7	mA
			Power	114.2	185.52	323.2	mW

Table 13. 1080p30 LINEAR 74 MHZ HISPI SLVS

(Operating currents are measured in mA at the following conditions: V_{AA} = V_{AA}_PIX = V_{DD}_PLL = 2.8 V; V_{DD} = V_{DD}_IO = 1.8 V; V_{DD}_SLVS = 0.4 V; PLL Enabled and PIXCLK = 74.25 MHz; 4-lane HiSPi mode; Low power mode enabled; T_A = 25°C Dark Image, 8× Analog Gain, HCG, 20 ms integration time)

Definition	Condition	Symbol	Voltage	Min	Typ	Max	Unit
Digital Operating Current	Streaming 1080p30	I_{DD}	1.8	25	44	65	mA
Analog Operating Current	Streaming 1080p30	I_{AA}	2.8	15	26	50	mA
Pixel Supply Current	Streaming 1080p30	I_{AA}_PIX	2.8	1	3	7	mA
PLL Supply Current	Streaming 1080p30	I_{DD}_PLL	2.8	6	7.5	8.5	mA
SLVS Supply Current	Streaming 1080p30	I_{DD}_SLVS	0.4	6	9.5	14	mA
			Power	109	185.2	306	mW

Table 14. 1080p30 LINEAR 74 MHZ HISPI HIV_{CM}

(Operating currents are measured in mA at the following conditions: V_{AA} = V_{AA}_PIX = V_{DD}_PLL = 2.8 V; V_{DD} = V_{DD}_IO = V_{DD}_SLVS = 1.8 V; PLL Enabled and PIXCLK = 74.25 MHz; 4-lane HiSPi mode; Low power mode enabled; T_A = 25°C Dark Image, 8× Analog Gain, HCG, 20 ms integration time)

Definition	Condition	Symbol	Voltage	Min	Typ	Max	Unit
Digital Operating Current	Streaming 1080p30	I_{DD}	1.8	25	44	65	mA
Analog Operating Current	Streaming 1080p30	I_{AA}	2.8	15	26	50	mA
Pixel Supply Current	Streaming 1080p30	I_{AA}_PIX	2.8	1	3	7	mA
PLL Supply Current	Streaming 1080p30	I_{DD}_PLL	2.8	6	7.5	8.5	mA
SLVS Supply Current	Streaming 1080p30	I_{DD}_SLVS	1.8	12	20	35	mA
			Power	128.2	217.4	363.4	mW

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Table 15. 1080p60 LINEAR 74 MHZ LINEAR SLVS

(Operating currents are measured in mA at the following conditions: V_{AA} = V_{AA}_PIX = V_{DD}_PLL = 2.8 V; V_{DD} = V_{DD}_IO = 1.8 V; V_{DD}_SLVS = 0.4 V; PLL Enabled and PIXCLK = 74.25 MHz; 4-lane HiSPi mode; T_A= 25°C Dark Image, 8× Analog Gain, HCG, 20 ms integration time)

Definition	Condition	Symbol	Voltage	Min	Typ	Max	Unit
Digital Operating Current	Streaming 1080p60	I_{DD}	1.8	50	88	130	mA
Analog Operating Current	Streaming 1080p60	I_{AA}	2.8	20	36	60	mA
Pixel Supply Current	Streaming 1080p60	I_{AA}_PIX	2.8	1	4	8	mA
PLL Supply Current	Streaming 1080p60	I_{DD}_PLL	2.8	7	8.5	9.5	mA
SLVS Supply Current	Streaming 1080p60	I_{DD}_SLVS	0.4	6	9.5	14	mA
			Power	170.8	298	442.6	mW

Table 16. 1080p60 LINEAR 74 MHZ LINEAR HIV_{CM}

(Operating currents are measured in mA at the following conditions: V_{AA} = V_{AA}_PIX = V_{DD}_PLL = 2.8 V; V_{DD} = V_{DD}_IO = 1.8 V; V_{DD}_SLVS = 1.8 V; PLL Enabled and PIXCLK = 74.25 MHz; 4-lane HiSPi mode; T_A= 25°C Dark Image, 8× Analog Gain, HCG, 20 ms integration time)

Definition	Condition	Symbol	Voltage	Min	Typ	Max	Unit
Digital Operating Current	Streaming 1080p60	I_{DD}	1.8	50	88	130	mA
Analog Operating Current	Streaming 1080p60	I_{AA}	2.8	20	36	60	mA
Pixel Supply Current	Streaming 1080p60	I_{AA}_PIX	2.8	1	4	8	mA
PLL Supply Current	Streaming 1080p60	I_{DD}_PLL	2.8	7	8.5	9.5	mA
SLVS Supply Current	Streaming 1080p60	I_{DD}_SLVS	1.8	12	20	35	mA
			Power	190	330.2	500	mW

Table 17. 1080p30 LINEAR 74 MHZ LINE INTERLEAVED SLVS

(Operating currents are measured in mA at the following conditions: V_{AA} = V_{AA}_PIX = V_{DD}_PLL = 2.8 V; V_{DD} = V_{DD}_IO = 1.8 V; V_{DD}_SLVS = 0.4 V; PLL Enabled and PIXCLK = 74.25 MHz; 4-lane HiSPi mode; T_A= 25°C Dark Image, 8× Analog Gain, HCG, 20 ms integration time)

Definition	Condition	Symbol	Voltage	Min	Typ	Max	Unit
Digital Operating Current	Streaming 1080p30	I_{DD}	1.8	50	88	130	mA
Analog Operating Current	Streaming 1080p30	I_{AA}	2.8	20	36	60	mA
Pixel Supply Current	Streaming 1080p30	I_{AA}_PIX	2.8	1	4	8	mA
PLL Supply Current	Streaming 1080p30	I_{DD}_PLL	2.8	7	8.5	9.5	mA
SLVS Supply Current	Streaming 1080p30	I_{DD}_SLVS	0.4	6	9.5	14	mA
			Power	170.8	298	442.6	mW

Table 18. 1080p30 LINEAR 74 MHZ LINE INTERLEAVED HIV_{CM}

(Operating currents are measured in mA at the following conditions: V_{AA} = V_{AA}_PIX = V_{DD}_PLL = 2.8 V; V_{DD} = V_{DD}_IO = 1.8 V; V_{DD}_SLVS = 1.8 V; PLL Enabled and PIXCLK = 74.25 MHz; 4-lane HiSPi mode; T_A= 25°C Dark Image, 8× Analog Gain, HCG, 20 ms integration time)

Definition	Condition	Symbol	Voltage	Min	Typ	Max	Unit
Digital Operating Current	Streaming 1080p30	I_{DD}	1.8	50	88	130	mA
Analog Operating Current	Streaming 1080p30	I_{AA}	2.8	20	36	60	mA
Pixel Supply Current	Streaming 1080p30	I_{AA}_PIX	2.8	1	4	8	mA
PLL Supply Current	Streaming 1080p30	I_{DD}_PLL	2.8	7	8.5	9.5	mA
SLVS Supply Current	Streaming 1080p30	I_{DD}_SLVS	1.8	12	20	35	mA
			Power	190	330.2	500	mW

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HiSPi Electrical Specifications

The ON Semiconductor AR0237 sensor supports both SLVS and HiV_{CM} HiSPi modes. Refer to the High-Speed Serial Pixel (HiSPi) Interface Physical Layer Specification v2.00.00 for electrical definitions, specifications, and timing information. The V_{DD}_SLVS supply in this datasheet corresponds to V_{DD}_TX in the HiSPi Physical Layer Specification. Similarly, V_{DD} is equivalent to V_{DD}_HiSPi as referenced in the specification. The DLL as implemented on AR0237 is limited in the number of available delay steps and differs from the HiSPi specification as described in this section.

Table 19. CHANNEL SKEW

(Measurement Conditions: V_{DD}_HiSPi = 1.8 V; V_{DD}_HiSPi_TX = 0.4 V; Data Rate = 480 Mbps; DLL set to 0)

Definition	Symbol	Value	Unit
Data Lane Skew in Reference to Clock	$t_{CHSKEW1PHY}$	−150	ps

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POWER-ON RESET AND STANDBY TIMING

Power-Up Sequence

The recommended power-up sequence for the AR0237 is shown in Figure 16. The available power supplies (V_{DD}_IO, V_{DD}, V_{DD}_SLVS, V_{DD}_PLL, V_{AA}, V_{AA}_PIX) must have the separation specified below.

1. Turn on V_{DD}_PLL power supply.
2. After 100 µs, turn on V_{AA} and V_{AA}_PIX power supply.
3. After 100 µs, turn on V_{DD}_IO power supply.
4. After 100 µs, turn on V_{DD} power supply.
5. After 100 µs, turn on V_{DD}_SLVS power supply.
6. After the last power supply is stable, enable EXTCLK.
7. Assert RESET_BAR for at least 1 ms. The parallel interface will be tri-stated during this time.
8. Wait 15,0000 EXTCLKs (for internal initialization into software standby.
9. Configure PLL, output, and image settings to desired values.
10. Wait 1 ms for the PLL to lock.
11. Set streaming mode (R0x301a[2] = 1).

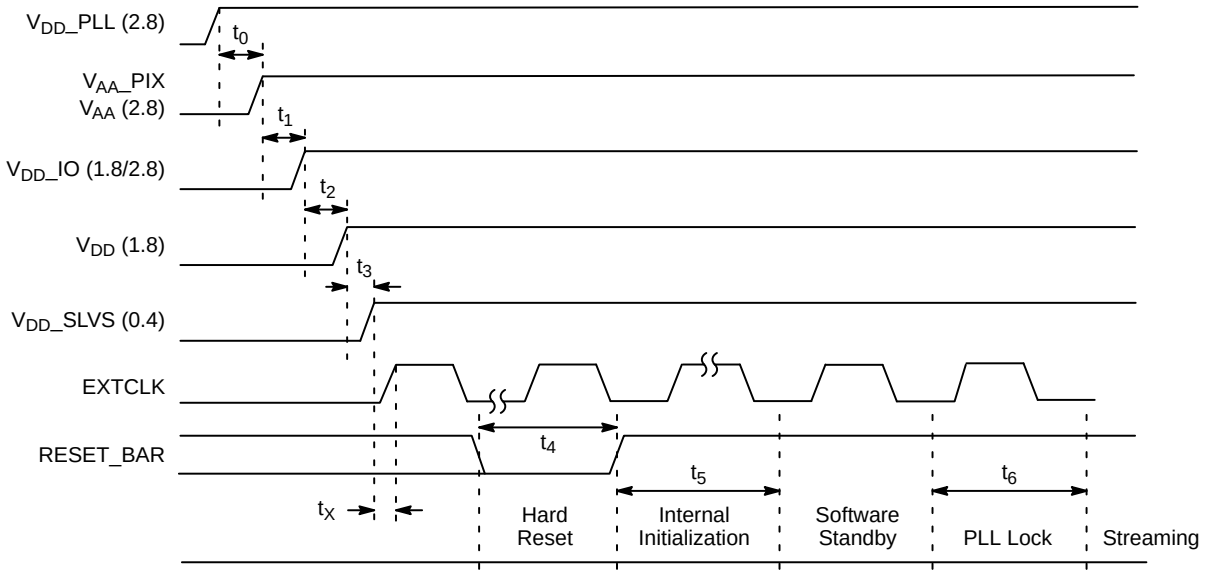

Figure 16. Power Up

Table 20. POWER-UP SEQUENCE

Symbol	Definition	Min	Typ	Max	Unit
t_0	V_{DD}_PLL to V_{AA}/V_{AA}_PIX (Note 3)	0	100	–	µs
t_1	V_{AA}/V_{AA}_PIX to V_{DD}_IO	0	100	–	µs
t_2	V_{DD}_IO to V_{DD}	0	100	–	µs
t_3	V_{DD} to V_{DD}_SLVS	0	100	–	µs
t_X	Xtal Settle Time	–	30 (Note 1)	–	ms
t_4	Hard Reset	1 (Note 2)	–	–	ms
t_5	Internal Initialization	150000	–	–	EXTCLKs
t_6	PLL Lock Time	1	–	–	ms

1. Xtal settling time is component-dependent, usually taking about 10–100 ms.
2. Hard reset time is the minimum time required after power rails are settled. In a circuit where hard reset is held down by RC circuit, then the RC time must include the all power rail settle time and Xtal settle time.
3. It is critical that V_{DD}_PLL is not powered up after the other power supplies. It must be powered before or at least at the same time as the others. If the case happens that V_{DD}_PLL is powered after other supplies then the sensor may have functionality issues and will experience high current draw on this supply.

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Power-Down Sequence

The recommended power-down sequence for the AR0237 is shown in Figure 17. The available power supplies (V_{DD}_IO, V_{DD}, V_{DD}_SLVS, V_{DD}_PLL, V_{AA}, V_{AA}_PIX) must have the separation specified below.

1. Disable streaming if output is active by setting standby R0x301a[2] = 0.
2. The soft standby state is reached after the current row or frame, depending on configuration, has ended.
3. Turn off V_{DD}_SLVS.
4. Turn off V_{DD}.
5. Turn off V_{DD}_IO.
6. Turn off V_{AA}/V_{AA}_PIX.
7. Turn off V_{DD}_PLL.

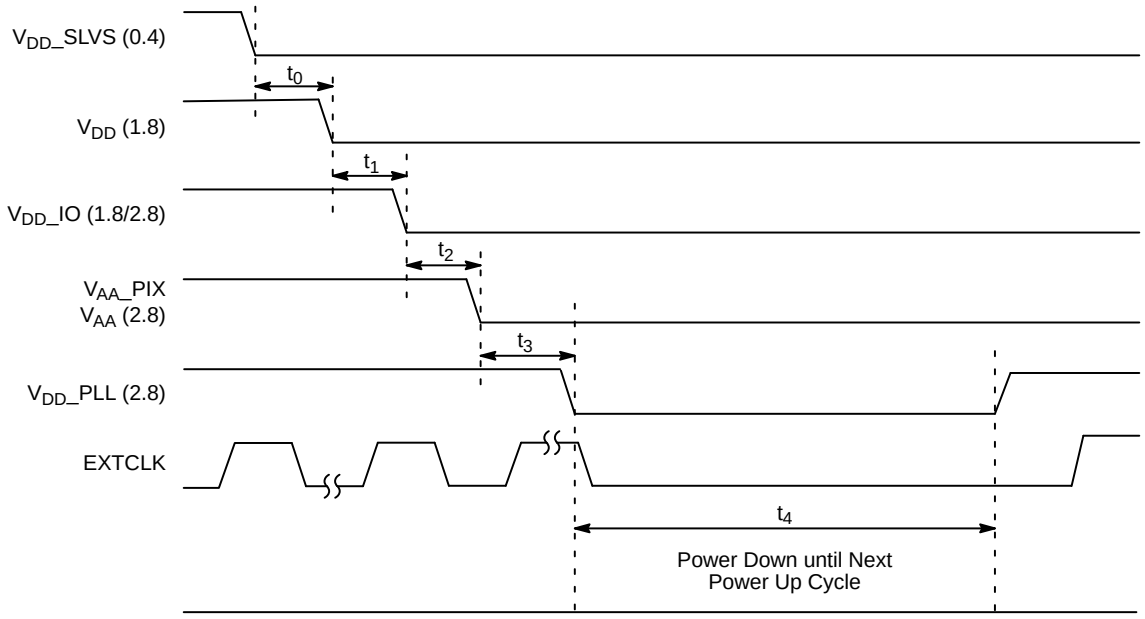

Figure 17. Power Down

Table 21. POWER-DOWN SEQUENCE

Symbol	Parameter	Min	Typ	Max	Unit
t_0	V_{DD}_SLVS to V_{DD}	0	–	–	µs
t_1	V_{DD} to V_{DD}_IO	0	–	–	µs
t_2	V_{DD}_IO to V_{AA}/V_{AA}_PIX	0	–	–	µs
t_3	V_{AA}/V_{AA}_PIX to V_{DD}_PLL	0	–	–	µs
t_4	Power Down until Next Power Up Time	100	–	–	ms

1. t_4 is required between power down and next power up time; all decoupling caps from regulators must be completely discharged.

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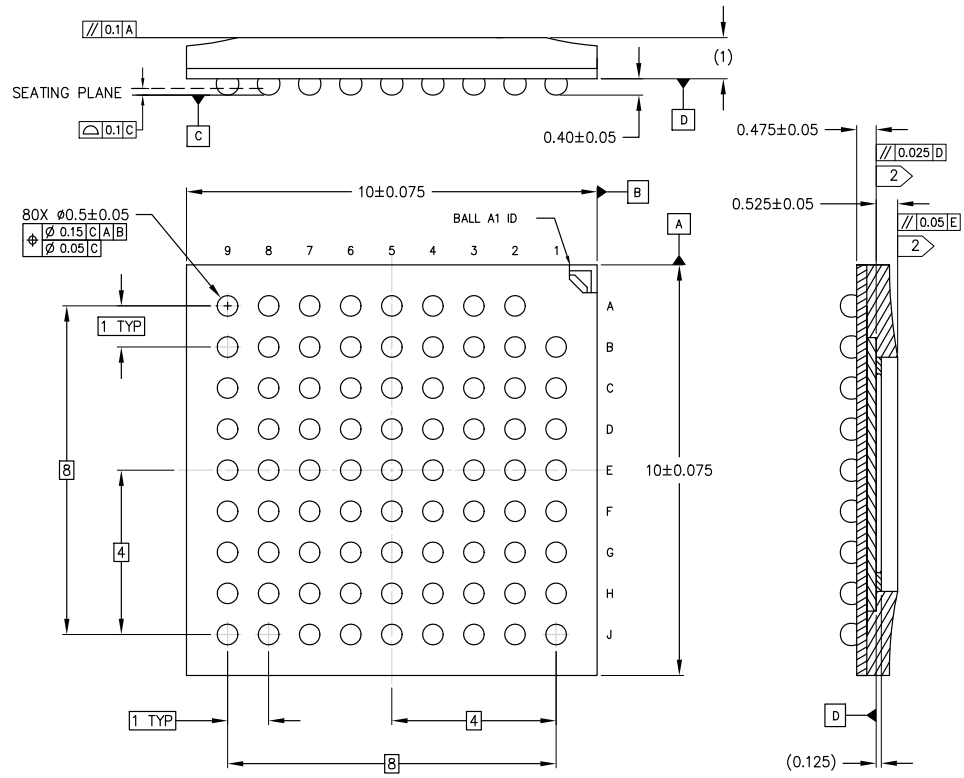
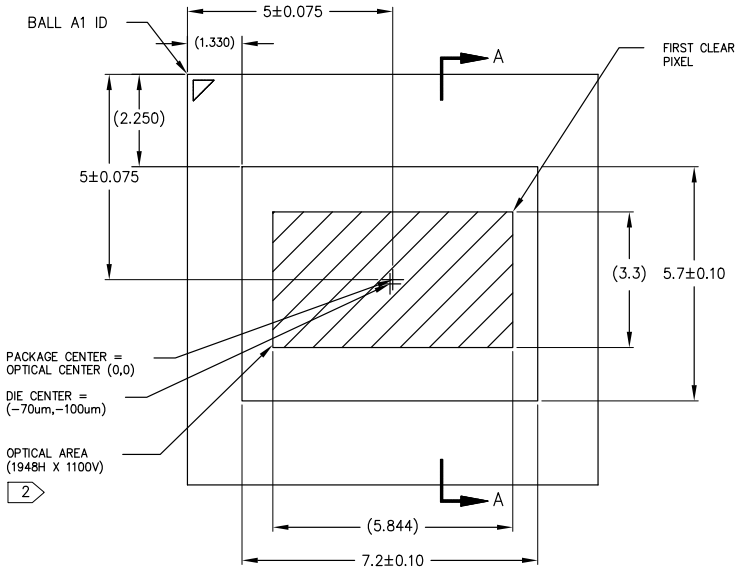
PACKAGE DIMENSIONS

IBGA80 10x10
CASE 503BA
ISSUE O





NOTES	
1	DIMENSIONS IN MM. DIMENSIONS IN ( ) ARE FOR REFERENCE ONLY.
2	MAXIMUM ROTATION OF OPTICAL AREA RELATIVE TO PACKAGE EDGES: 1°. MAXIMUM TILT OF OPTICAL AREA RELATIVE TO SUBSTRATE PLANE D: 25 MICRONS MAXIMUM TILT OF COVER GLASS RELATIVE TO OPTICAL AREA PLANE E: 50 MICRONS.

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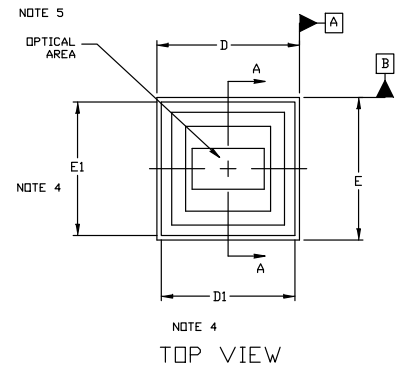
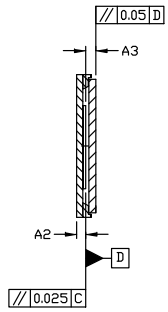
PACKAGE DIMENSIONS

PLCC48 11.43x11.43 (HiSPi)
CASE 776AQ
ISSUE C



TOP VIEW

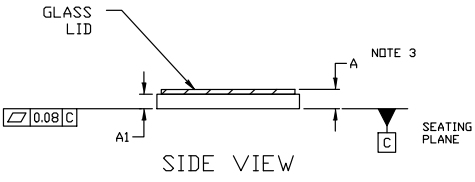


SECT. A-A

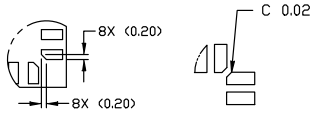
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION A INCLUDES THE PACKAGE BODY AND LID BUT DOES NOT INCLUDE HEATSINKS OR OTHER ATTACHED FEATURES.
4. THE LID DEFINED BY DIMENSIONS D2 AND E2 MUST BE LOCATED WITHIN DIMENSIONS D AND E.
5. MAXIMUM ROTATION OF OPTICAL AREA RELATIVE D AND E WILL BE 0.5°. OPTICAL AREA IS DEFINED BY THE ACTIVE PIXEL ARRAY AND IS NOT DELINEATED BY THE LIGHT BLOCK BOUNDARY. REFER TO THE DEVICE DATA SHEET FOR TOTAL ARRAY AND FIRST ACTIVE PIXEL DEFINITIONS.
6. SOLDER MASK OPENINGS FOR THERMAL CONNECTION PADS.

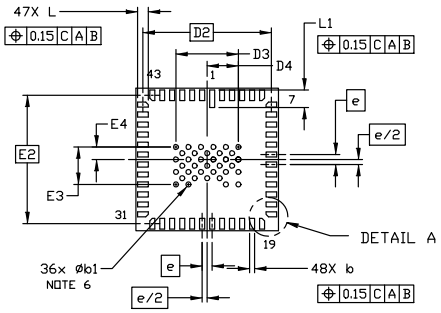
	MILLIMETERS	
DIM	MIN.	MAX.
A	---	1.62
A1	1.15 REF	
A2	0.65	0.80
A3	0.80	0.82
b	0.35	0.45
b1	0.40 REF	
D	11.33	11.53
D1	10.70 REF	
D2	10.28 BSC	
D3	5.00 REF	
D4	2.50 REF	
E	11.33	11.53
E1	10.70 REF	
E2	10.28 BSC	
E3	3.00 REF	
E4	1.00 REF	
e	0.80 BSC	
L	0.80	0.90
L1	1.35	1.45



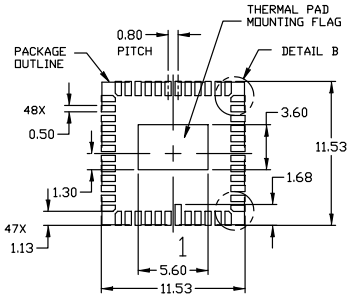
SIDE VIEW



DETAIL A DETAIL B



BOTTOM VIEW



RECOMMENDED MOUNTING FOOTPRINT

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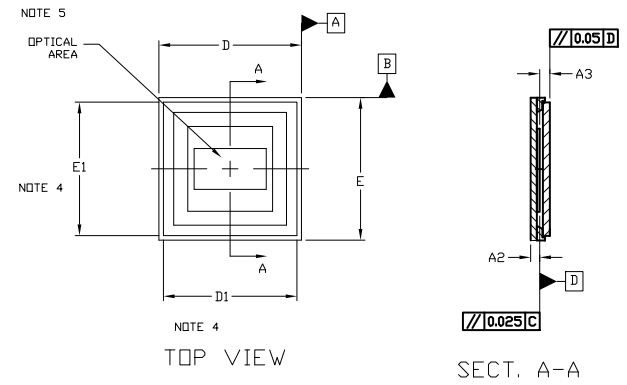
PACKAGE DIMENSIONS

PLCC48 11.43x11.43 (Parallel)
CASE 776AS
ISSUE O



NOTES:

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DIM	MILLIMETERS	
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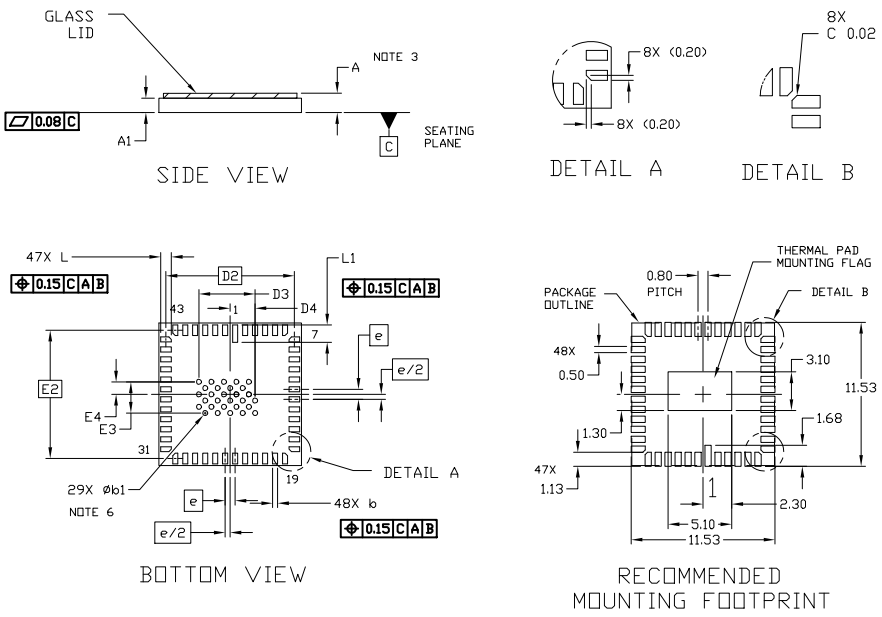
A1	1.15 REF	
A2	0.65	0.80
A3	0.80	0.82
b	0.35	0.45
b1	0.40 REF	
D	11.33	11.53
D1	10.70 REF	
D2	10.28 BSC	
D3	4.50 REF	
D4	2.00 REF	
E	11.33	11.53
E1	10.70 REF	
E2	10.28 BSC	
E3	2.50 REF	
E4	1.00 REF	
e	0.80 BSC	
L	0.80	0.90
L1	1.35	1.45



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