

BUK7623-75A

N-channel TrenchMOS standard level FET Rev. 2 — 2 February 2011

Product data sheet

1. **Product profile**

1.1 General description

Standard level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product has been designed and qualified to the appropriate AEC standard for use in automotive critical applications.

1.2 Features and benefits

- AEC Q101 compliant
- Low conduction losses due to low on-state resistance
- Suitable for standard level gate drive sources
- Suitable for thermally demanding environments due to 175 °C rating

1.3 Applications

- 12 V, 24 V and 42 V loads
- Automotive and general purpose power switching

Motors, lamps and solenoids

1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V_{DS}	drain-source voltage	$T_j \ge 25 \text{ °C}; T_j \le 175 \text{ °C}$	-	-	75	V
I _D	drain current	V _{GS} = 10 V; T _{mb} = 25 °C; see <u>Figure 1</u> ; see <u>Figure 3</u>	-	-	53	Α
P _{tot}	total power dissipation	T _{mb} = 25 °C; see <u>Figure 2</u>	-	-	138	W
Static chara	acteristics					
R _{DSon}	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A};$ $T_j = 175 ^{\circ}\text{C}; \text{ see } \frac{\text{Figure 12}}{\text{Figure 13}};$	-	-	49	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A};$ $T_j = 25 \text{ °C}; \text{ see } \frac{\text{Figure } 12}{\text{see } \frac{\text{Figure } 13}}$	-	17	23	mΩ
Avalanche	ruggedness					
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I_D = 49 A; $V_{sup} \le 75$ V; R_{GS} = 50 Ω ; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; unclamped	-	-	120	mJ



2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		
2	D	drain	mb	D
3	S	source		
mb	D	mounting base; connected to drain		mbb076 S
			SOT404 (D2PAK)	

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK7623-75A	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404

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4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 175 °C	-	75	V
V_{DGR}	drain-gate voltage	$R_{GS} = 20 \text{ k}\Omega$	-	75	V
V_{GS}	gate-source voltage		-20	20	V
I_D	drain current	T _{mb} = 25 °C; V _{GS} = 10 V; see <u>Figure 1</u> ; see <u>Figure 3</u>	-	53	Α
		T_{mb} = 100 °C; V_{GS} = 10 V; see <u>Figure 1</u>	-	37	Α
I _{DM}	peak drain current	T_{mb} = 25 °C; pulsed; $t_p \le 10 \mu s$; see Figure 3	-	213	Α
P _{tot}	total power dissipation	T _{mb} = 25 °C; see <u>Figure 2</u>	-	138	W
T _{stg}	storage temperature		-55	175	°C
T _j	junction temperature		-55	175	°C
Source-drain	n diode				
Is	source current	T _{mb} = 25 °C	-	53	Α
I _{SM}	peak source current	pulsed; $t_p \le 10 \ \mu s$; $T_{mb} = 25 \ ^{\circ}C$	-	213	Α
Avalanche r	uggedness				
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I_D = 49 A; $V_{sup} \le 75$ V; R_{GS} = 50 Ω ; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; unclamped	-	120	mJ

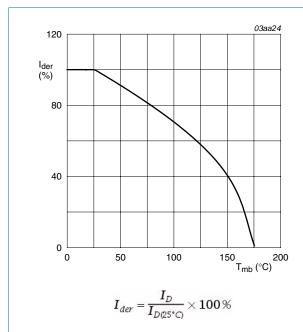


Fig 1. Normalized continuous drain current as a function of mounting base temperature

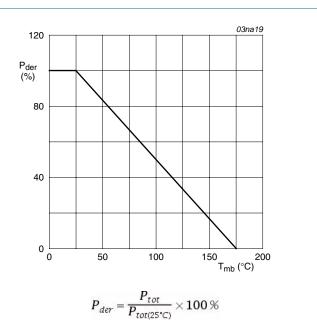
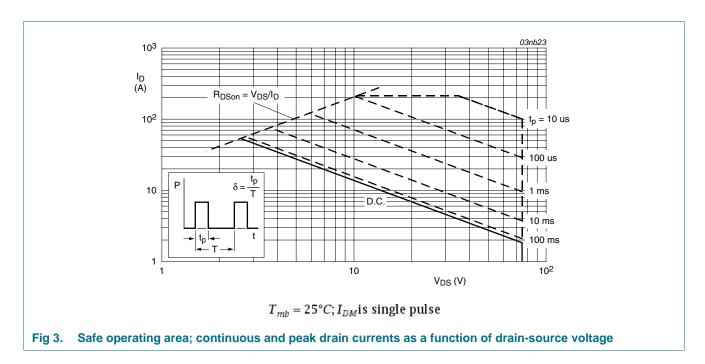


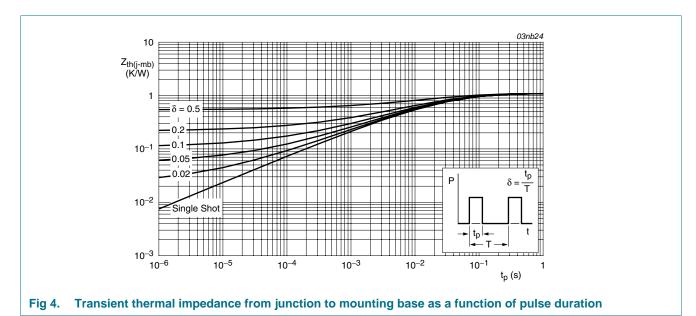
Fig 2. Normalized total power dissipation as a function of mounting base temperature



5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 4	-	-	1.1	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	minimum footprint; mounted on a printed-circuit board	-	50	-	K/W



6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit	
Static cha	racteristics						
V _{(BR)DSS}	drain-source	$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ °C}$	75	-	-	V	
breakdown voltage	$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = -55 \text{ °C}$	70	-	-	V		
V _{GS(th)} gate-source threshold voltage		$I_D = 1$ mA; $V_{DS} = V_{GS}$; $T_j = -55$ °C; see <u>Figure 11</u>	-	-	4.4	V	
			I_D = 1 mA; V_{DS} = V_{GS} ; T_j = 25 °C; see <u>Figure 11</u>	2	3	4	V
	$I_D = 1$ mA; $V_{DS} = V_{GS}$; $T_j = 175$ °C; see <u>Figure 11</u>	1	-	-	V		
DSS	drain leakage current	$V_{DS} = 75 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 \text{ °C}$	-	-	500	μΑ	
		$V_{DS} = 75 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	0.05	10	μΑ	
GSS	gate leakage current	$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	2	100	nA	
	$V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	2	100	nA		
R _{DSon} drain-source on-s	drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A; T_j = 175 °C; see <u>Figure 12</u> ; see <u>Figure 13</u>	-	-	49	mΩ	
		V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C; see <u>Figure 12</u> ; see <u>Figure 13</u>	-	17	23	mΩ	
Dynamic c	haracteristics						
C _{iss}	input capacitance	$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}; f = 1 \text{ MHz};$	-	1789	2385	pF	
Coss	output capacitance	T _j = 25 °C; see <u>Figure 14</u>	-	382	458	pF	
C _{rss}	reverse transfer capacitance		-	219	300	pF	
d(on)	turn-on delay time	$V_{DS} = 30 \text{ V}; R_L = 1.2 \Omega; V_{GS} = 10 \text{ V};$	-	14	-	ns	
r	rise time	$R_{G(ext)} = 10 \Omega; T_j = 25 °C$	-	66	-	ns	
d(off)	turn-off delay time		-	61	-	ns	
f	fall time		-	41	-	ns	
-D	internal drain inductance	from drain lead 6 mm from package to centre of die; $T_j = 25$ °C	-	4.5	-	nΗ	
		from upper edge of drain mounting base to centre of die; $T_j = 25$ °C	-	2.5	-	nΗ	
-S	internal source inductance	from source lead to source bond pad	-	7.5	-	nΗ	
Source-dra	ain diode						
√ _{SD}	source-drain voltage	$I_S = 25 \text{ A}$; $V_{GS} = 0 \text{ V}$; $T_j = 25 \text{ °C}$; see <u>Figure 15</u>	-	0.85	1.2	V	
rr	reverse recovery time	$I_S = 46 \text{ A}$; $dI_S/dt = -100 \text{ A/}\mu\text{s}$;	-	53	-	ns	
Q_r	recovered charge	$V_{GS} = -10 \text{ V}; V_{DS} = 30 \text{ V}; T_j = 25 \text{ °C}$	-	144	-	nC	

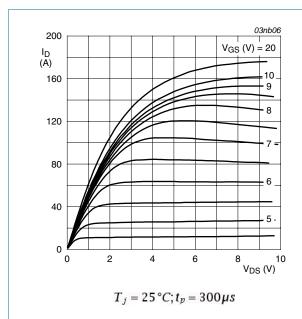


Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values

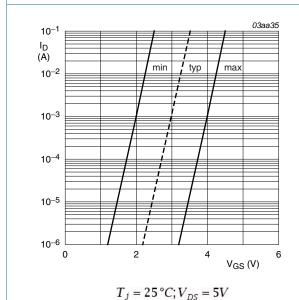
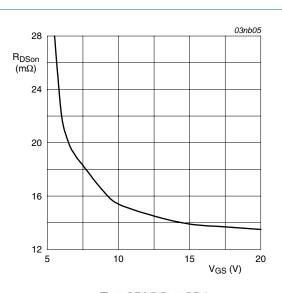
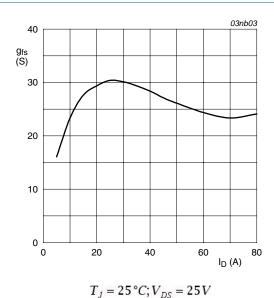


Fig 7. Sub-threshold drain current as a function of gate-source voltage



 $T_j=25\,^{\circ}C; I_D=25A$

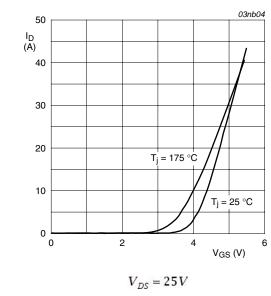
Fig 6. Drain-source on-state resistance as a function of gate-source voltage; typical values

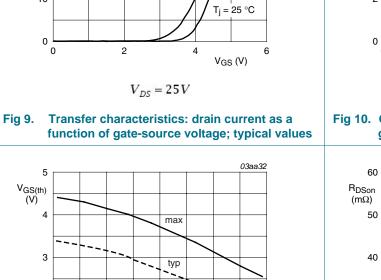


Forward transconductance as a function of

drain current; typical values

Fig 8.





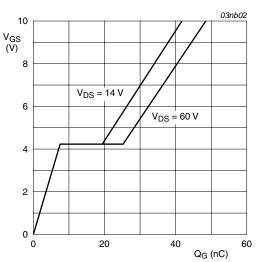
 $I_D = 1mA; V_{DS} = V_{GS}$

60

T_i (°C)

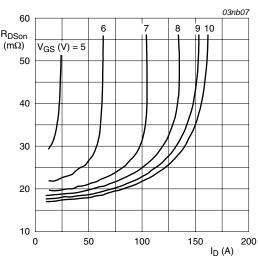
min

Fig 11. Gate-source threshold voltage as a function of junction temperature



 $T_j = 25 \,^{\circ}C; I_D = 25A$

Fig 10. Gate-source voltage as a function of turn-on gate charge; typical values



 $T_j = 25 \,^{\circ}C$

Fig 12. Drain-source on-state resistance as a function of drain current; typical values

2

-60

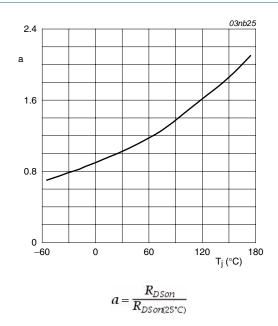
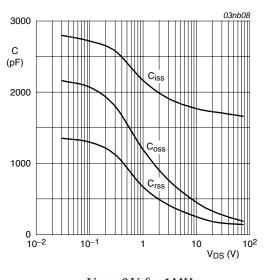


Fig 13. Normalized drain-source on-state resistance factor as a function of junction temperature



 $V_{GS} = 0V; f = 1MHz$

Fig 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

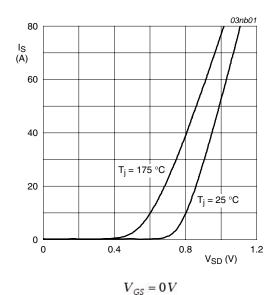


Fig 15. Reverse diode current; typical values

7. Package outline

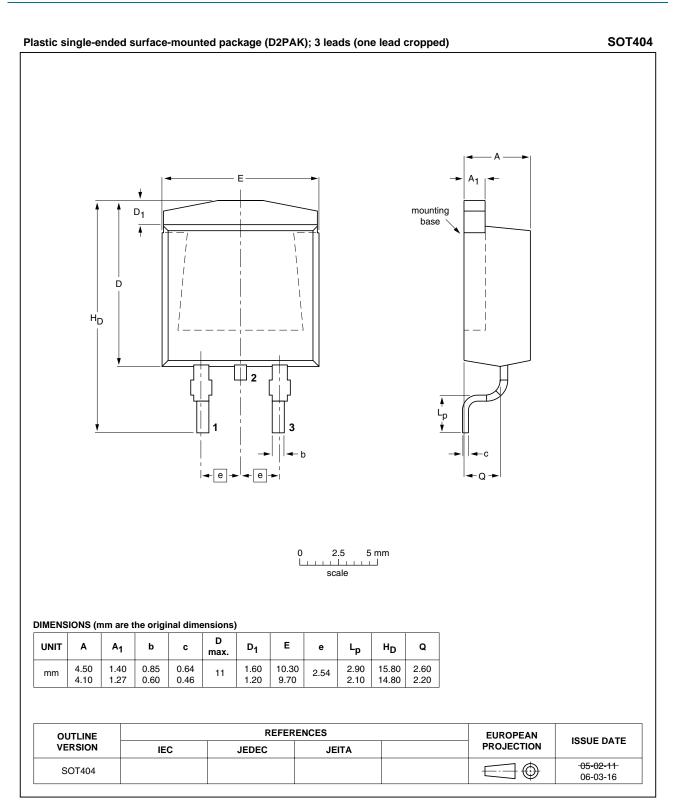


Fig 16. Package outline SOT404 (D2PAK)

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8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BUK7623-75A	20110202	Product data sheet	-	BUK7523_7623_75A-01
Modifications:		of this data sheet has be of NXP Semiconductors.	•	omply with the new identity
	 Legal texts 	have been adapted to the	e new company na	me where appropriate.
	 Type numb 	er BUK7623-75A separa	ted from data shee	t BUK7523_7623_75A-01.
BUK7523_7623_75A-01	20001009	Product specification	-	-

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9.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions"
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N-channel TrenchMOS standard level FET

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