Dual Schmitt-Trigger Buffer

The NLX2G17 MiniGate[™] is an advanced high-speed CMOS dual non-inverting Schmitt-trigger buffer in ultra-small footprint.

The NLX2G17 input and output structures provide protection when voltages up to 7.0 V are applied, regardless of the supply voltage.

The NLX2G17 can be used to enhance noise immunity or to square up slowly changing waveforms.

Features

- High Speed: $t_{PD} = 3.1 \text{ ns (Typ)} @ V_{CC} = 5.0 \text{ V}$
- Designed for 1.65 V to 5.5 V V_{CC} Operation
- Low Power Dissipation: $I_{CC} = 1 \mu A$ (Max) at $T_A = 25^{\circ}C$
- 24 mA Balanced Output Source and Sink Capability
- Balanced Propagation Delays
- Overvoltage Tolerant (OVT) Input and Output Pins
- Ultra-Small Packages
- These are Pb-Free Devices

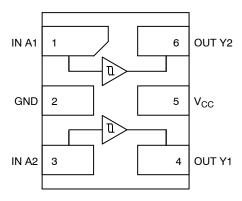


Figure 1. Pinout (Top View)

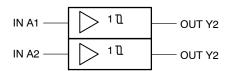


Figure 2. Logic Symbol

PIN ASSIGNMENT

A Y L L H H

1	IN A1
2	GND
3	IN A2
4	OUT Y2
5	V _{CC}
6	OUT Y1



ON Semiconductor®

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MARKING DIAGRAMS



ULLGA6 1.0 x 1.0 CASE 613AD





ULLGA6 1.2 x 1.0 CASE 613AE





ULLGA6 1.45 x 1.0 CASE 613AF





UDFN6 1.0 x 1.0 CASE 517BX





UDFN6 1.2 x 1.0 CASE 517AA





UDFN6 1.45 x 1.0 CASE 517AQ



K,4,J,Q = Device Marking M = Date Code

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

MAXIMUM RATINGS

Symbol	Parameter	1	Value	Unit		
V _{CC}	DC Supply Voltage	-0.5 to +7.0	٧			
V _{IN}	DC Input Voltage		-0.5 to +7.0	V		
V _{OUT}	DC Output Voltage		-0.5 to +7.0	V		
I _{IK}	DC Input Diode Current	V _{IN} < GND	-50	mA		
I _{OK}	DC Output Diode Current	-50	mA			
I _O	DC Output Source/Sink Current	±50	mA			
I _{CC}	DC Supply Current Per Supply Pin	±100	mA			
I _{GND}	DC Ground Current per Ground Pin	±100	mA			
T _{STG}	Storage Temperature Range	-65 to +150	°C			
T_L	Lead Temperature, 1 mm from Case for 10 Sec	onds	260	°C		
TJ	Junction Temperature Under Bias	150	°C			
MSL	Moisture Sensitivity	Level 1				
F _R	Flammability Rating Oxygen	UL 94 V-0 @ 0.125 in				
I _{LATCHUP}	Latchup Performance Above V _{CC} and Below G	Latchup Performance Above V _{CC} and Below GND at 125 °C (Note 5)				

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Measured with minimum pad spacing on an FR4 board, using 10 mm-by-1 inch, 2 ounce copper trace no air flow.

2. Tested to EIA/JESD22-A114-A.

- 3. Tested to EIA/UESD22-A115-A.
- 4. Tested to JESD22-C101-A.
- 5. Tested to EIA / JESD78.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter			Max	Unit
V _{CC}	Positive DC Supply Voltage	1.65	5.5	V	
V _{IN}	Digital Input Voltage	0	5.5	V	
V _{OUT}	Output Voltage	0	5.5	V	
T _A	Operating Free-Air Temperature	-55	+125	°C	
Δt/ΔV	Voc	= 2.5 V ± 0.2 V = 3.3 V ± 0.3 V = 5.0 V ± 0.5 V	0 0 0	No Limit No Limit No Limit	ns/V

DC ELECTRICAL CHARACTERISTICS

		Vo	V _{CC}	T _A = 25 °C		-85°C		55°C to 5°C			
Symbol	Parameter	Conditions	(V)	Min	Тур	Max	Min	Max	Min	Max	Unit
V _{T+}	Positive Threshold Voltage		1.65 2.3 2.7 3.0 4.5 5.5	0.6 1.0 1.2 1.3 1.9 2.2	1.0 1.5 1.7 1.9 2.7 3.3	1.4 1.8 2.0 2.2 3.1 3.6	0.6 1.0 1.2 1.3 1.9 2.2	1.4 1.8 2.0 2.2 3.1 3.6	0.6 1.0 1.2 1.3 1.9 2.2	1.4 1.8 2.0 2.2 3.1 3.6	٧
V _{T-}	Negative Threshold Voltage		1.65 2.3 2.7 3.0 4.5 5.5	0.2 0.4 0.5 0.6 1.0	0.5 0.75 0.87 1.0 1.5 1.9	0.8 1.15 1.4 1.5 2.0 2.3	0.2 0.4 0.5 0.6 1.0	0.8 1.15 1.4 1.5 2.0 2.3	0.2 0.4 0.5 0.6 1.0	0.8 1.15 1.4 1.5 2.0 2.3	V
V _H	Low-Level Input Voltage		1.65 2.3 2.7 3.0 4.5 5.5	0.1 0.25 0.3 0.4 0.6 0.7	0.48 0.75 0.83 0.93 1.2 1.4	0.9 1.1 1.15 1.2 1.5	0.1 0.25 0.3 0.4 0.6 0.7	0.9 1.1 1.15 1.2 1.5 1.7	0.1 0.25 0.3 0.4 0.6 0.7	0.9 1.1 1.15 1.2 1.5 1.7	V
V _{OH}	High- Level	$V_{IN} \ge V_{T+MAX}$ $I_{OH} = -100 \mu A$	1.65 – 5.5	V _{CC} - 0.1	V _{CC}		V _{CC} - 0.1		V _{CC} - 0.1		V
	Output Voltage	$\begin{array}{c} V_{IN} \geq V_{T+MAX} \\ I_{OH} = -4 \text{ mA} \\ I_{OH} = -8 \text{ mA} \\ I_{OH} = -12 \text{ mA} \\ I_{OH} = -16 \text{ mA} \\ I_{OH} = -24 \text{ mA} \\ I_{OH} = -32 \text{ mA} \end{array}$	1.65 2.3 2.7 3.0 3.0 4.5	1.29 1.9 2.2 2.4 2.3 3.8	1.52 2.1 2.4 2.7 2.5 4.0		1.29 1.9 2.2 2.4 2.3 3.8		1.29 1.9 2.2 2.4 2.3 3.8		
V _{OL}	Low-Level Output Voltage	$V_{IN} \leq V_{T-MIN}$ $I_{OL} = 100 \mu A$	1.65 – 5.5		0	0.1		0.1		0.1	V
	voltage	$\begin{array}{c} V_{IN} \leq V_{T-MIN} \\ I_{OH} = 4 \text{ mA} \\ I_{OH} = 8 \text{ mA} \\ I_{OH} = 12 \text{ mA} \\ I_{OH} = 16 \text{ mA} \\ I_{OH} = 24 \text{ mA} \\ I_{OH} = 32 \text{ mA} \end{array}$	1.65 2.3 2.7 3.0 3.0 4.5		0.08 0.2 0.22 0.28 0.38 0.42	0.24 0.3 0.4 0.4 0.55 0.55		0.24 0.3 0.4 0.4 0.55 0.55		0.24 0.3 0.4 0.4 0.55 0.55	
I _{IN}	Input Leakage Current	$0 \le V_{IN} \le 5.5 V$	0 to 5.5			±0.1		±1.0		±1.0	μΑ
l _{OFF}	Power-Off Output Leakage Current	V _{OUT} = 5.5 V	0			1.0		10		10	μΑ
I _{CC}	Quiescent Supply Current	$0 \le V_{IN} \le V_{CC}$	5.5			1.0		10		10	μΑ

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0 \text{ nS}$)

		V _{CC}	Vcc Test		΄ _Α = 25 °(C	T _A = - to +1		
Symbol	Parameter	(V)	Condition	Min	Тур	Max	Min	Max	Unit
t _{PLH} , t _{PHL}	Propagation Delay Input A to Output	1.65	$R_L = 1 M\Omega$, $C_L = 15 pF$	2.0	9.1	15	2.0	15.6	ns
		1.8	$R_L = 1 M\Omega$, $C_L = 15 pF$	2.0	7.6	12.5	2.0	13	
		2.3-2.7	$R_L = 1 M\Omega$, $C_L = 15 pF$	1.0	5.0	9.0	1.0	9.5	
		3.0-3.6	$R_L = 1 M\Omega$, $C_L = 15 pF$	1.0	3.7	6.3	1.0	6.5	
			$R_L = 500 \Omega,$ $C_L = 50 pF$	1.5	4.4	7.2	1.5	7.5	
		4.5–5.5	$R_L = 1 M\Omega$, $C_L = 15 pF$	0.5	3.1	5.2	0.5	5.5	
			$R_L = 500 \Omega$, $C_L = 50 pF$	0.8	3.7	5.9	0.8	6.2	
C _{IN}	Input Capacitance	5.5	V _{IN} = 0 V or V _{CC}		7.0				pF
C _{PD}	Power Dissipation Capacitance (Note 6)	3.3 5.5	10 MHz V _{IN} = 0 V or V _{CC}		9.0 11				pF

^{6.} C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the dynamic operating current consumption without load. Average operating current can be obtained by the equation I_{CC(OPR)} = C_{PD} • V_{CC} • f_{in} + I_{CC}. C_{PD} is used to determine the no–load dynamic power consumption: P_D = C_{PD} • V_{CC}² • f_{in} + I_{CC} • V_{CC}.

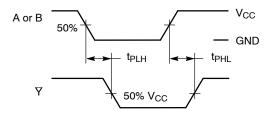
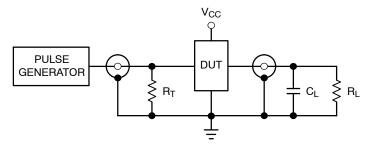


Figure 3. Switching Waveforms



 $R_T = Z_{OUT}$ of pulse generator (typically 50 Ω)

Figure 4. Test Circuit

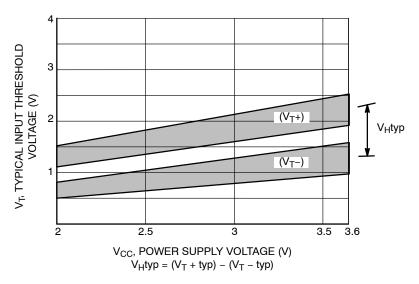
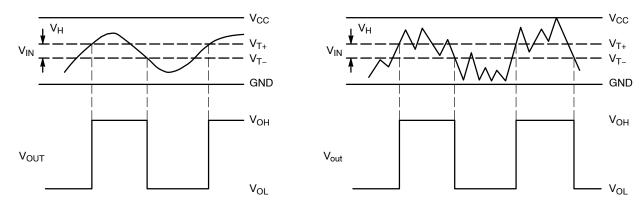


Figure 5. Typical Input Threshold, V_T+, V_T-versus Power Supply Voltage



(a) A Schmitt-Trigger Squares Up Inputs With Slow Rise and Fall Times

(b) A Schmitt-Trigger Offers Maximum Noise Immunity

Figure 6. Typical Schmitt-Trigger Applications

ORDERING INFORMATION

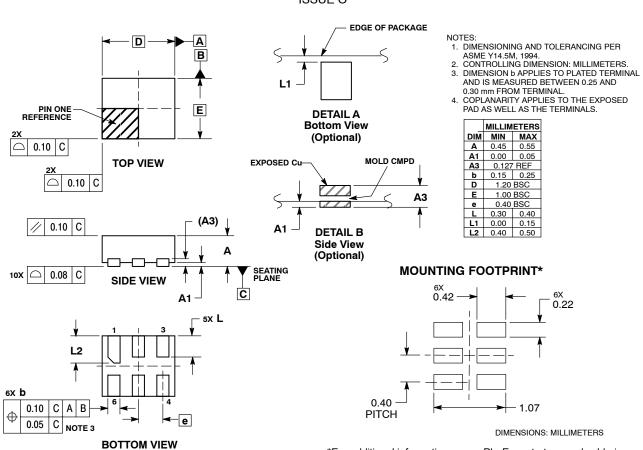
Device	Package	Shipping [†]
NLX2G17AMX1TCG	ULLGA6, 1.45 x 1.0, 0.5P (Pb-Free)	3000 / Tape & Reel
NLX2G17BMX1TCG	ULLGA6, 1.2 x 1.0, 0.4P (Pb-Free)	3000 / Tape & Reel
NLX2G17CMX1TCG	ULLGA6, 1.0 x 1.0, 0.35P (Pb-Free)	3000 / Tape & Reel
NLX2G17MUTCG*	UDFN6, 1.2 x 1.0, 0.4P (Pb-Free)	3000 / Tape & Reel
NLX2G17AMUTCG*	UDFN6, 1.45 x 1.0, 0.5P (Pb-Free)	3000 / Tape & Reel
NLX2G17CMUTCG*	UDFN6, 1.0 x 1.0, 0.35P (Pb-Free)	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

^{*}In Development

PACKAGE DIMENSIONS

UDFN6 1.2x1.0, 0.4P CASE 517AA ISSUE O



^{*}For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

UDFN6 1.45x1.0, 0.5P CASE 517AQ **ISSUE O** D Α NOTES: 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994. 2. CONTROLLING DIMENSION: MILLIMETERS. 3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP. В **DETAIL A** PIN ONE REFERENCE OPTIONAL CONSTRUCTIONS Е MILLIMETERS DIM MIN MAX A 0.45 0.55 A1 0.00 0.05 0.10 C EXPOSED Cu MOLD CMPD 0.07 REF A2 **TOP VIEW** b D E 0.20 0.30 |△| 0.10 | C 1.45 BSC 1.00 BSC е 0.50 BSC DETAIL B **DETAIL B** 0.30 0.40 --- 0.15 OPTIONAL CONSTRUCTIONS 0.05 C **MOUNTING FOOTPRINT** 0.05 C Α1 C SEATING PLANE 6X 0.30 SIDE VIEW **A2** PACKAGE OUTLINE е 6X L 1.24 DETAIL A 0.53 0.50 **PITCH** DIMENSIONS: MILLIMETERS *For additional information on our Pb-Free strategy and soldering 0.10 CAB details, please download the ON Semiconductor Soldering and С моте з

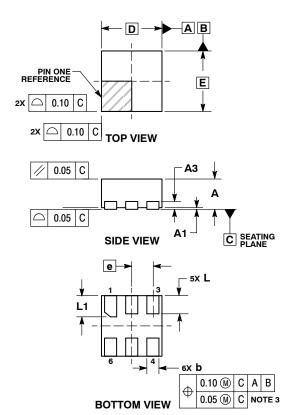
Mounting Techniques Reference Manual, SOLDERRM/D.

0.05

BOTTOM VIEW

PACKAGE DIMENSIONS

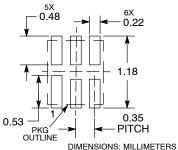
UDFN6 1.0x1.0, 0.35P CASE 517BX **ISSUE O**



- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.
 3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 MM FROM TERMINAL TIP.
 4. PACKAGE DIMENSIONS EXCLUSIVE OF BURRS AND MOLD FLASH.

	MILLIMETERS					
DIM	MIN	MAX				
Α	0.45	0.55				
A1	0.00	0.05				
А3	0.13 REF					
b	0.12	0.22				
D	1.00	BSC				
Е	1.00	BSC				
е	0.35 BSC					
L	0.25	0.35				
L1	0.30	0.40				

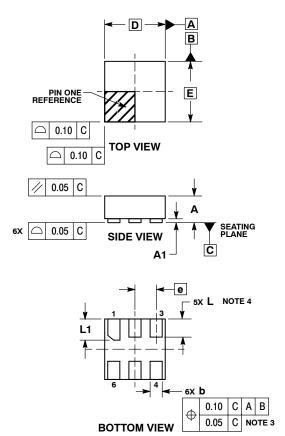
RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

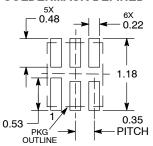
ULLGA6 1.0x1.0, 0.35P CASE 613AD ISSUE A



- NOTES:
 1. DIMENSIONING AND TOLERANCING PER
 ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.
 3. DIMENSION b APPLIES TO PLATED TERMINAL
 AND IS MEASURED BETWEEN 0.15 AND
 0.30 mm FROM THE TERMINAL TIP.
 4. A MAXIMUM OF 0.05 PULL BACK OF THE
 PLATED TERMINAL FROM THE EDGE OF THE
 PACKAGE IS ALLOWED. PACKAGE IS ALLOWED.

	MILLIMETERS					
DIM	MIN MAX					
Α		0.40				
A1	0.00	0.05				
b	0.12	0.22				
D	1.00 BSC					
E	1.00 BSC					
е	0.35 BSC					
L	0.25	0.35				
L1	0.30	0.40				

MOUNTING FOOTPRINT SOLDERMASK DEFINED*

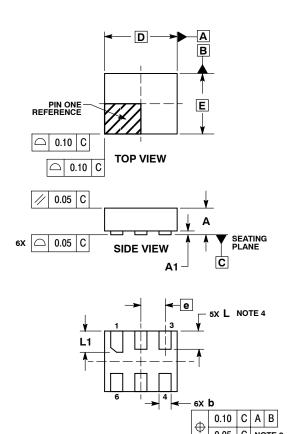


DIMENSIONS: MILLIMETERS

^{*}For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

ULLGA6 1.2x1.0, 0.4P CASE 613AE ISSUE A



BOTTOM VIEW

0.05 C NOTE 3

NOTES:

- NOTES:

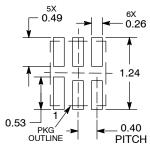
 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.

 2. CONTROLLING DIMENSION: MILLIMETERS.

 3. DIMENSION & APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm EPOLM TUE TERMINAL TIP.
- 0.30 mm FROM THE TERMINAL TIP.
 A MAXIMUM OF 0.05 PULL BACK OF THE
 PLATED TERMINAL FROM THE EDGE OF THE
 PACKAGE IS ALLOWED.

	MILLIMETERS						
DIM	MIN	MAX					
Α		0.40					
A1	0.00	0.05					
b	0.15	0.25					
D	1.20	BSC					
E	1.00	BSC					
е	0.40	BSC					
L	0.25	0.35					
L1	0.35	0.45					

MOUNTING FOOTPRINT SOLDERMASK DEFINED*

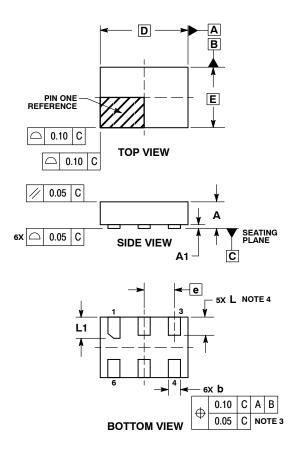


DIMENSIONS: MILLIMETERS

^{*}For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

ULLGA6 1.45x1.0, 0.5P CASE 613AF **ISSUE A**

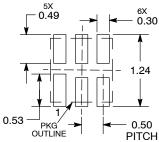


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- DIMENSIONING AND TOLERANCING PER
- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 CONTROLLING DIMENSION: MILLIMETERS.
 DIMENSION 6 APPLIES TO PLATED TERMINAL AND 1S MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.
 A MAXIMUM OF 0.05 PULL BACK OF THE PLATED TERMINAL FROM THE EDGE OF THE PLATED TERMINAL FROM THE EDGE OF THE
- PACKAGE IS ALLOWED.

	MILLIMETERS					
DIM	MIN	MAX				
Α		0.40				
A1	0.00	0.05				
b	0.15	0.25				
D	1.45 BSC					
Е	1.00 BSC					
е	0.50 BSC					
L	0.25	0.35				
L1	0.30	0.40				

MOUNTING FOOTPRINT **SOLDERMASK DEFINED***



DIMENSIONS: MILLIMETERS

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