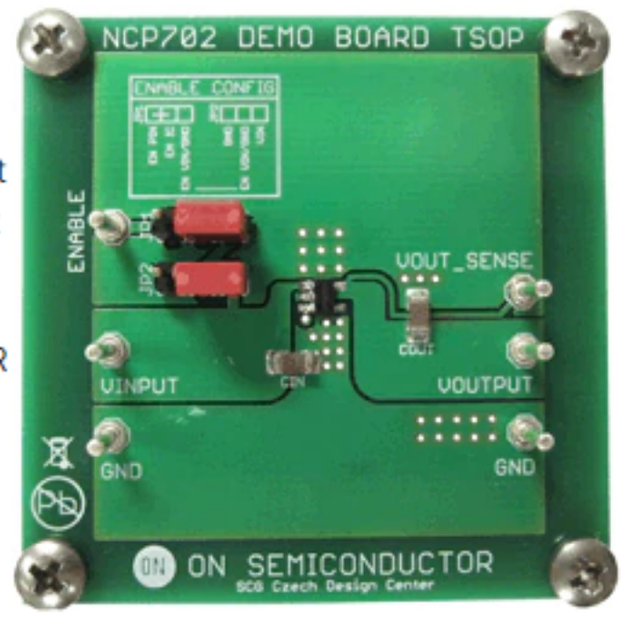
NCP702SN33T1GEVB: 3.3 V LDO Linear Regulator Evaluation Board



The NCP702 is a high performance 200mA Low Dropout Linear Regulator. This device delivers excellent noise and dynamic performance. Thanks to its adaptive ground current feature the device consumes only 10µA of quiescent current at no-load condition.

The regulator features ultra-low noise of 11µVRMS, the PSRR of 68dB at 1kHz and very good load/line transient performance. Such excellent dynamic parameters and small package size make the device an ideal choice for powering the precision analog and noise sensitive circuitry in portable applications. The LDO achieves this ultra-low noise level without the need for a noise bypass capacitor.

A Logic EN input provides ON/OFF control of the output voltage. When the EN is low the device consumes as low as typ. 10nA from the IN terminal. The device is fully protected in case of output overload, output short circuit condition and overheating assuring a very robust design.

This demonstration board operates from a dc input voltage: VIN ≤ 5.5V and produces fixed output voltage which is set internally within the IC. External waveform generator could be connected to the EN (Enable) pin in order to verify the ON/OFF operation.

Evaluation/Development Tool Information

Product	Status	Compliance	Short Description	Parts Used	Action
NCP702SN33T1GEVB	Active	Pb-free	3.3 V LDO Linear Regulator Evaluation Board	NCP702SN33T1G	Buy

Technical Documents

Type	Document Title	Document ID/Size	Rev
Eval Board: BOM	NCP702SN33T1GEVB Bill of Materials ROHS Compliant	NCP702SN33T1GEVB_BOM_ROHS.PDF - 71.0 KB	0
Eval Board: Gerber	NCP702SN33T1GEVB Gerber Layout Files (Zip Format)	NCP702SN33T1GEVB_GERBER.ZIP - 31.0 KB	0
Eval Board: Schematic	NCP702SN33T1GEVB Schematic	NCP702SN33T1GEVB_SCHEMATIC.PDF - 37.0 KB	0
Eval Board: Test Procedure	NCP702SN33T1GEVB Test Procedure	NCP702SN33T1GEVB_TEST_PROCEDURE.PDF - 205.0 KB	0

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