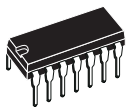
M74HCT04

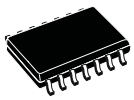
Hex inverter

Features

- High speed:
  t_{PD} = 11 ns (typ.) at V_{CC} = 4.5 V
- Low power dissipation:
  I_{CC} = 1 µA (max.) at T_A = 25 °C
- Compatible with TTL outputs:
  V_{IH} = 2 V (min.) V_{IL} = 0.8 V (max)
- Balanced propagation delays:
  $t_{PLH} \cong t_{PHL}$
- Symmetrical output impedance:
  $|I_{OH}| = I_{OL}$ = 4 mA (min)
- Pin and function compatible with 74 series 04



DIP-14



SO-14

Description

The M74HCT04 is a high speed CMOS hex inverter fabricated with silicon gate C^2MOS technology.

The internal circuit is composed of 3 stages including a buffer output, which enables high noise immunity and stable output.

The M74HCT04 is designed to directly interface HSC^2MOS systems with TTL and NMOS components.

All inputs are equipped with protection circuits against static discharge and transient excess voltage.

Table 1. Device summary

Order code	Package	Packing
M74HCT04B1R	DIP-14	Tube
M74HCT04RM13TR	SO-14	Tape and reel

1 Pin connection and IEC logic symbols

Figure 1. Pin connections and IEC logic symbols

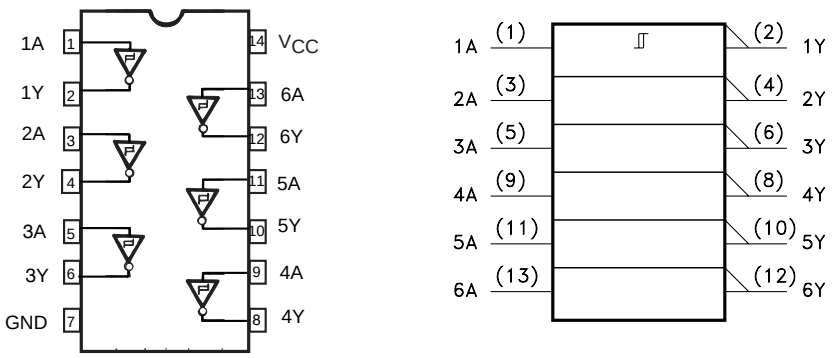


Table 2. Pin description

Pin number	Symbol	Name and function
1, 3, 5, 9, 11, 13	1A to 6A	Data inputs
2, 4, 6, 8, 10, 12	1Y to 6Y	Data outputs
7	GND	Ground (0 V)
14	V_{CC}	Positive supply voltage

Figure 2. Input and output equivalent circuit

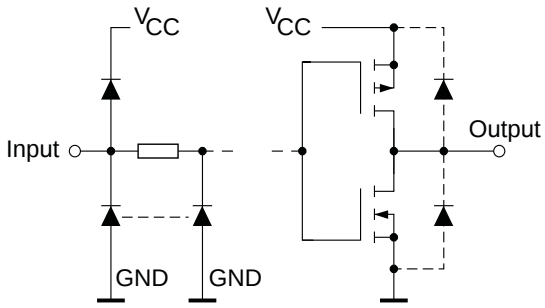


Table 3. Truth table

A	Y
L	H
H	L

2 Maximum rating

Stressing the device above the rating listed in the “Absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only, and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	-0.5 to +7	V
V_I	DC input voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC output voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC input diode current	±20	mA
I_{OK}	DC output diode current	±20	mA
I_O	DC output current	±25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground current	±50	mA
P_D	Power dissipation	500(1)	mW
T_{stg}	Storage temperature	-65 to +150	°C
T_L	Lead temperature (10 sec)	300	°C

1. 500 mW at 65 °C; derate to 300 mW by 10 mW/ °C from 65 °C to 85 °C

Table 5. Recommemded operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	4.5 to 5.5	V
V_I	Input voltage	0 to V_{CC}	V
V_O	Output voltage	0 to V_{CC}	V
T_{op}	Operating temperature	-55 to 125	°C
t_r, t_f	Input rise and fall time (V_{CC} = 4.5 to 5.5 V)	0 to 500	ns

Table 6. DC specifications

Symbol	Parameter	Test condition		Value							Unit
		V_{CC} (V)		T_A = 25 °C			-40 to 85°C		-55 to 125°C		
				Min	Typ	Max	Min	Max	Min	Max	
V_{IH}	High level input voltage	4.5 to 5.5		2.0			2.0		2.0		V
V_{IL}	Low level input voltage	4.5 to 5.5				0.8		0.8		0.8	V
V_{OH}	High level output voltage	4.5	I_O = -20 µA	4.4	4.5		4.4		4.4		V
			I_O = -4.0 mA	4.18	4.31		4.13		4.10		
V_{OL}	Low level output voltage	4.5	I_O = 20 µA		0.0	0.1		0.1		0.1	V
			I_O = 4.0 mA		0.17	0.26		0.33		0.40	
I_I	Input leakage current	5.5	V_I = V_{CC} or GND			±0.1		±1		±1	µA
I_{CC}	Quiescent supply current	5.5	V_I = V_{CC} or GND			1		10		20	µA
ΔI_{CC}	Additional worst case supply current	5.5	Per input pin V_I = 0.5 V or V_I = 2.4 V Other inputs at V_{CC} or GND I_O = 0			2.0		2.9		3.0	mA

Table 7. AC electrical characteristics (C_L = 50 pF, input t_r = t_f = 6 ns)

Symbol	Parameter	Test condition		Value							Unit
		V_{CC} (V)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output transition time	4.5			8	15		19		23	ns
t_{PLH} t_{PHL}	Propagation delay time	4.5			11	18		23		27	ns

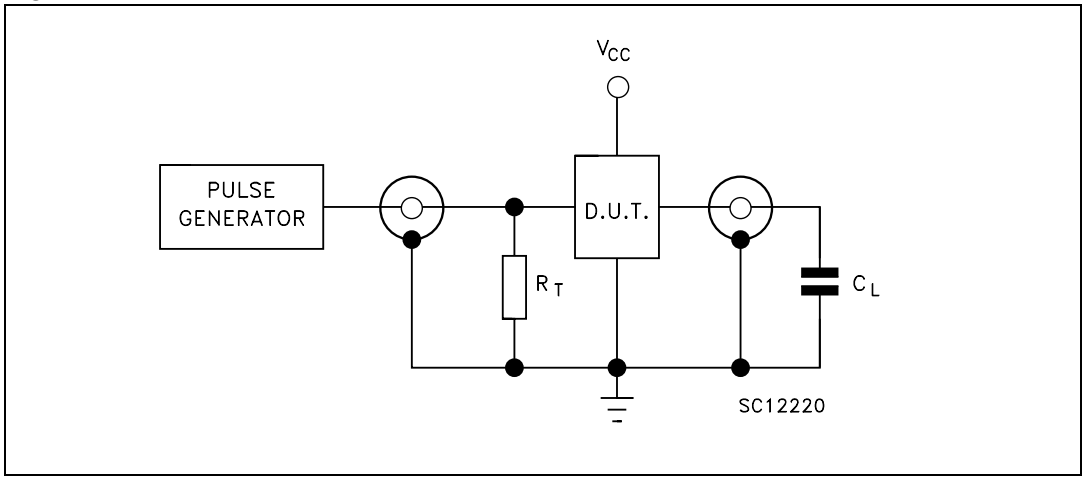
Table 8. Capacitive characteristics

Symbol	Parameter	Test condition		Value							Unit
		V_{CC} (V)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
				Min	Typ	Max	Min	Max	Min	Max	
C_{IN}	Input capacitance				5	10		10		10	pF
C_{PD}	Power dissipation capacitance (1)				20						pF

1. C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/6$ (per gate)

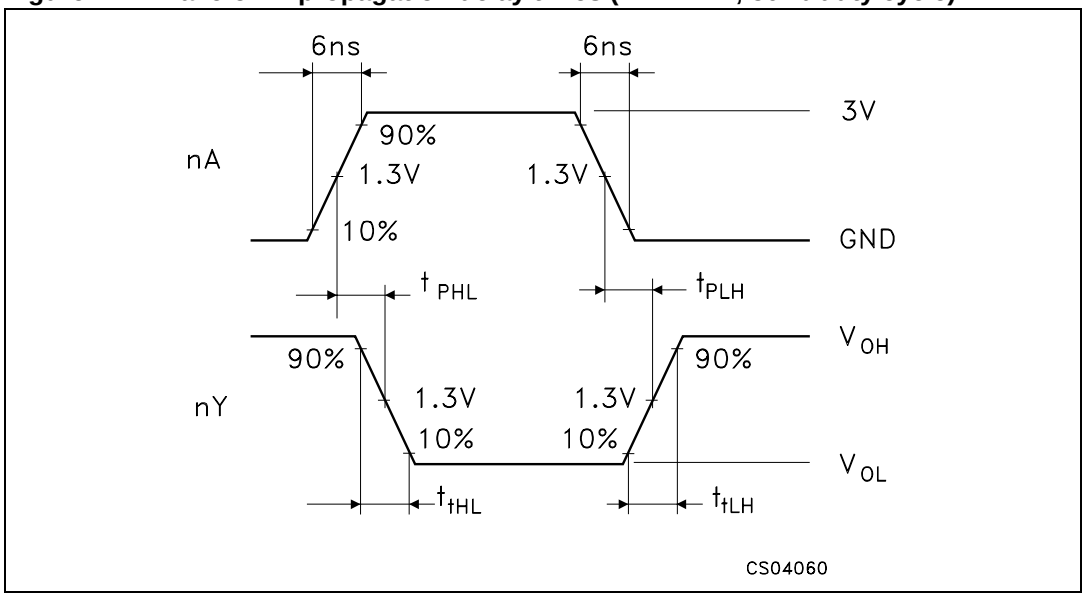
3 Test circuit

Figure 3. Test circuit



1. C_L = 50pF or equivalent (includes jig and probe capacitance)
2. $R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

Figure 4. Waveform: propagation delay times (f = 1 MHz; 50 % duty cycle)

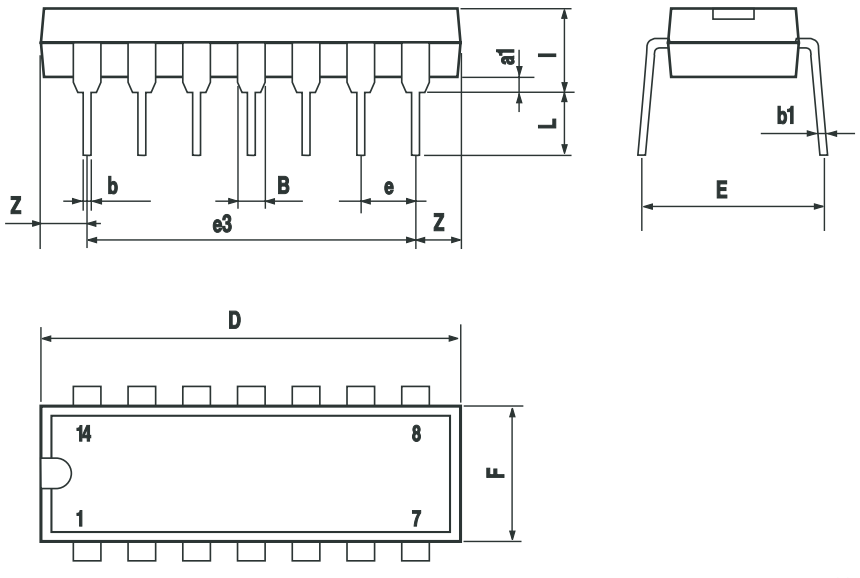


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Plastic DIP-14 MECHANICAL DATA

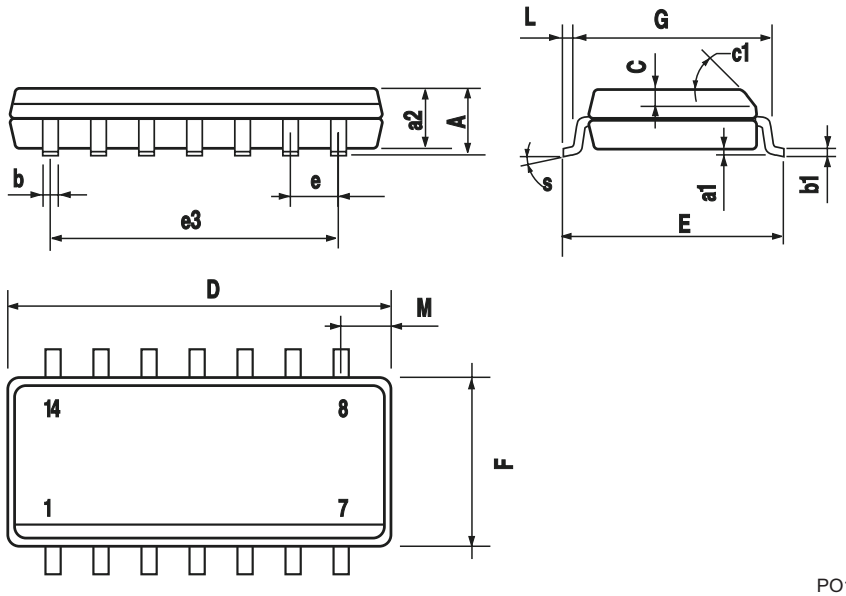
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	1.39		1.65	0.055		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		15.24			0.600	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z	1.27		2.54	0.050		0.100



P001A

SO-14 MECHANICAL DATA

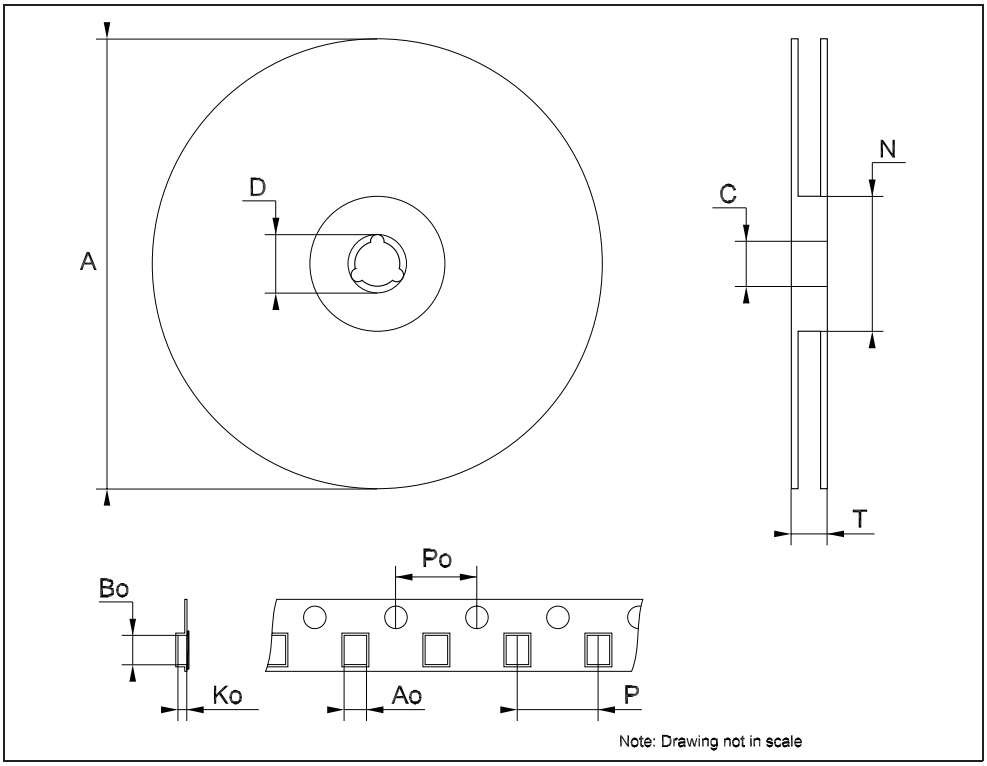
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	8.55		8.75	0.336		0.344
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		7.62			0.300	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.68			0.026
S	8° (max.)					



PO13G

Tape & Reel SO-14 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			22.4			0.882
Ao	6.4		6.6	0.252		0.260
Bo	9		9.2	0.354		0.362
Ko	2.1		2.3	0.082		0.090
Po	3.9		4.1	0.153		0.161
P	7.9		8.1	0.311		0.319



5 Revision history

Table 9. Document revision history

Date	Revision	Changes
July-2001	1	Initial release.
23-May-2008	2	Document converted and restructured to new template. Removed: M74HC04M1R and M74HCT04TTR order codes. Added: tape and reel specifications for SO-14 package.