

MC74VHC1GT125E

Noninverting Buffer / CMOS Logic Level Shifter with LSTTL-Compatible Inputs

The MC74VHC1GT125E is a single gate noninverting buffer fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The MC74VHC1GT125E requires the 3-state control input (\overline{OE}) to be set High to place the output into the high impedance state.

The device input is compatible with TTL-type input thresholds and the output has a full 5 V CMOS level output swing. The input protection circuitry on this device allows overvoltage tolerance on the input, allowing the device to be used as a logic-level translator from 3 V CMOS logic to 5 V CMOS Logic or from 1.8 V CMOS logic to 3 V CMOS Logic while operating at the high-voltage power supply.

The MC74VHC1GT125E input structure provides protection when voltages up to 5.5 V are applied, regardless of the supply voltage. This allows the MC74VHC1GT125E to be used to interface 5 V circuits to 3 V circuits. The output structures also provide protection when $V_{CC} = 0$ V. These input and output structures help prevent device destruction caused by supply voltage – input/output voltage mismatch, battery backup, hot insertion, etc.

Features

- High Speed: $t_{PD} = 3.5$ ns (Typ) at $V_{CC} = 5$ V
- Low Power Dissipation: $I_{CC} = 1$ μ A (Max) at $T_A = 25^\circ$ C
- TTL-Compatible Inputs: $V_{IL} = 0.8$ V; $V_{IH} = 2$ V
- CMOS-Compatible Outputs: $V_{OH} > 0.8 V_{CC}$; $V_{OL} < 0.1 V_{CC}$ @Load
- Power Down Protection Provided on Inputs and Outputs
- Balanced Propagation Delays
- Pin and Function Compatible with Other Standard Logic Families
- Chip Complexity: FETs = 62; Equivalent Gates = 16
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

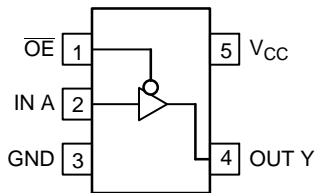


Figure 1. Pinout (Top View)



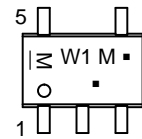
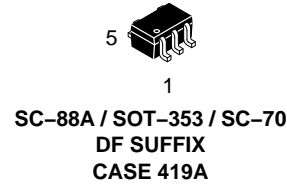
Figure 2. Logic Symbol



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MARKING DIAGRAMS



- W1 = Device Code
- M = Date Code*
- = Pb-Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

PIN ASSIGNMENT

Pin	Function
1	\overline{OE}
2	IN A
3	GND
4	OUT Y
5	V_{CC}

FUNCTION TABLE

A Input	\overline{OE} Input	Y Output
L	L	L
H	L	H
X	H	Z

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

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MAXIMUM RATINGS

Symbol	Characteristics	Value	Unit
V_{CC}	DC Supply Voltage	-0.5 to +6.5	V
V_{IN}	DC Input Voltage	-0.5 to +6.5	V
V_{OUT}	DC Output Voltage Tri-State Mode $V_{CC} = 0$ High or Low State	-0.5 to +6.5 -0.5 to +6.5 -0.5 to $V_{CC} + 0.5$	V
I_{IK}	Input Diode Current	-20	mA
I_{OK}	Output Diode Current $V_{OUT} < GND; V_{OUT} > V_{CC}$	+20	mA
I_{OUT}	DC Output Current, per Pin	+25	mA
I_{CC}	DC Supply Current, V_{CC} and GND	+50	mA
P_D	Power Dissipation in Still Air SC-88A	200	mW
θ_{JA}	Thermal Resistance SC-88A	333	°C/W
T_L	Lead Temperature, 1 mm from Case for 10 s	260	°C
T_J	Junction Temperature Under Bias	+150	°C
T_{stg}	Storage Temperature	-65 to +150	°C
V_{ESD}	ESD Withstand Voltage Human Body Model (Note 1) Charged Device Model (Note 2)	> 4000 > 1000	V
$I_{Latchup}$	Latchup Performance Above V_{CC} and Below GND at 125°C (Note 3)	±100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Tested to EIA/JESD22-A114-A
2. Tested to JESD22-C101-A
3. Tested to EIA/JESD78

RECOMMENDED OPERATING CONDITIONS

Symbol	Characteristics	Min	Max	Unit
V_{CC}	DC Supply Voltage	3.0	5.5	V
V_{IN}	DC Input Voltage	0.0	5.5	V
V_{OUT}	DC Output Voltage	0.0	V_{CC}	V
T_A	Operating Temperature Range	-55	+125	°C
t_r, t_f	Input Rise and Fall Time $V_{CC} = 5.0 V \pm 0.5 V$	0	5	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

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DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V _{CC} (V)	T _A = 25°C			T _A ≤ 85°C		-55 ≤ T _A ≤ 125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
V _{IH}	Minimum High-Level Input Voltage		3.0	1.4			1.4		1.4		V
			4.5	2.0			2.0		2.0		
			5.5	2.0			2.0		2.0		
V _{IL}	Maximum Low-Level Input Voltage		3.0							0.53	V
			4.5							0.8	
			5.5							0.8	
V _{OH}	Minimum High-Level Output Voltage V _{IN} = V _{IH} or V _{IL}	V _{IN} = V _{IH} or V _{IL} I _{OH} = -50 μA	3.0	2.9	3.0		2.9		2.9		V
			4.5	4.4	4.5		4.4		4.4		
		V _{IN} = V _{IH} or V _{IL} I _{OH} = -4 mA I _{OH} = -8 mA	3.0	2.58			2.48		2.34		
			4.5	3.94			3.80		3.66		
V _{OL}	Maximum Low-Level Output Voltage V _{IN} = V _{IH} or V _{IL}	V _{IN} = V _{IH} or V _{IL} I _{OL} = 50 μA	3.0		0.0	0.1		0.1		0.1	V
			4.5		0.0	0.1		0.1		0.1	
		V _{IN} = V _{IH} or V _{IL} I _{OL} = 4 mA I _{OL} = 8 mA	3.0			0.36		0.44		0.52	
			4.5			0.36		0.44		0.52	
I _{IN}	Maximum Input Leakage Current	V _{IN} = 5.5 V or GND	0 to 5.5			±0.10		±1.0		±1.0	μA
I _{CC}	Maximum Quiescent Supply Current	V _{IN} = V _{CC} or GND	5.5			1.0		20		40	μA
I _{CC(T)}	Additional Quiescent Supply Current per Input Pin	Input: V _{IN} = 3.4 V Other Input: V _{CC} or GND	5.5			1.35		1.50		1.65	mA
I _{OPD}	Power Off Output Leakage Current	V _{OUT} = 5.5 V	0.0			0.5		5.0		10	μA
I _{OZ}	Maximum 3-State Leakage Current	V _{IN} = V _{IH} or V _{IL} V _{OUT} = V _{CC} or GND	5.5			±0.25		±2.5		±2.5	μA

AC ELECTRICAL CHARACTERISTICS Input t_r = t_f = 3.0 ns

Symbol	Parameter	Test Conditions	T _A = 25°C			T _A ≤ 85°C		-55 ≤ T _A ≤ 125°C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, A to Y (Figure 5)	V _{CC} = 3.3 ± 0.3 V C _L = 15pF		5.6	8.0		9.5		12.0	ns
		V _{CC} = 5.0 ± 0.5 V C _L = 50pF		8.1	11.5		13.0		16.0	
t _{PZL} , t _{PZH}	Maximum Output Enable Time, OE to Y (Figures 3 and 4)	V _{CC} = 3.3 ± 0.3 V C _L = 15pF		5.4	8.0		9.5		11.5	ns
		V _{CC} = 5.0 ± 0.5 V C _L = 50pF		7.9	11.5		13.0		15.0	
t _{PLZ} , t _{PHZ}	Maximum Output Disable Time, OE to Y (Figures 3 and 4)	V _{CC} = 3.3 ± 0.3 V C _L = 15pF		6.5	9.7		11.5		14.5	ns
		V _{CC} = 5.0 ± 0.5 V C _L = 50pF		8.0	13.2		15.0		18.0	
C _{in}	Maximum Input Capacitance			4	10		10		10	pF
C _{out}	Maximum Three-State Output Capacitance (Output in High Impedance State)			6						pF
C _{PD}	Power Dissipation Capacitance (Note 4)	Typical @ 25°C, V_{CC} = 5.0 V								
		14								pF

4. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC(OPR)} = C_{PD} • V_{CC} • f_{in} + I_{CC}/4 (per buffer). C_{PD} is used to determine the no-load dynamic power consumption; P_D = C_{PD} • V_{CC}² • f_{in} + I_{CC} • V_{CC}.

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SWITCHING WAVEFORMS

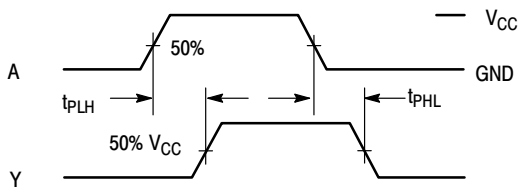


Figure 3. Switching Waveforms

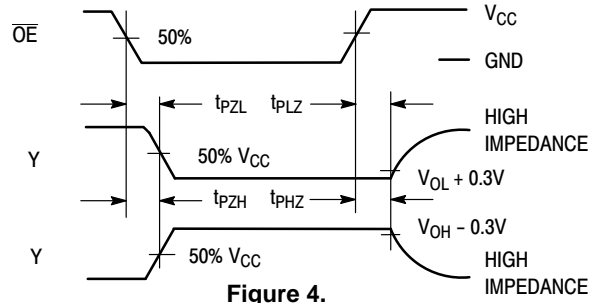
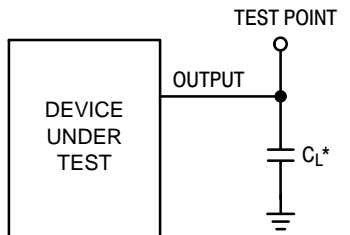
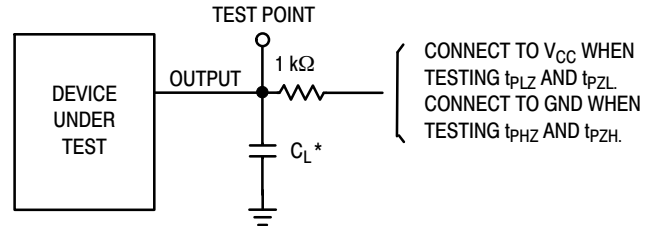


Figure 4.



*Includes all probe and jig capacitance

Figure 5. Test Circuit



*Includes all probe and jig capacitance

Figure 6. Test Circuit

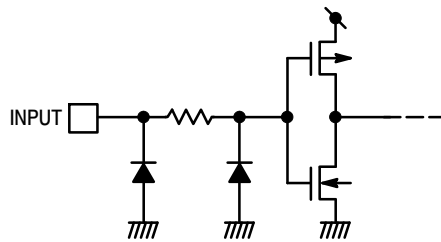


Figure 7. Input Equivalent Circuit

ORDERING INFORMATION

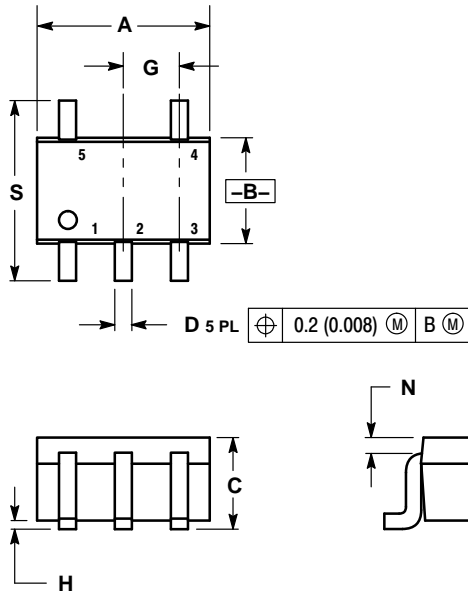
Device	Package	Shipping†
MC74VHC1GT125EDFT2G	SC-88A / SOT-353 / SC-70 (Pb-Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MC74VHC1GT125E

PACKAGE DIMENSIONS

SC-88A (SC-70-5/SOT-353)
CASE 419A-02
ISSUE L

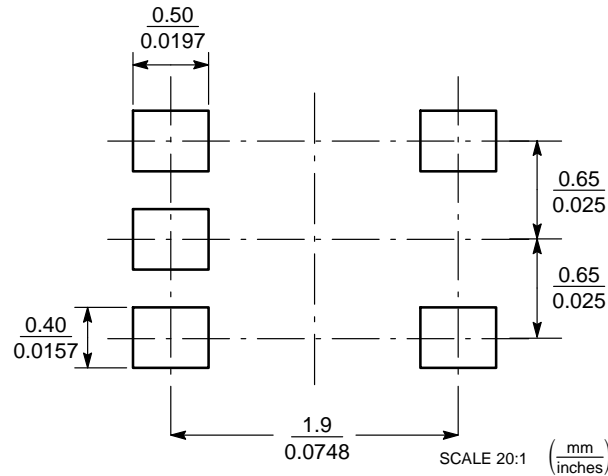


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 419A-01 OBSOLETE. NEW STANDARD 419A-02.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.071	0.087	1.80	2.20
B	0.045	0.053	1.15	1.35
C	0.031	0.043	0.80	1.10
D	0.004	0.012	0.10	0.30
G	0.026 BSC		0.65 BSC	
H	---	0.004	---	0.10
J	0.004	0.010	0.10	0.25
K	0.004	0.012	0.10	0.30
N	0.008 REF		0.20 REF	
S	0.079	0.087	2.00	2.20

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