FAIRCHILD SEMICONDUCTOR®

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74VCXH162373
Low Voltage 16-Bit Transparent Latch with Bushold and 26Ω Series Resistors in Outputs

General Description

The VCXH162373 contains sixteen non-inverting latches with 3-STATE outputs and is intended for bus oriented applications. The device is byte controlled. The flip-flops appear to be transparent to the data when the Latch enable (LE) is HIGH. When LE is LOW, the data that meets the setup time is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH, the outputs are in a high impedance state.

The VCXH162373 data inputs include active bushold circuitry, eliminating the need for external pull-up resistors to hold unused or floating data inputs at a valid logic level.

The VCXH162373 is also designed with 26Ω series resistors in the outputs. This design reduces line noise in applications such as memory address driver, clock drivers and bus transceivers/transmitters.

The 74VCXH162373 is designed for low voltage (1.4V to 3.6V) V_{CC} applications with output compatibility up to 3.6V.

The 74VCXH162373 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining low CMOS power dissipation.

Features

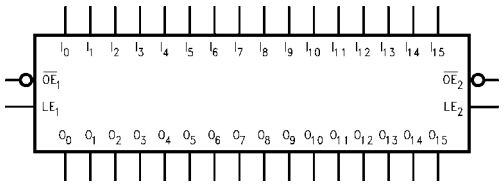
- 1.4V to 3.6V V_{CC} supply operation
- 3.6V tolerant control inputs and outputs
- Bushold on data inputs eliminates the need for external pull-up/pull-down resistors
- 26Ω series resistors in outputs
- t_{PD} (I_n to O_n)
  3.3 ns max for 3.0V to 3.6V V_{CC}
- Static Drive (I_{OH}/I_{OL})
  ±12 mA @ 3.0V V_{CC}
- Uses patented noise/EMI reduction circuitry
- Latch-up performance exceeds 300 mA
- ESD performance:
  Human body model > 2000V
  Machine model > 200V

Ordering Code:

Ordering Number	Package Number	Package Description
74VCXH162373MTD	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide [TUBES]
74VCXH162373MTX (Note 1)	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide [TAPE and REEL]

Note 1: Use this Order Number to receive devices in Tape and Reel.

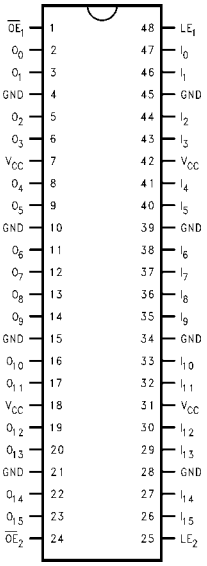
Logic Symbol



Pin Descriptions

Pin Names	Description
$\overline{OE}_n$	Output Enable Input (Active LOW)
LE_n	Latch Enable Input
I_0–I_{15}	Bushold Inputs
O_0–O_{15}	Outputs

Connection Diagram



Truth Tables

Inputs			Outputs
LE_1	$\overline{OE}_1$	I_0–I_7	O_0–O_7
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	O_0

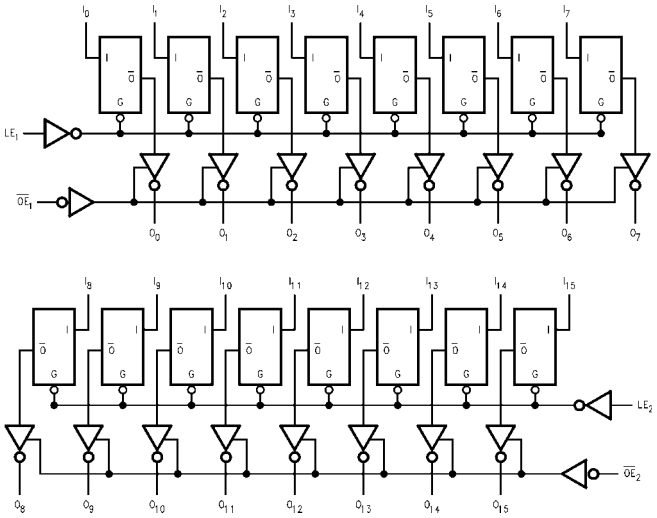
Inputs			Outputs
LE_2	$\overline{OE}_2$	I_8–I_{15}	O_8–O_{15}
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	O_0

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial (HIGH or LOW, control inputs may not float)
Z = High Impedance
O_0 = Previous O_0 before HIGH-to-LOW of Latch Enable

Functional Description

The 74VCXH162373 contains sixteen edge D-type latches with 3-STATE outputs. The device is byte controlled with each byte functioning identically, but independent of the other. Control pins can be shorted together to obtain full 16-bit operation. The following description applies to each byte. When the Latch Enable (LE_n) input is HIGH, data on the I_n enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its I input changes. When LE_n is LOW, the latches store information that was present on the I inputs a setup time preceding the HIGH-to-LOW transition on LE_n. The 3-STATE outputs are controlled by the Output Enable ($\overline{OE}_n$) input. When $\overline{OE}_n$ is LOW the standard outputs are in the 2-state mode. When $\overline{OE}_n$ is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the latches.

Logic Diagrams



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 2)

Supply Voltage (V_{CC})	−0.5V to +4.6V
DC Input Voltage (V_I)	−0.5V to 4.6V
Output Voltage (V_O)	
Outputs 3-STATED	−0.5V to +4.6V
Outputs Active (Note 3)	−0.5V to V_{CC} +0.5V
DC Input Diode Current (I_{IK}) V_I < 0V	−50 mA
DC Output Diode Current (I_{OK})	
V_O < 0V	−50 mA
V_O > V_{CC}	+50 mA
DC Output Source/Sink Current	
(I_{OH}/I_{OL})	±50 mA
DC V_{CC} or GND Current per	
Supply Pin (I_{CC} or GND)	±100 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C

Recommended Operating Conditions (Note 4)

Power Supply	
Operating	1.4V to 3.6V
Input Voltage	−0.3V to V_{CC}
Output Voltage (V_O)	
Output in Active States	0V to V_{CC}
Output in 3-STATE	0.0V to 3.6V
Output Current in I_{OH}/I_{OL}	
V_{CC} = 3.0V to 3.6V	±12 mA
V_{CC} = 2.3V to 2.7V	±8 mA
V_{CC} = 1.65V to 2.3V	±3 mA
V_{CC} = 1.4V to 1.6V	±1 mA
Free Air Operating Temperature (T_A)	−40°C to +85°C
Minimum Input Edge Rate ($\Delta t/\Delta V$)	
V_{IN} = 0.8V to 2.0V, V_{CC} = 3.0V	10 ns/V

Note 2: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 3: I_O Absolute Maximum Rating must be observed.

Note 4: Floating or unused control inputs must be held HIGH or LOW.

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	Min	Max	Units
V_{IH}	HIGH Level Input Voltage		2.7 - 3.6	2.0		V
			2.3 - 2.7	1.6		
			1.65 - 2.3	0.65 x V_{CC}		
			1.4 - 1.6	0.65 x V_{CC}		
V_{IL}	LOW Level Input Voltage		2.7 - 3.6		0.8	V
			2.3 - 2.7		0.7	
			1.65 - 2.3		0.35 x V_{CC}	
			1.4 - 1.6		0.35 x V_{CC}	
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 μA	2.7 - 3.6	V_{CC} - 0.2		V
		I_{OH} = −6 mA	2.7	2.2		
		I_{OH} = −8 mA	3.0	2.4		
		I_{OH} = −12 mA	3.0	2.2		
		I_{OH} = −100 μA	2.7 - 3.6	V_{CC} - 0.2		
		I_{OH} = −4 mA	2.3	2.0		
		I_{OH} = −6 mA	2.3	1.8		
		I_{OH} = −8 mA	2.3	1.7		
		I_{OH} = −100 μA	1.65 - 2.3	V_{CC} - 0.2		
		I_{OH} = −3 mA	1.65	1.25		
		I_{OH} = −100 μA	1.4 - 1.6	V_{CC} - 0.2		
		I_{OH} = −1 mA	1.4	1.05		

DC Electrical Characteristics (Continued)

Symbol	Parameter		Conditions	V_{CC} (V)	Min	Max	Units
V_{OL}	LOW Level Output Voltage		I_{OL} = 100 μA	2.7 - 3.6		0.2	V
			I_{OL} = 6 mA	2.7		0.4	
			I_{OL} = 8 mA	3.0		0.55	
			I_{OL} = 12 mA	3.0		0.8	
			I_{OL} = 100 μA	2.3 - 2.7		0.2	
			I_{OL} = 6 mA	2.3		0.4	
			I_{OL} = 8 mA	2.3		0.6	
			I_{OL} = 100 μA	1.65 - 2.3		0.2	
			I_{OL} = 3 mA	1.65		0.3	
			I_{OL} = 100 μA	1.4 - 1.6		0.2	
			I_{OL} = 1 mA	1.4		0.35	
I_I	Input Leakage Current	Control Pins	0 ≤ V_I ≤ 3.6V	1.4 - 3.6		±5.0	μA
		Data Pins	V_I = V_{CC} or GND	1.4 - 3.6		±5.0	μA
$I_{I(HOLD)}$	Bushold Input Minimum Drive Hold Current		V_{IN} = 0.8V	3.0	75		μA
			V_{IN} = 2.0V	3.0	−75		
			V_{IN} = 0.7V	2.3	45		
			V_{IN} = 1.6V	2.3	−45		
			V_{IN} = 0.57V	1.65	25		
			V_{IN} = 1.07V	1.65	−25		
$I_{I(OD)}$	Bushold Input Over-Drive Current to Change State		(Note 5)	3.6	450		μA
			(Note 6)	3.6	−450		
			(Note 5)	2.7	300		
			(Note 6)	2.7	−300		
			(Note 5)	1.95	200		
			(Note 6)	1.95	−200		
I_{OZ}	3-STATE Output Leakage		0 ≤ V_O ≤ 3.6V V_I = V_{IH} or V_{IL}	1.4 - 3.6		±10	μA
I_{OFF}	Power-OFF Leakage Current		0 ≤ (V_O) ≤ 3.6V	0		10	μA
I_{CC}	Quiescent Supply Current		V_I = V_{CC} or GND	1.4 - 3.6		20	μA
			V_{CC} ≤ (V_O) ≤ 3.6V (Note 7)	1.4 - 3.6		±20	
ΔI_{CC}	Increase in I_{CC} per Input		V_{IH} = V_{CC} −0.6V	2.7 - 3.6		750	μA

Note 5: An external driver must source at least the specified current to switch from LOW-to-HIGH.

Note 6: An external driver must sink at least the specified current to switch from HIGH-to-LOW.

Note 7: Outputs disabled or 3-STATE only.

AC Electrical Characteristics (Note 8)

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = -40°C$ to $+85°C$		Units	Figure Number
				Min	Max		
t_{PHL} t_{PLH}	Propagation Delay I_n to O_n	$C_L = 30$ pF, $R_L = 500\Omega$	3.3 ± 0.3	0.8	3.3	ns	Figures 1, 2
			2.5 ± 0.2	1.0	4.5		
			1.8 ± 0.15	1.5	9.0		
		$C_L = 30$ pF, $R_L = 2k\Omega$	1.5 ± 0.1	1.0	18.0		Figures 7, 8
t_{PHL} t_{PLH}	Propagation Delay LE to O_n	$C_L = 30$ pF, $R_L = 500\Omega$	3.3 ± 0.3	0.8	3.6	ns	Figures 1, 2
			2.5 ± 0.2	1.0	4.9		
			1.8 ± 0.15	1.5	9.8		
		$C_L = 30$ pF, $R_L = 500\Omega$	1.5 ± 0.1	1.0	19.6		Figures 7, 8
t_{PZL} t_{PZH}	Output Enable Time	$C_L = 30$ pF, $R_L = 500\Omega$	3.3 ± 0.3	0.8	3.9	ns	Figures 1, 3, 4
			2.5 ± 0.2	1.0	5.4		
			1.8 ± 0.15	1.5	9.8		
		$C_L = 30$ pF, $R_L = 2k\Omega$	1.5 ± 0.1	1.0	19.6		Figures 7, 9, 10
t_{PLZ} t_{PHZ}	Output Disable Time	$C_L = 30$ pF, $R_L = 500\Omega$	3.3 ± 0.3	0.8	4.0	ns	Figures 1, 3, 4
			2.5 ± 0.2	1.0	4.4		
			1.8 ± 0.15	1.5	7.9		
		$C_L = 30$ pF, $R_L = 2k\Omega$	1.5 ± 0.1	1.0	15.8		Figures 7, 9, 10
t_S	Setup Time	$C_L = 30$ pF, $R_L = 500\Omega$	3.3 ± 0.3	1.5		ns	Figure 6
			2.5 ± 0.2	1.5			
			1.8 ± 0.15	2.5			
		$C_L = 30$ pF, $R_L = 500\Omega$	1.5 ± 0.1	3.0			
t_H	Hold Time	$C_L = 30$ pF, $R_L = 500\Omega$	3.3 ± 0.3	1.0		ns	Figure 6
			2.5 ± 0.2	1.0			
			1.8 ± 0.15	1.0			
		$C_L = 30$ pF, $R_L = 500\Omega$	1.5 ± 0.1	2.0			
t_W	Pulse Width	$C_L = 30$ pF, $R_L = 500\Omega$	3.3 ± 0.3	1.5		ns	Figure 5
			2.5 ± 0.2	1.5			
			1.8 ± 0.15	4.0			
		$C_L = 30$ pF, $R_L = 500\Omega$	1.5 ± 0.1	4.0			
t_{OSHL} t_{OSLH}	Output to Output Skew (Note 9)	$C_L = 30$ pF, $R_L = 500\Omega$	3.3 ± 0.3		0.5	ns	
			2.5 ± 0.2		0.5		
			1.8 ± 0.15		0.75		
		$C_L = 30$ pF, $R_L = 2k\Omega$	1.5 ± 0.1		1.5		

Note 8: For $C_L = 50$pF, add approximately 300 ps to the AC maximum specification.

Note 9: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}).

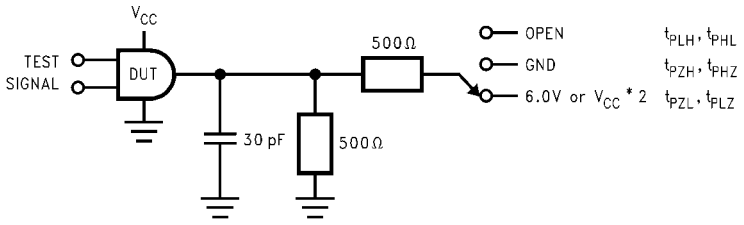
Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = +25°C$ Typical	Units
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	C_L = 30 pF, $V_{IH} = V_{CC}$, V_{IL} = 0V	1.8	0.15	
			2.5	0.25	V
			3.3	0.35	
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	C_L = 30 pF, $V_{IH} = V_{CC}$, V_{IL} = 0V	1.8	−0.15	
			2.5	−0.25	V
			3.3	−0.35	
V_{OHV}	Quiet Output Dynamic Valley V_{OH}	C_L = 30 pF, $V_{IH} = V_{CC}$, V_{IL} = 0V	1.8	1.55	
			2.5	2.05	V
			3.3	2.65	

Capacitance

Symbol	Parameter	Conditions	$T_A = +25°C$ Typical	Units
C_{IN}	Input Capacitance	V_{CC} = 1.8V, 2.5V or 3.3V, V_I = 0V or V_{CC}	6	pF
C_{OUT}	Output Capacitance	V_I = 0V or V_{CC}, V_{CC} = 1.8V, 2.5V or 3.3V	7	pF
C_{PD}	Power Dissipation Capacitance	V_I = 0V or V_{CC}, f = 10 MHz, V_{CC} = 1.8V, 2.5V or 3.3V	20	pF

AC Loading and Waveforms (V_{CC} 3.3V ± 0.3V to 1.8V ± 0.15V)



TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	6V at V_{CC} = 3.V3 ± 0.3V; V_{CC} x 2 at V_{CC} = 2.V5 ± 0.2V; 1.8V ± 0.15V
t_{PZH}, t_{PHZ}	GND

FIGURE 1. AC Test Circuit

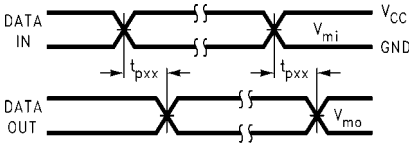


FIGURE 2. Waveform for Inverting and Non-Inverting Functions

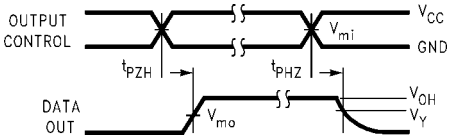


FIGURE 3. 3-STATE Output HIGH Enable and Disable Times for Low Voltage Logic

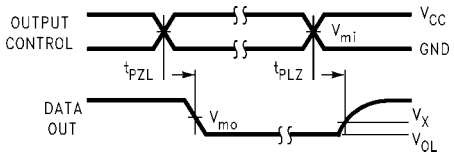


FIGURE 4. 3-STATE Output LOW Enable and Disable Times for Low Voltage Logic

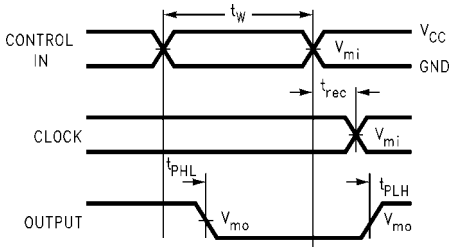


FIGURE 5. Propagation Delay, Pulse Width and t_{REC} Waveforms

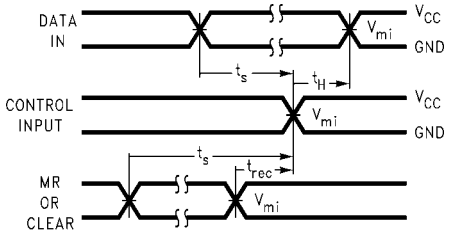
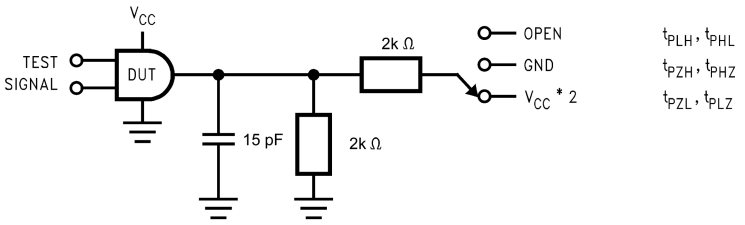


FIGURE 6. Setup Time, Hold Time and Recovery Time for Low Voltage Logic

Symbol	V_{CC}		
	3.3V ± 0.3V	**2.5V ± 0.2V**	**1.8V ± 0.15V**
V_{mi}	1.5V	V_{CC}/2	V_{CC}/2
V_{mo}	1.5V	V_{CC}/2	V_{CC}/2
V_X	V_{OL} +0.3V	V_{OL} +0.15V	V_{OL} +0.15V
V_Y	V_{OH} −0.3V	V_{OH} −0.15V	V_{OH} −0.15V

AC Loading and Waveforms (V_{CC} 1.5V ± 0.1V)



TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	V_{CC} x 2 at V_{CC} = 1.5 ± 0.1V
t_{PZH}, t_{PHZ}	GND

FIGURE 7. AC Test Circuit

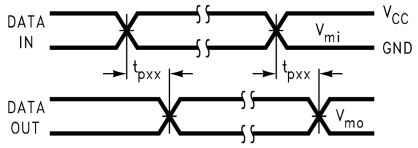


FIGURE 8. Waveform for Inverting and Non-Inverting Functions

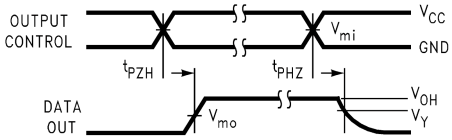


FIGURE 9. 3-STATE Output HIGH Enable and Disable Times for Low Voltage Logic

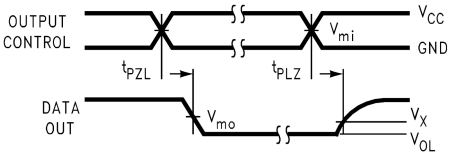
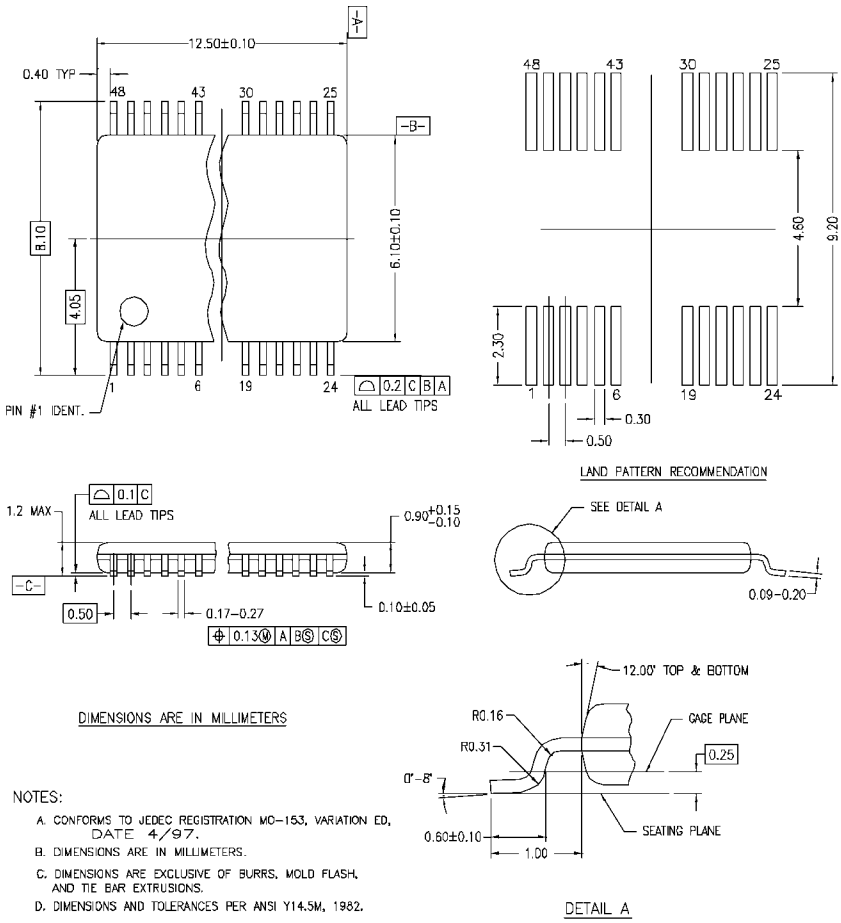


FIGURE 10. 3-STATE Output LOW Enable and Disable Times for Low Voltage Logic

Symbol	V_{CC}
	1.5V ± 0.1V
V_{mi}	V_{CC}/2
V_{mo}	V_{CC}/2
V_X	V_{OL} +0.1V
V_Y	V_{OH} −0.1V

Physical Dimensions inches (millimeters) unless otherwise noted



48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD48

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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