MT29F64G08CBAAAL74A3WC1P

Data Sheets (1)

Die Data Sheet

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MT29F64G08CBAAAL74A3WC1P

Orderable Part Information

Status	Contact Factory	**Alternative Part**	view
FBGA Code	N/A	**SPD Data**	N/A
MBQual Data	N/A	**Shipping Media**	N/A
PLP	No	**Start Date**	N/A

Specs

Density	64Gb	**Status**	Contact Factory
RoHS	Yes	**Width**	x8
Voltage	3.3V	**Package**	Wafer
Pin Count	n/a	**MT/s**	
I/O	Common	**Product Name**	

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FAQs

- Do you support small block devices?
- How much ECC do I need to support your devices?
- I am using the correct amount of error correction code (ECC) for the NAND device, but I'm still seeing bit/byte errors in data I read back from the NAND device.
- See all FAQs

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MLC NAND FAQs (3)

Do you support small block devices?
How much ECC do I need to support your devices?
I am using the correct amount of error correction code (ECC) for the NAND device, but I'm still seeing bit/byte errors in data I read back from the NAND device.

NAND Flash FAQs (15)

How do I achieve greater PROGRAM/READ throughput for the NAND device?
How is Nvb specified?
I am seeing a lot of READ DISTURB errors. Can you tell me if there is a problem with your part?
I've heard that NAND has too many errors to boot from. Is this true?
Should I be marking blocks bad due to READ errors?
When I issue a Read ID command (90h) to a two-die NAND device, I get a device ID back that states it is a one-die NAND device.
Where can I find additional technical information about Micron NAND devices that is not covered in the device data sheets?
Where can I find simulation models for NAND Flash devices?
Why am I getting a bit/byte error reading back the information I programmed into the NAND device?
Why doesn't the NAND Flash device respond correctly to commands issued to it?
What is a "bank"?
What is the impedance tolerance of the driver in match-impedance mode relative to the expected value base on the perfect reference resistor connected to ZQ pin?
Does thermal information change for IT parts?
My design was based on a specification stating the JTAG was relative to VDD (1.8V), but now we've discovered that JTAG is actually relative to VDDQ (1.5V). It's a fairly significant board spin to change this; what do I risk by leaving the design as-is? I assume that the specification is still for VDDQ + 0.3V = 1.8V, but with CMOS parts there's no way I can guarantee that it won't swing past that on transitions.
Should the ECC memory chip share chip select and CKE signals with the other two main memory chips in our point-to-point application?

Products and Support FAQs (1)

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