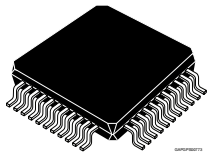
TDA7416

Car radio signal processor

Features

- 3 stereo inputs
- 1 pseudo differential stereo input
- Volume control
- 7 band equalizer filter control
- High-pass filter for subwoofer application
- Direct mute and soft mute
- 4 independent speaker outputs
- Soft-step speaker control
- Subwoofer output with soft step
- 7 band spectrum analyzer
- Full mixing capability
- HPF2 with ZeroCross
- I^2C bus interface



TQFP44

Table 1. Device summary

Order code	Package	Packing
E-TDA7416	TQFP44	Tray

Description

The device includes a high performance audio processor with 7 bands equalizer and spectrum analyzer.

The digital control allows a programming in a wide range of all the filter characteristics.

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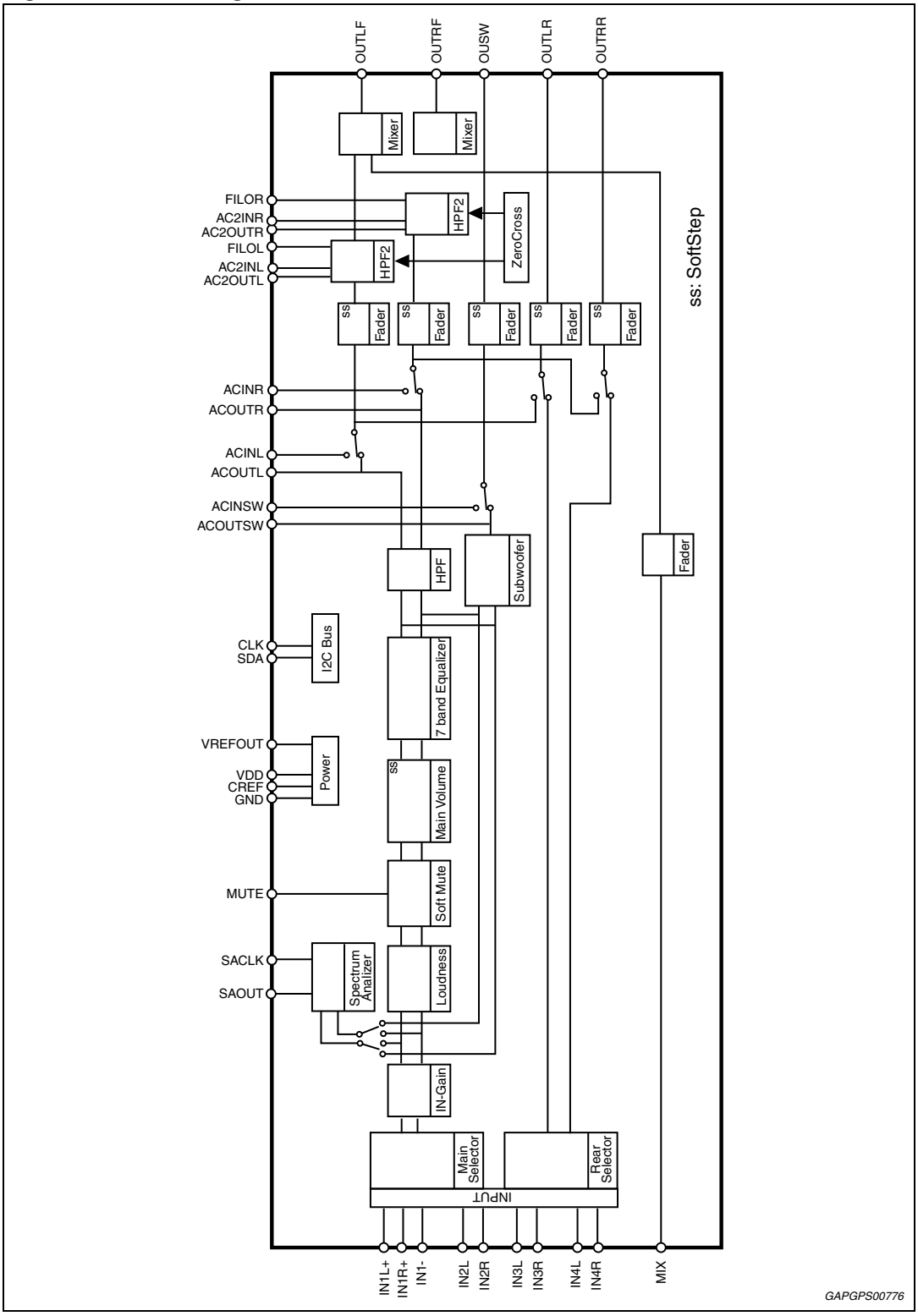
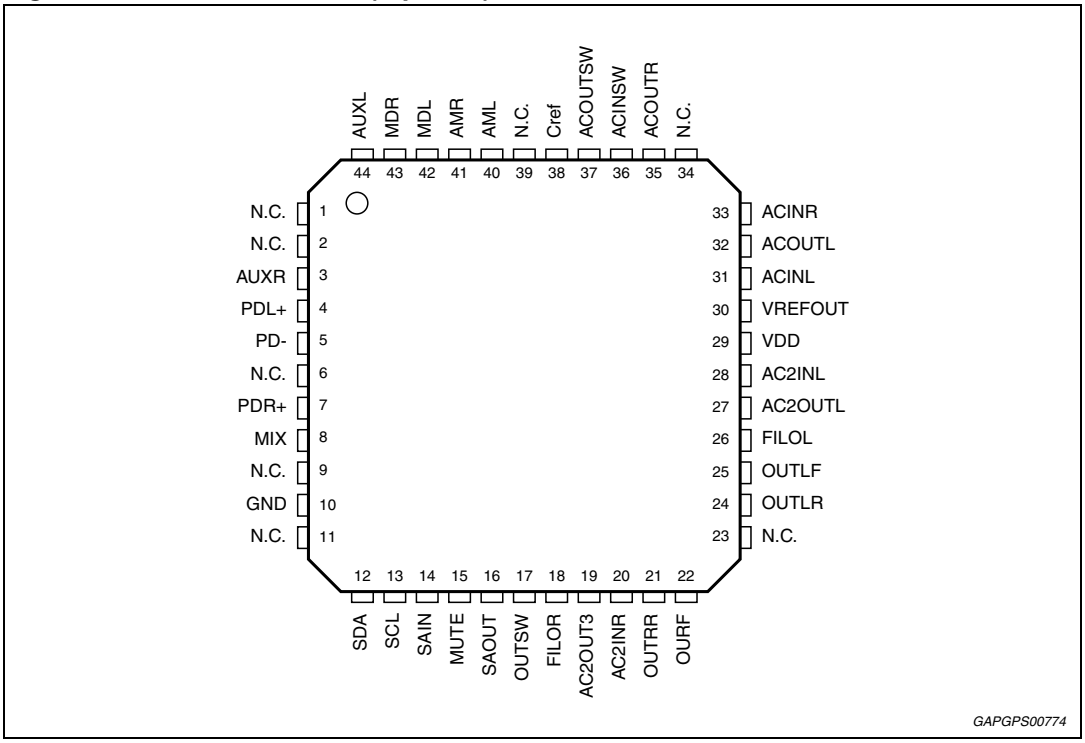
Figure 1. Block diagram



2 Pins connection

Figure 2. Pins connection (top view)



3 Electrical specifications

3.1 Supply

Table 2. Supply

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_S	Supply voltage		7.5	9	10	V
I_S	Supply current	V_S = 9 V	35	45	55	mA
SVRR	Ripple rejection @ 1kHz	Audio processor (all Filters flat)	-	60	-	dB

3.2 Thermal data

Table 3. Thermal data

Symbol	Description	Value	Unit
$R_{th\ j\text{-}pins}$	Thermal resistance junction-to-pins max	65	°C/W

3.3 Absolute maximum ratings

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_S	Operating supply voltage	10.5	V
T_{amb}	Operating temperature range	-40 to 85	°C
T_{stg}	Storage temperature range	-55 to +150	°C

3.4 ESD

All pins are protected against ESD according to the MIL883 standard.

3.5 Electrical characteristics

V_S = 9 V; T_{amb} = 25 °C; R_L = 10 kΩ; all gains = 0 dB; f = 1 kHz; unless otherwise specified.

Table 5. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Input selector						
R_{in}	Input resistance	All single-ended Inputs	70	100	130	kΩ
V_{CL}	Clipping level	-	1.8	2.2		V_{RMS}
S_{IN}	Input separation	-	80	100		dB
$G_{IN\ MIN}$	Min. input gain	-	-1	0	1	dB
$G_{IN\ MAX}$	Max. input gain	-	13	15	17	dB
G_{STEP}	Step resolution	-	0.5	1	1.5	dB
V_{DC}	DC steps	Adjacent gain steps	-5	1	5	mV
		G_{MIN} to G_{MAX}	-10	1	10	mV
V_{offset}	Remaining offset with AutoZero	-	-	0.5	-	mV
Differential stereo inputs						
R_{in}	Input resistance (see *Figure 3*)	Differential	70	100	130	kΩ
CMRR	Common mode rejection ratio	V_{CM} = 1 V_{RMS} @ 1 kHz	46	70	-	dB
		V_{CM} = 1 V_{RMS} @ 10 kHz	46	60	-	dB
e_{NO}	Output-noise @ speaker-outputs	20Hz - 20kHz, flat; all stages 0dB	-	11	-	µV
Mixing control						
M_{LEVEL}	Mixing ratio	Main / mix-source	-	-6/-6	-	dB
G_{MAX}	Max. gain	-	13	15	17	dB
A_{MAX}	Max. attenuation	-	-83	-79	-75	dB
A_{STEP}	Attenuation step	-	0.5	1	1.5	dB
Loudness control						
A_{STEP}	Step resolution	-	0.5	1	1.5	dB
A_{MAX}	Max. attenuation	-	-21	-19	-17	dB
f_{Peak}	Peak frequency	f_{P1}	180	200	220	Hz
		f_{P2}	360	400	440	Hz
		f_{P3}	540	600	660	Hz
		f_{P4}	720	800	880	Hz
Volume control						
G_{MAX}	Max. gain	-	18	20	22	dB
A_{MAX}	Max. attenuation	-	-83	-79	-75	dB
A_{STEP}	Step resolution	-	0	0.5	1	dB

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
E_A	Attenuation set error	G = -20 to +20 dB	-0.75	0	+0.75	dB
		G = -80 to -20 dB	-4	0	3	dB
E_T	Tracking error	-	-	-	2	dB
V_{DC}	DC steps	Adjacent attenuation steps	-	0.1	3	mV
		From 0dB to G_{MIN}	-	0.5	5	mV
Soft-mute						
A_{MUTE}	Mute attenuation	-	80	100	-	dB
T_D	Delay time	T1	-	0.48	1	ms
		T2	-	0.96	2	ms
		T3	70	123	170	ms
$V_{TH\ low}$	Low threshold for SM-Pin [1]	-	-	-	1	V
$V_{TH\ high}$	High threshold for SM - Pin	-	2.5	-	-	V
R_{PU}	Internal pull-up resistor	-	32	45	58	kΩ
V_{PU}	Internal pull-up Voltage	-	-	3.3	-	V
Equalizer control						
C_{RANGE}	Control range	-	±14	±15	±16	dB
A_{STEP}	Step resolution	-	0.5	1	1.5	dB
f_{C1}	Center frequency band 1	f_{C1a}	55	62	69	Hz
		f_{C1b}	90	100	110	Hz
f_{C2}	Center frequency band 2	f_{C2}	141	157	173	Hz
f_{C3}	Center frequency band 3	f_{C3}	365	396	437	Hz
f_{C4}	Center frequency band 4	f_{C4}	0.9	1	1.1	kHz
f_{C5}	Center frequency band 5	f_{C5}	2.25	2.51	2.76	kHz
f_{C6}	Center frequency band 6	f_{C6a}	3.6	4	4.4	kHz
		f_{C6b}	5.70	6.34	6.98	kHz
f_{C7}	Center frequency band 7	f_{C7a}	13.5	15	16.5	kHz
		f_{C7b}	14.4	16	17.6	kHz
Q	Quality factor	Q_1	0.9	1	1.1	
		Q_2	1.26	1.4	1.54	
		Q_3	1.62	1.8	1.98	
		Q_4	1.98	2.2	2.44	
DC_{GAIN}	DC-gain, Band 1	DC = off	-1	0	+1	dB
		DC = on, 15dB boost		4		dB

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Spectrum analyzer control						
V_{SAOut}	Output voltage range	-	0		3.3	V
f_{C1}	Center frequency band 1	f_{C1}	55	62	69	Hz
f_{C2}	Center frequency band 2	f_{C2}	141	157	173	Hz
f_{C3}	Center frequency band 3	f_{C3}	356	396	436	Hz
f_{C4}	Center frequency band 4	f_{C4}	0.9	1	1.1	kHz
f_{C5}	Center frequency band 5	f_{C5}	2.26	2.51	2.76	kHz
f_{C6}	Center frequency band 6	f_{C6}	5.70	6.34	6.98	kHz
f_{C7}	Center frequency band 7	f_{C7}	14.4	16	17.6	kHz
Q	Quality factor	Q_1	1.62	1.8	1.98	
		Q_2	3.15	3.5	3.85	
f_{SAClk}	Clock frequency	-	1	-	100	kHz
t_{SAdel}	Analog output delay time	-	2	-	-	µs
t_{repeat}	Spectrum analyzer repeat time	-	50	-	-	ms
t_{intres}	Internal reset time	-	-	3	-	ms
HPF2						
V_{TH}	Zero crossing threshold	-	-	±20	-	mV
E_{MAX}	Max. effect	-	-	22	-	dB
E_{MIN}	Min. effect	-	-	4	-	dB
E_{STEP}	Step resolution	-	1.5	2	2.5	dB
Speaker attenuators						
R_{in}	Input Impedance	-	35	50	65	kΩ
G_{MAX}	Max. gain	-	13	15	17	dB
A_{MAX}	Max. attenuation	-	-83	-79	-75	dB
A_{STEP}	Step resolution	-	0.5	1	1.5	dB
A_{MUTE}	Output mute attenuation	-	80	90	-	dB
E_E	Attenuation set error	-	-	-	3	dB
V_{DC}	DC steps	Adjacent Attenuation Steps	-	0.5	5	mV
M_R	Mixing ratio	$Signal/Mix_{In}$	-	50/50	-	%
Audio outputs						
V_{CLIP}	Clipping level	Thd=0.3%	1.8	2.2	-	V_{RMS}
R_L	Output load resistance	-	2	-	-	kΩ
C_L	Output load capacitance	-	-	-	10	nF
R_{OUT}	Output impedance	-	-	30	120	W

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{DC}	DC voltage level	-	4.3	4.5	4.7	V
High-pass						
f_{HP}	High-pass corner frequency	f_{HP1}	81	90	99	Hz
		f_{HP2}	122	135	148	Hz
		f_{HP3}	162	180	198	Hz
		f_{HP4}	194	215	236	Hz
Subwoofer attenuator						
R_{in}	Input impedance	-	35	50	65	kΩ
G_{MAX}	Max. gain	-	14	15	16	dB
A_{ATTN}	Max. attenuation	-	-83	-79	-75	dB
A_{STEP}	Step resolution	-	0.5	1	1.5	dB
A_{MUTE}	Output mute attenuation	-	80	90	-	dB
E_E	Attenuation set error		-	-	2	dB
V_{DC}	DC steps	Adjacent Attenuation Steps	-	1	5	mV
Subwoofer low-pass						
f_{LP}	Low-pass corner frequency	f_{LP1}	72	80	88	Hz
		f_{LP2}	108	120	132	Hz
		f_{LP3}	144	160	176	Hz
General						
e_{NO}	Output noise	BW = 20 Hz - 20 kHz output muted	-	3	15	µV
		BW = 20 Hz - 20 kHz all gains = 0dB single-ended inputs	-	15	20	µV µV
S/N	Signal-to-noise ratio	all gains = 0 dB flat; V_O = 2 V_{RMS}	-	103	-	dB
		All EQ-bands at +12dB; Q = 1.0 a-weighted; V_O = 2.6V_{RMS}	-	87	-	dB
d	Distortion	V_{IN} = 1V_{RMS}; all stages 0dB	-	0.01	0.1	%
		V_{OUT} = 1V_{RMS}; Bass & treble = 12dB	-	0.05	0.1	%
S_C	Channel separation left/right	-	80	90	-	dB

4 Description of the audio processor part

4.1 Audio processor features

- Input multiplexer
  - 1 pseudo differential CDC stereo input, programmable as single-ended input
  - 3 single-ended stereo inputs
  - Input gain adjust 0 to 15 dB with 1 dB steps
  - direct mute
  - internal offset-cancellation (AutoZero)
- Mixing stage
  - mixable mix input to Front speaker outputs
  - Input controls +15 to -79 dB with 1 dB steps
  - direct mute
  - Loudness
  - programmable center frequency and filter slope
  - 19 dB with 1dB steps
  - selectable flat-mode (constant attenuation)
- Volume
  - +32 to -79.5 dB with 0.5 dB step resolution
  - soft-step control with programmable blend times
  - 100 dB range
- Equalizer
  - seven bands
  - 2^{nd} order frequency response
  - center frequency programmable for lowest and highest filter
  - programmable quality factor in four steps for each filter
  - -15 to 15 dB range with 1dB resolution
- Spectrum analyzer
  - seven bandpass filters
  - 2^{nd} order frequency response
  - programmable quality factor for different visual appearance
  - analog output
  - controlled by external serial clock
- High-pass
  - 2^{nd} order butterworth high-pass with programmable cut-off frequency
  - selectable flat-mode
- Speaker
  - 4 independent soft-step speaker controls, +15 to -79 dB with 1 dB steps
  - mute
  - 4 independent programmable mix inputs with 50% mixing ratio
- Subwoofer

– single-ended monaural output

- independent soft-step level control +15 to -79 dB with 1 dB steps

Mute functions

– direct mute

– digitally controlled Soft-mute with 3 programmable mute-times

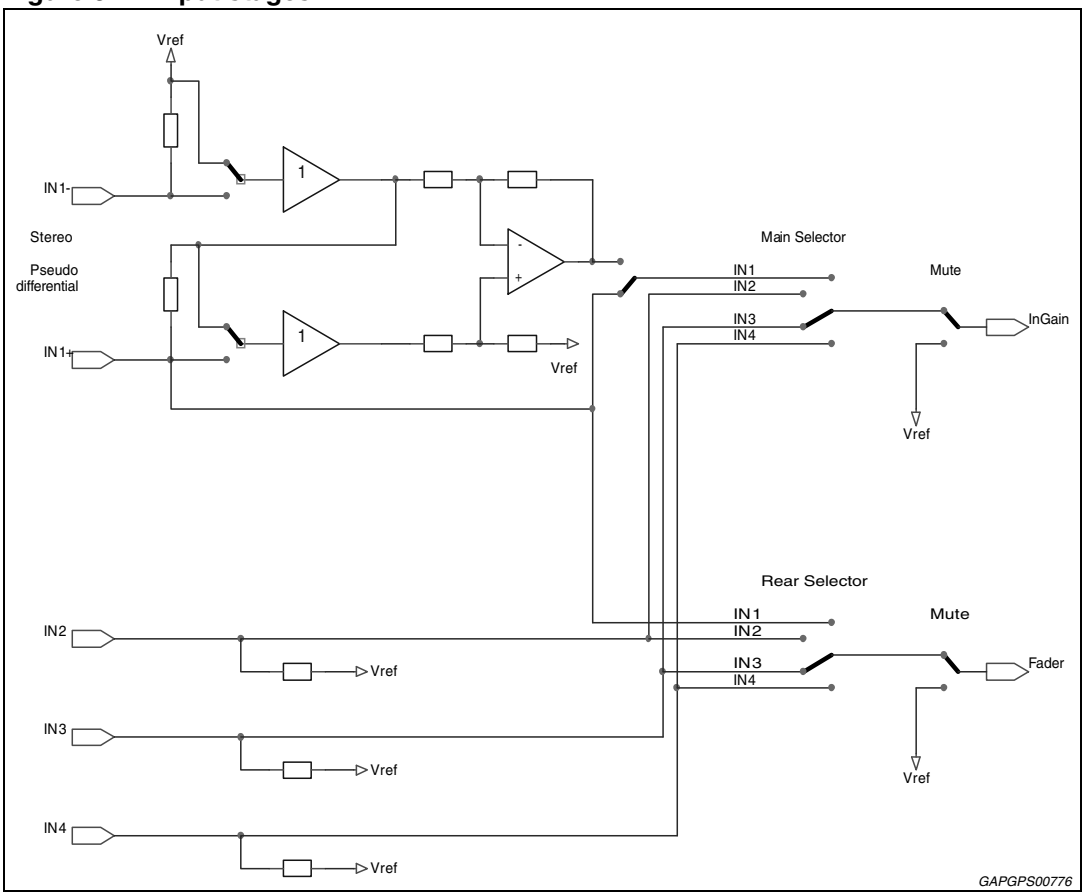
- Effect

– Gain effect or high-pass effect fixed external components

4.2 Input stages

In the basic configuration one pseudo-differential, three single-ended stereo are available.

Figure 3. Input stages



4.2.1 Pseudo-differential stereo input (IN1)

The IN1- input is implemented as a buffered pseudo-differential stereo stage with 100 kΩ input-impedance at each input pin. This input is also configurable as single-ended stereo input. The common input-pin, IN1- features a fast charge switch to speed up the charge time of external capacitors. This switch is released the first time the input-selector data-byte (0) is accessed.

4.2.2 Single-ended stereo inputs

All single-ended inputs have an input impedance of 100 kΩ.

4.3 AutoZero

The AutoZero allows a reduction of the number of pins as well as external components by canceling any offset generated by or before the In-Gain-stage (Please notice that externally generated offsets, e.g. generated through the leakage current of the coupling capacitors, are not canceled).

The auto-zeroing is started every time the DATA-BYTE 0 is selected and needs max. 0.3 ms for the alignment. To avoid audible clicks the Audioprocessor have to be muted by soft-mute or hard-mute during this time.

4.3.1 AutoZero remain

In some cases, for example if the µP is executing a refresh cycle of the IIC-Bus-programming, it is not useful to start a new AutoZero action because no new source is selected and an undesired mute would appear at the out-puts. For such applications the TDA7416 could be switched in the AutoZero remain-mode (Bit 6(I1) of the subaddress-byte). If this bit is set to high, the DATABYTE 0 could be loaded without invoking the AutoZero and the old adjustment-value remains.

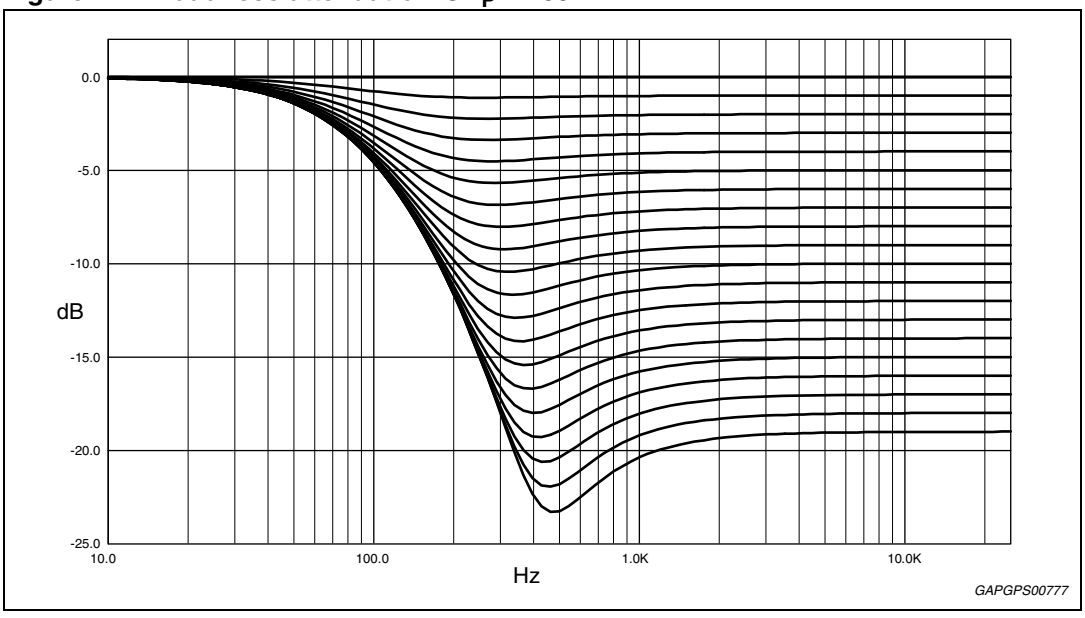
4.4 Loudness

There are four parameters programmable in the loudness stage.

4.4.1 Attenuation

Figure 4 shows the attenuation as a function of frequency at f_P = 400 Hz

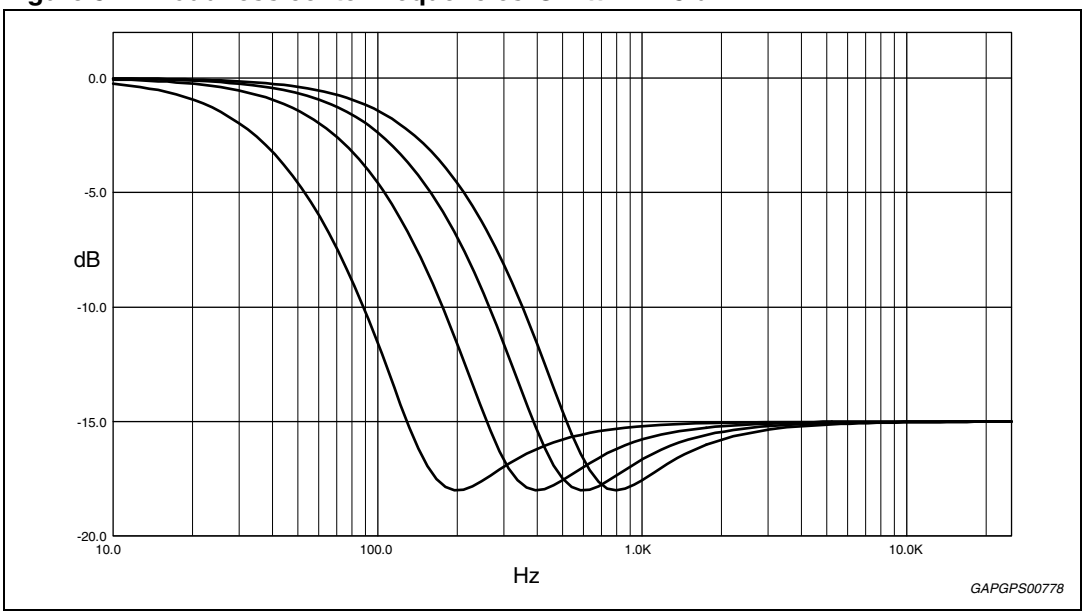
Figure 4. Loudness attenuation @ f_P = 400 Hz



4.4.2 Peak frequency

Figure 5 shows the four possible peak-frequencies at 200, 400, 600 and 800Hz

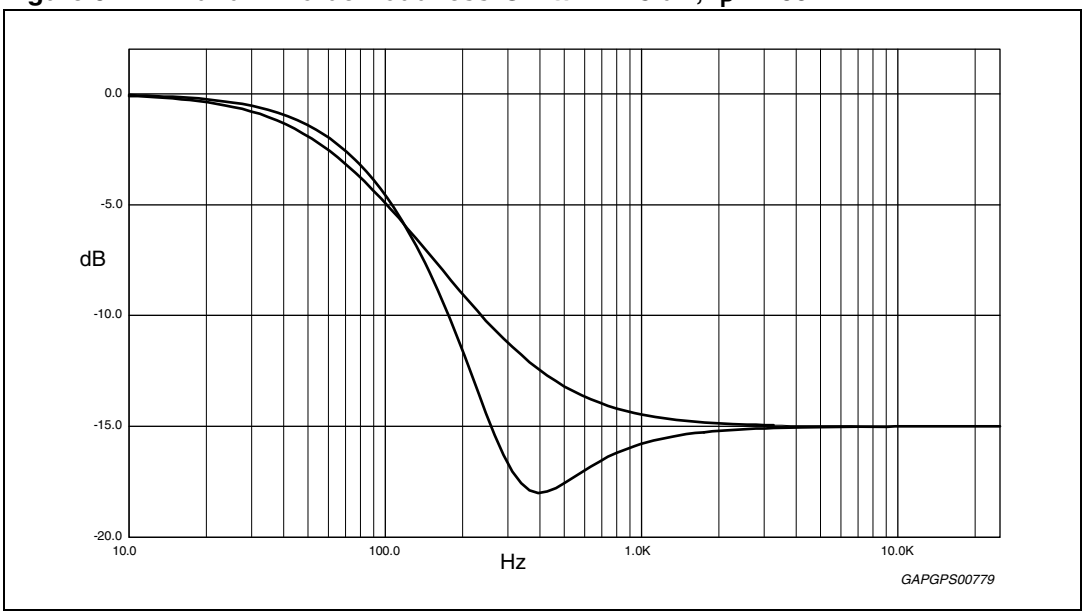
Figure 5. Loudness center frequencies @ Attn. = 15 dB



4.4.3 Loudness filter order

Different shapes of 1st and 2nd-order loudness

Figure 6. 1st and 2nd order loudness @ Attn. = 15 dB, f_P = 400 Hz



4.4.4 Flat mode

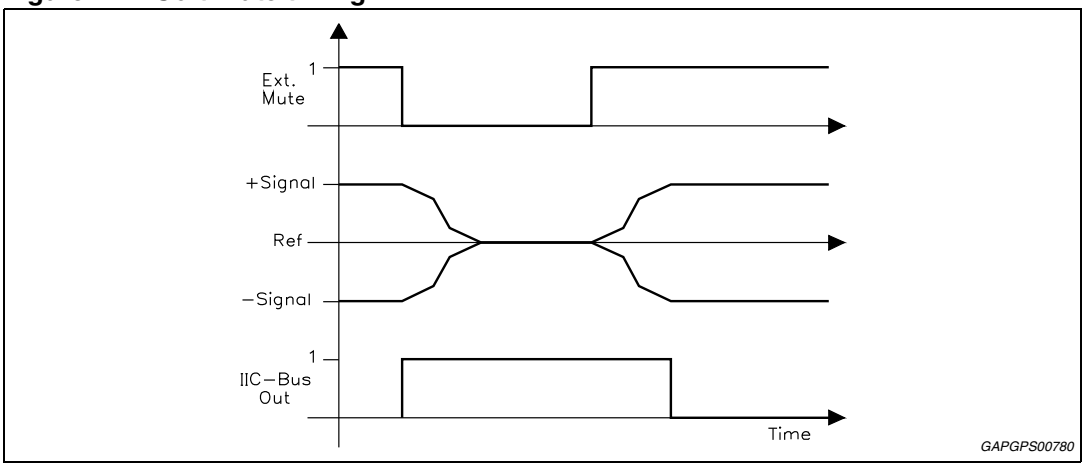
In flat mode the loudness stage works as a 0dB to -19dB attenuator.

4.5 Soft-mute

The digitally controlled soft-mute stage allows muting/demuting the signal with a I^2C bus programmable slope. The mute process can either be activated by the soft-mute pin or by the I^2C bus. This slope is realized in a special S-shaped curve to mute slow in the critical regions (see *Figure 7*).

For timing purposes the Bit0 of the I^2C bus output register is set to 1 from the start of muting until the end of de-muting.

Figure 7. Soft-mute timing

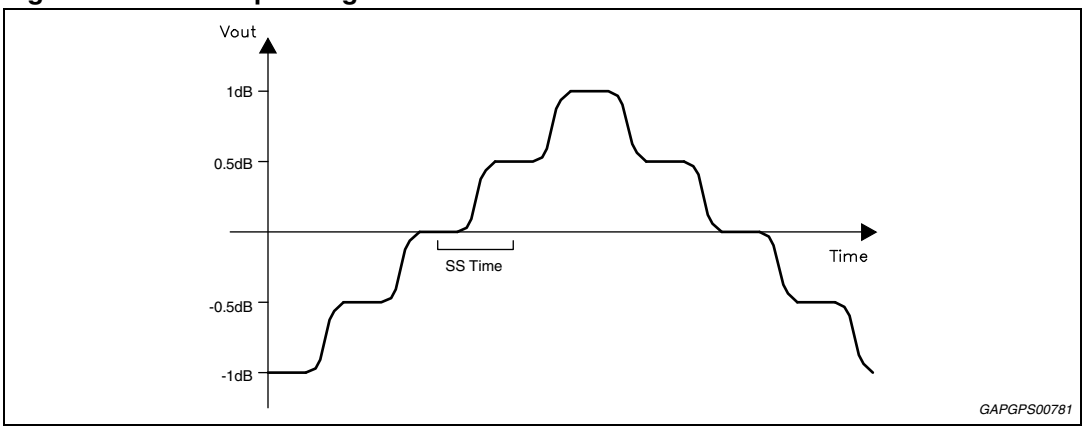


1. Please notice that a started Mute-action is always terminated and could not be interrupted by a change of the mute -signal.

4.6 Soft-step volume and speaker

When the speaker-level is changed audible clicks could appear at the output. The root cause of those clicks could either be a DC-Offset before the speaker-stage or the sudden change of the envelope of the audio signal. With the soft-step feature both kinds of clicks could be reduced to a minimum and are no more audible. The blend-time from one step to the next is programmable in four steps.

Figure 8. Soft-step timing for volume



1. For steps more than 0.5dB (Volume) or 1dB (Speaker) the soft-step mode should be deactivated because it could generate a hard 1dB step during blending.

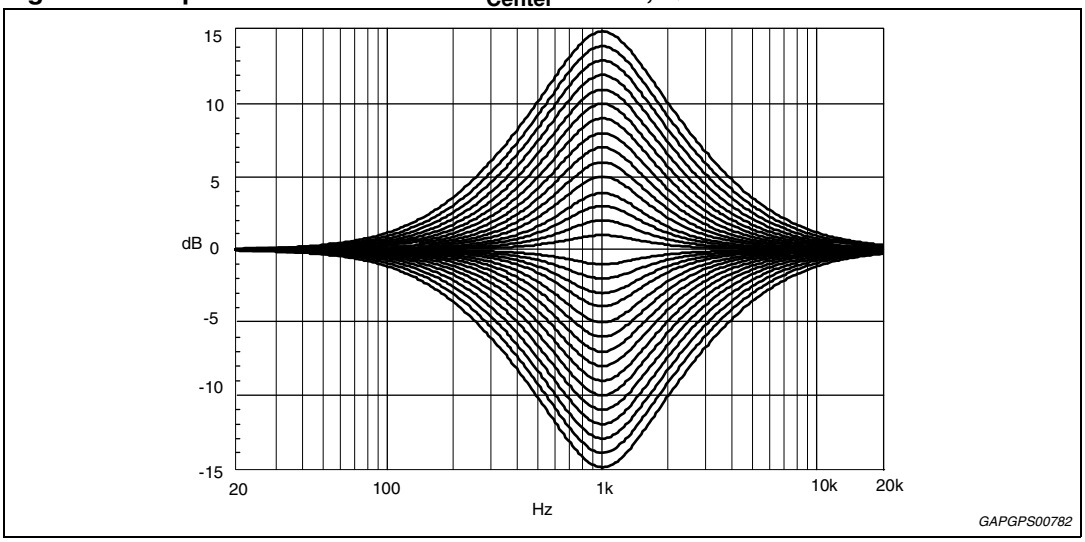
4.7 Equalizer filter

There are three parameters programmable in the equalizer filter:

4.7.1 Attenuation

Figure 9 shows the boost and cut response as a function of frequency at a center frequency of 1kHz.

Figure 9. Equalizer filter control @ f_{Center} = 1kHz, Q = 1.0

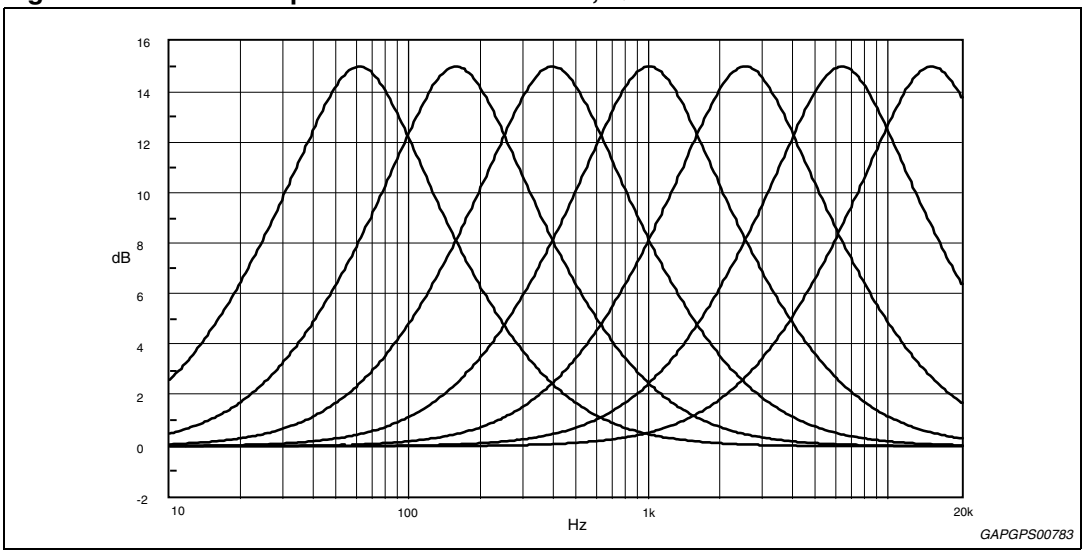


4.7.2 Center frequency

This parameter is programmable in the filter stage 1(62/100Hz), 6(4/6.34kHz) and 7(15/16kHz) only.

Figure 10 shows the center frequencies 62, 156, 396, 1000, 2510, 6340 and 15000 Hz of the 7 equalizer filters.

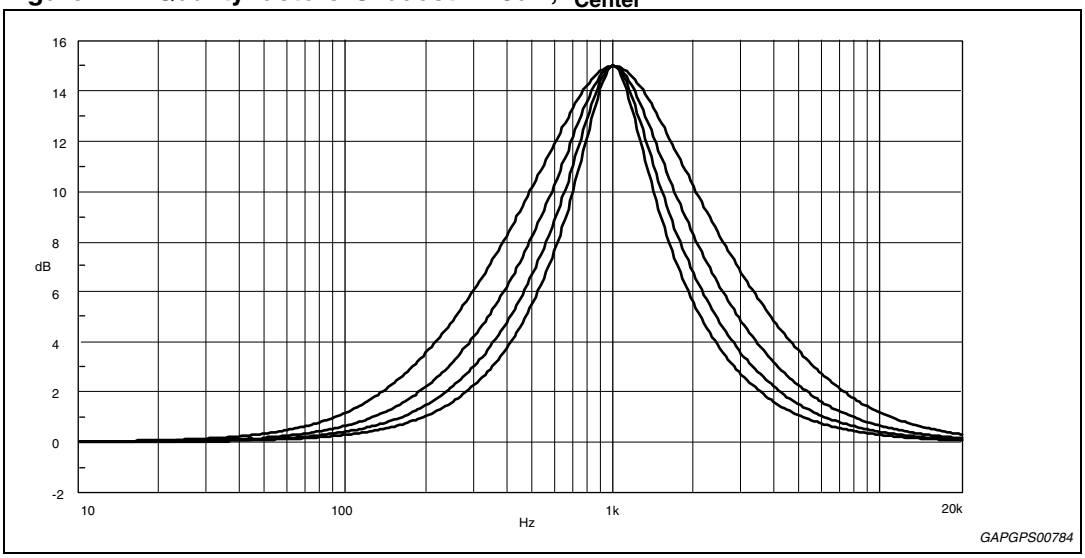
Figure 10. Center frequencies @ Gain = 15dB, Q = 1.0



4.7.3 Quality Factors

Figure 11 shows the four possible quality factors 1, 1.4, 1.8 and 2.2

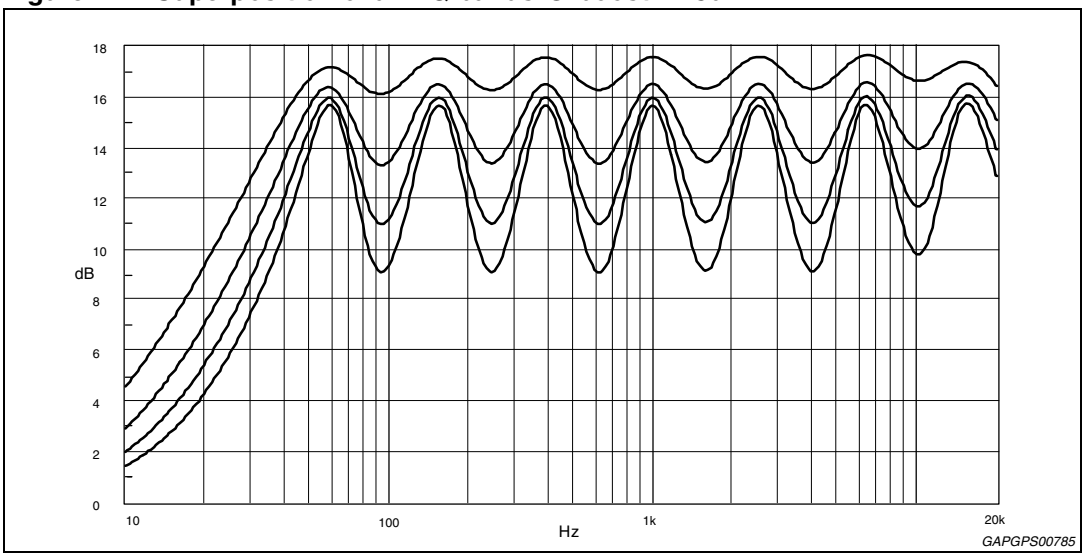
Figure 11. Quality factors @ boost = 15dB, f_{Center} = 1kHz



4.7.4 Superposition of all equalizer filters

Figure 12 shows the superposition of all equalizer filter curves for different quality factors. The gain for all filters is +15dB.

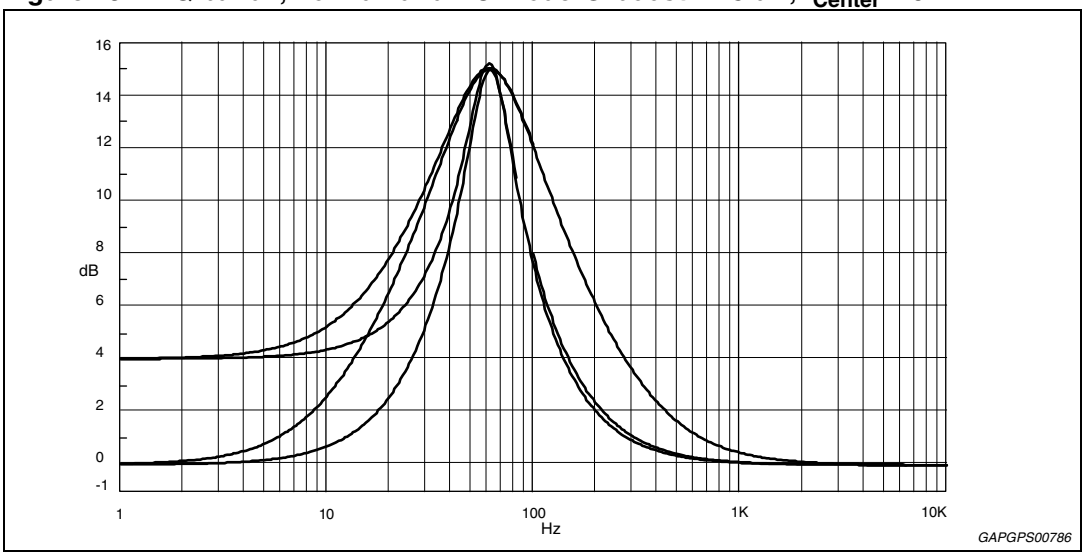
Figure 12. Superposition of all EQ bands @ boost = 15dB



4.7.5 DC-mode of equalizer band 1 (62/100 Hz)

In this mode, the DC-gain 4dB when set to 15dB boost.

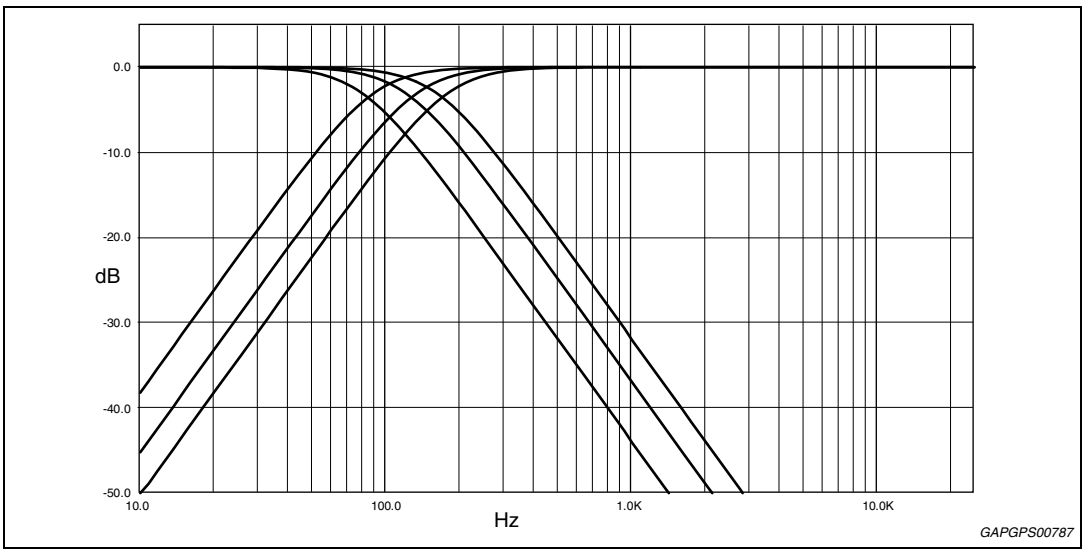
Figure 13. EQ band1, normal- and DC-mode @ boost = 15 dB, f_{Center} = 62 Hz



1. The center frequency, Q, DC-mode and boost/cut can be set fully independently for each filter.

4.8 Subwoofer application

Figure 14. Subwoofer application with low-pass @ 80/120/160Hz and high-pass @ 90/135/180Hz



Both filters, the low-pass as well as the high-pass filter, have butterworth characteristic so that their cut-off frequencies are not equal but shifted by the factor 1.125 to get a flat frequency response.

4.9 Spectrum analyzer

A fully integrated seven band spectrum analyzer with programmable quality factor is present in the TDA7416 (*Figure 15*).

The spectrum analyzer consists of seven band pass filters with rectifier and sample capacitor which stores the maximum peak signal level since the last read cycle. This peak signal level can be read by a microprocessor at the SAout-pin. To allow easy interfacing to an analog port of the microprocessor, the output voltage at this pin is referred to device ground.

The microprocessor starts a read cycle with the negative going clock edge at the SAclk input. On the following positive clock edges, the peak signal level for the band pass filters is subsequently switched to SAout. Each analog output data is valid after the time t_{SAdel}. A reset of the sample capacitors is induced whenever SAclk remains high for the time t_{intres}. Note that a proper reset requires the clock signal SAclk to be held at high potential. *Figure 15* shows the block diagram and *Figure 16* illustrates the read cycle timing of the spectrum analyzer.

Figure 15. Spectrum analyzer block diagram

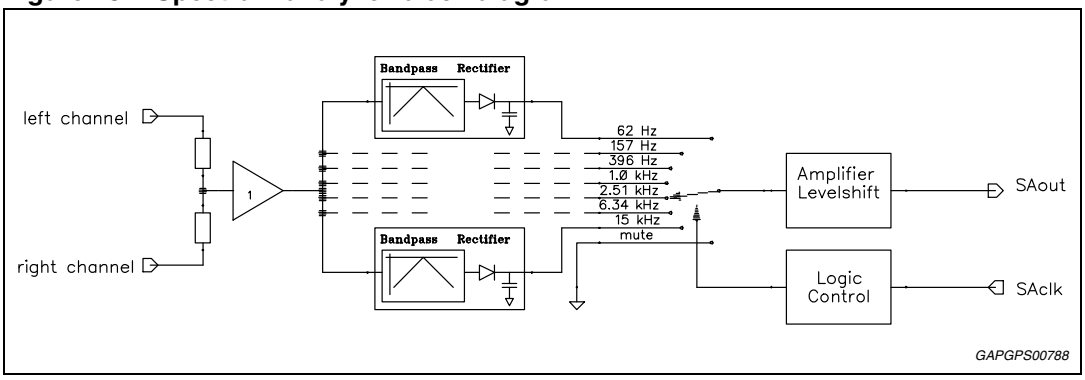
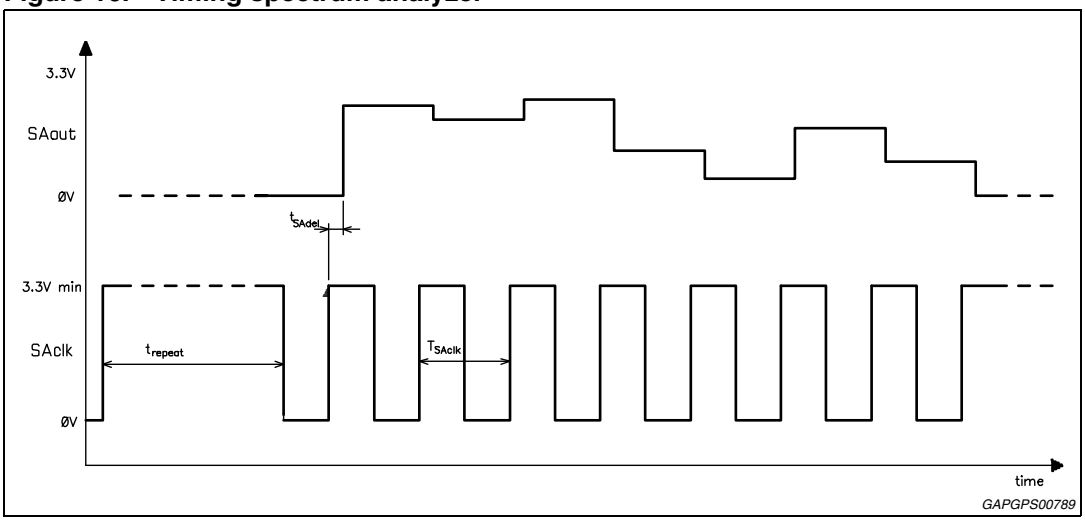


Figure 16. Timing spectrum analyzer



4.10 AC coupling

In some applications additional signal manipulations are desired. For this purpose an AC-coupling is placed before the speaker (fader)-attenuators, which can be activated or internally shorted by I^2C bus. In short condition the input-signal of the speaker-attenuator is available at the AC-outputs. The input-impedance of this AC-inputs is 50k. In addition there are Mix inputs available. With this inputs it is possible to mix an external signal to every speaker with a mixing ratio of 50% (see *Figure 16*).

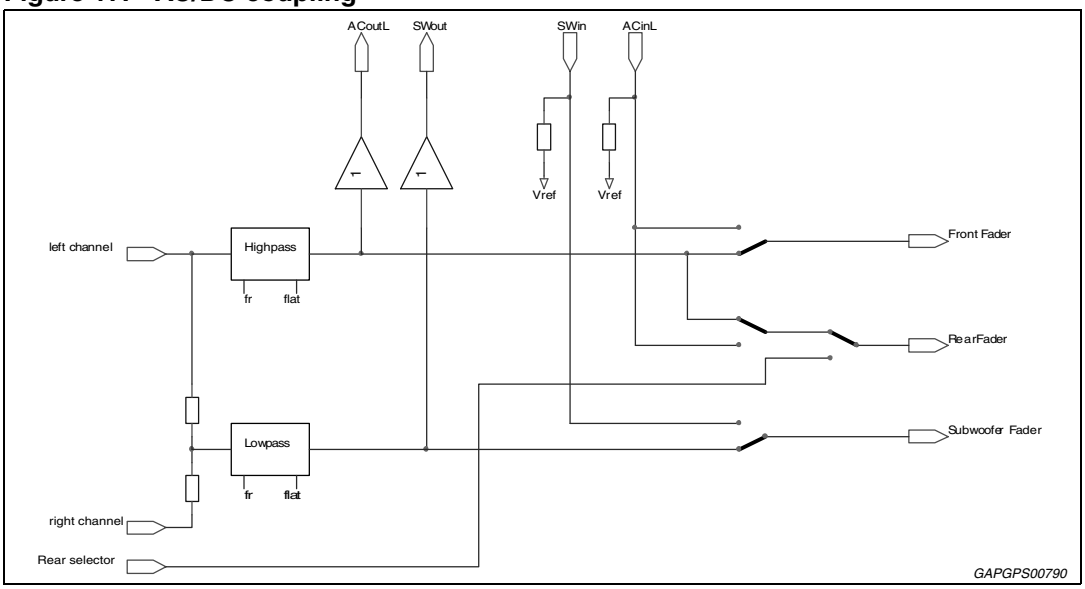
The source of front and rear speaker can be set independently.

As source is choosable:

internal dc coupling (not recommended)

external ac coupling using ACin pins

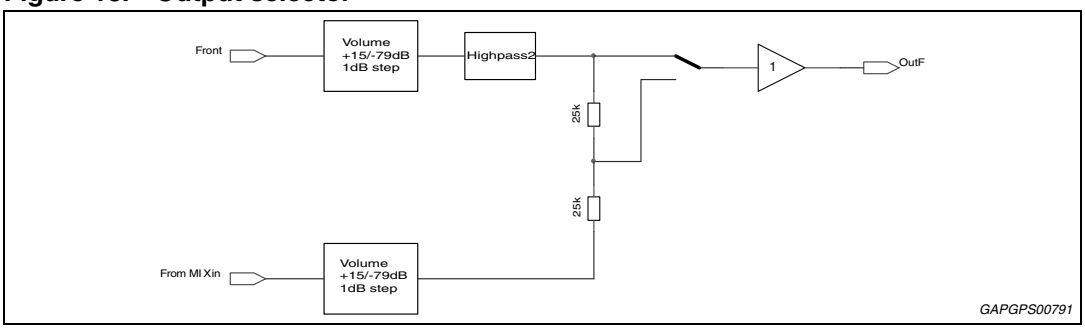
Figure 17. AC/DC coupling



4.11 Front speaker attenuator and mixing

A Mixing-stage is placed after front speaker-attenuator and can be set independently to mixing-mode. Having a full volume for the Mix-signal the stage offers a wide flexibility to adapt the mixing levels.

Figure 18. Output selector

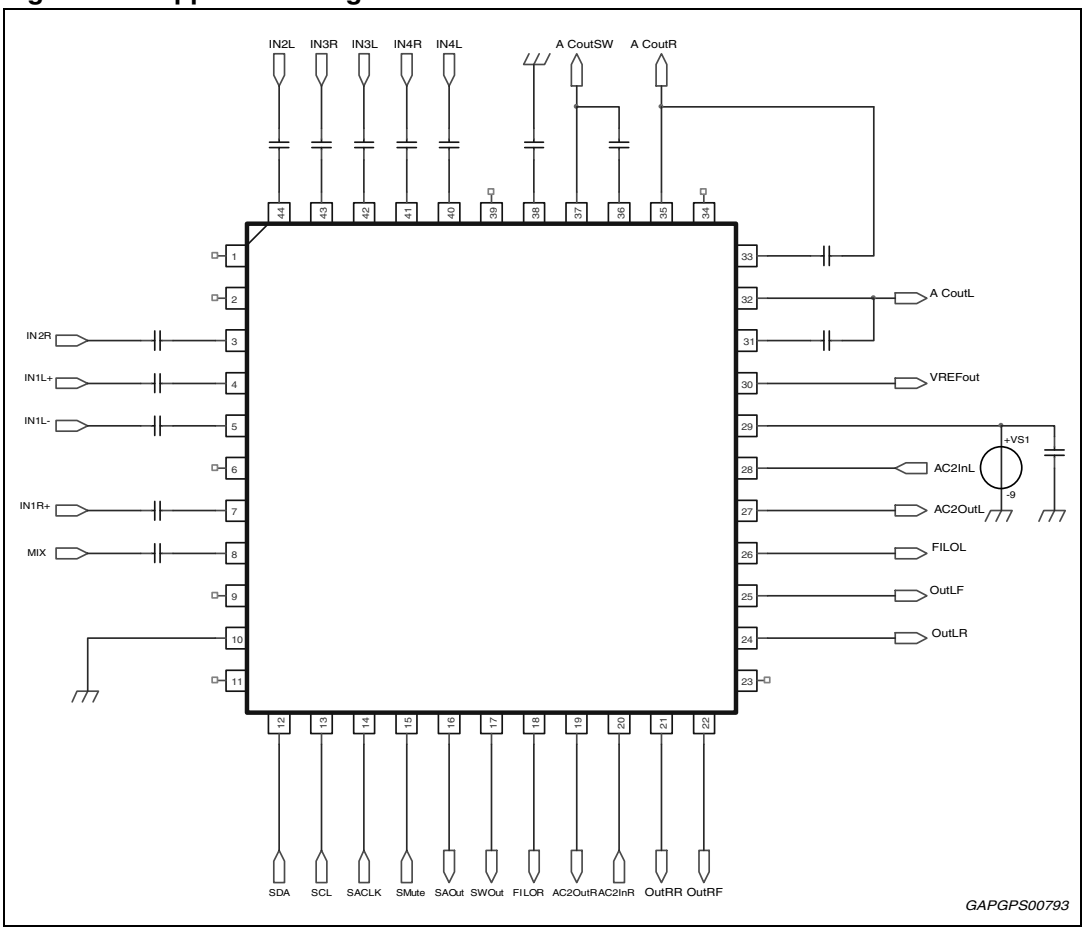


4.12 Audio processor testing

During the test mode, which can be activated by setting bit I_2 of the subaddress byte and D_0 of the audioprocessor testing byte, several internal signals are available at the Mix pin. During this mode the input resistance of 100 kOhm is disconnected from the pin. The internal signals available are shown in the Data-byte specification.

4.13 Application diagram

Figure 19. Application diagram



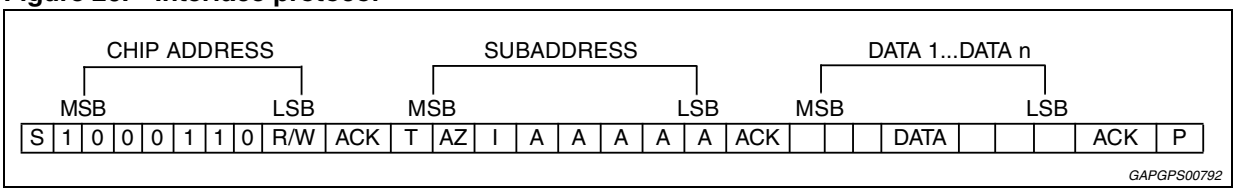
5 I²C bus interface

5.1 Interface protocol

The interface protocol comprises:

- a start condition (S)
- a chip address byte (the LSB bit determines read / write transmission)
- a subaddress byte
- a sequence of data (N-bytes + acknowledge)
- a stop condition (P)

Figure 20. Interface protocol



S = Start

R/W = "0" -> Receive-Mode (Chip could be programmed by µP)
"1" -> Transmission-Mode (Data could be received by µP)

ACK = Acknowledge

P = Stop

Max clock speed 500kbits/s

5.1.1 Auto increment

If bit I in the subaddress byte is set to "1", the auto increment of the subaddress is enabled.

5.1.2 Transmitted data (send mode)

MSB							LSB
X	X	X	X	X	X	X	SM

SM = Soft-mute activated

X = Not Used

The transmitted data is automatically updated after each ACK.
Transmission can be repeated without new chip address.

5.1.3 Reset condition

A power-on-reset is invoked if the supply voltage is below than 3.5V. After that, the following data is written automatically into the registers of all subaddresses:

MSB							LSB
1	1	1	1	1	1	1	0

The programming after POR is marked bold-face / underlined in the programming tables.

With this programming all the outputs are muted to V_{REF} ($V_{OUT} = V_{DD}/2$).

5.2 Subaddress (receive mode)

Table 6. Subaddress (receive mode)

1MSB							LSB	Function
I_2	I_1	I_0	A_4	A_3	A_2	A_1	A_0	
								Audio processor Testmode
0								off
1								on
								AutoZero remain
	0							off
	1							on
								Auto-increment mode
		0						off
		1						on
								Subaddress
			0	0	0	0	0	Source Selector
			0	0	0	0	1	Loudness
			0	0	0	1	0	Volume
			0	0	0	1	1	EQ Filter 1 (62/100Hz)
			0	1	1	0	0	EQ Filter 2 (157Hz)
			0	0	1	0	1	EQ Filter 3 (396Hz)
			0	0	1	1	0	EQ Filter 4 (1kHz)
			0	0	1	1	1	EQ Filter 5 (2.51kHz)
			0	1	0	0	0	EQ Filter 6 (4/6.34kHz)
			0	1	0	0	1	EQ Filter 7 (15/16kHz)
			0	1	0	1	0	Mixing Programming
			0	1	0	1	1	Soft-mute
			0	1	1	0	0	Subwoofer / Spectrum analyzer / High-pass
			0	1	1	0	1	Configuration Audio processor I
			0	1	1	1	0	Mixing Level Control
			0	1	1	1	1	Speaker attenuator LF
			1	0	0	0	0	Speaker attenuator RF
			1	0	0	0	1	Speaker attenuator LR
			1	0	0	1	0	Speaker attenuator RR
			1	0	0	1	1	Subwoofer attenuator
			1	0	1	0	0	Testing Audio processor

5.3 Data byte specification

The status after power-on-reset is marked bold-face / underlined in the programming tables.

5.3.1 Input selector (0)

Table 7. Input selector (0)

MSB							LSB	Function
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
								Source selector
					X	0	0	BUS/PD
					X	0	1	AUX
					X	**1**	**0**	MD
					X	1	1	AM/FM
								Input gain
	0	0	0	0				0dB
	0	0	0	1				1dB
	:	:	:	:				:
	1	1	1	0				14dB
	1	**1**	**1**	**1**				15dB
								Mute
0								off
1								on

5.3.2 Loudness (1)

Table 8. Loudness (1)

MSB							LSB	Function
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
								Attenuation
			0	0	0	0	0	0 dB
			0	0	0	0	1	-1 dB
			:	:	:	:	:	:
			0	1	1	1	0	-14 dB
			0	1	1	1	1	-15 dB
			:	:	:	:	:	:
			1	0	0	1	1	-19 dB
			:	:	:	:	:	not allowed
								Center frequency
	0	0						200Hz
	0	1						400Hz
	1	0						600Hz
	1	**1**						800Hz
								Loudness order
0								First order
1								Second order

5.3.3 Volume (2)

Table 9. Volume (2)

MSB							LSB	Function
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
								Gain/Attenuation
0	0	0	0	0	0	0	0	(+32.0dB)
0	0	0	0	0	0	0	1	(+31.5dB)
:	:	:	:	:	:	:	:	:
0	0	0	1	1	0	0	0	+20.0dB
0	0	0	1	1	0	0	1	+19.5dB
0	0	0	1	1	0	1	0	+19.0dB
:	:	:	:	:	:	:	:	:
0	0	1	1	1	1	1	1	+0.5dB
0	1	0	0	0	0	0	0	0.0dB
0	1	0	0	0	0	0	1	-0.5dB
:	:	:	:	:	:	:	:	:
1	**1**	X	**1**	**1**	**1**	**1**	**0**	-79.0dB
1	1	X	1	1	1	1	1	-79.5dB

Note: It is not recommended to use a gain more than 20dB for system performance reason. In general, the max. gain should be limited by software to the maximum value, which is needed for the system.

5.3.4 Equalizer (3,4,5,6,7,8,9)

Table 10. Equalizer (3,4,5,6,7,8,9)

MSB							LSB	Function
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
								Equalizer cut/boost level
			0	0	0	0	0	-15dB
			0	0	0	0	1	-14dB
			:	:	:	:	:	:
			0	1	1	1	0	-1dB
			0	1	1	1	1	0dB
			1	1	1	1	1	0dB
			1	**1**	**1**	**1**	**0**	+1dB
			:	:	:	:	:	:
			1	0	0	0	1	+14dB
			1	0	0	0	0	+15dB
								Equalizer Q-Factor
	0	0						2.2
	0	1						1.8
	1	0						1.4
	1	**1**						1.0
								Equalizer center frequency (only Subaddresses 3,8,9)
0								62Hz(addr 3)/4kHz(addr 8)/15kHz(addr 9)
1								100Hz(addr 3)/6.24kHz(addr 8)/16kHz(addr 9)
								DC mode EQ Band 1 (62/100 Hz, Subaddress. 4!)
0								on
1								off

5.3.5 Mixing programming (10)

Table 11. Mixing programming (10)

MSB							LSB	Function
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
							0 1	**Mixing** Mute enable
					0 0 1 **1**	0 1 0 **1**		**Rear Source Selector** BUS'(PD) AUX MD AM/FM
			0 **1**	0 **1**				**Mixing Target** Speaker LF off Speaker LF on Speaker RF off Speaker RF on
	0 **1**	X X						**ZeroCross on HPF2** on off
0 **1**								**Spectrum Analyzer Detect Point** After EQ Before EQ

5.3.6 Soft-mute and HPF2 (11)

Table 12. Soft-mute and HPF2 (11)

MSB							LSB	Function
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
							0 1	**Soft-mute** On (Mute) Off
					0 0 **1**	0 1 **X**		**Soft-mute time** Mute time = 0.48ms Mute time = 0.96ms Mute time = 123ms
				0 **1**				**Secondary high-pass enable** Filter available No Filter (Gain)
0 0 0 0 0 0 0 0 1 1 **1**	0 0 0 0 1 1 1 1 X X **X**	0 0 1 1 0 0 1 1 X 0 **1**	0 1 0 1 0 1 0 1 0 1 **1**					**Secondary high-pass effect (with ZeroCross)** 4 dB 6 dB 8 dB 10 dB 12 dB 14 dB 16 dB 18dB 20dB 22dB 0dB

Note: It is recommended to set D3(Filter available or not) during initial mute.

5.3.7 Subwoofer configuration / spectrum analyzer / high-pass (12)

Table 13. Subwoofer configuration / spectrum analyzer / high-pass (12)

MSB							LSB	Function
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
								Subwoofer Filter
						0	0	off
						0	1	80Hz
						1	**0**	120Hz
						1	1	160Hz
								Subwoofer Coupling
				X	0			AC using SW_{In} pin
				X	1			DC
								Spectrum Analyzer Q-Factor
			0					3.5
			1					1.8
								High-pass enable
		0						Filter off
		1						Filter on
								High-pass cut-off frequency
0	0							90Hz
0	1							135Hz
1	0							180Hz
1	**1**							225Hz

5.3.8 Configuration audio processor I (13)

Table 14. Configuration audio processor I (13)

MSB							LSB	Function
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
							0 1	**PD input mode** single ended pseudo differential
						0 1		PD Input Gain -6 dB 0 dB
					0 **1**			**Soft-step volume** off on
			0 0 1 **1**	0 1 0 **1**				**Soft-step time** 320µs 1.28ms 5.12ms 20.4ms
		0 **1**						**Loudness** flat filter ON
	0 **1**							**Front AC speaker** AC coupling (ACin) DC coupling
0 **1**								**Rear effect** No effect signal Equalizing signal

5.3.9 Mixer level control (14)

Table 15. Mixer level control (14)

MSB							LSB	Function
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
								Gain/Attenuation
1	0	0	0	1	1	1	1	+15dB
	:	:	:	:	:	:	:	:
1	0	0	0	0	0	0	1	+ 1dB
1	0	0	0	0	0	0	0	0dB
0	0	0	0	0	0	0	0	0dB
0	0	0	0	0	0	0	1	- 1dB
:	:	:	:	:	:	:	:	:
0	0	0	0	1	1	1	1	-15dB
0	0	0	1	0	0	0	0	-16dB
:	:	:	:	:	:	:	:	:
0	1	0	0	1	1	1	0	-78dB
0	1	0	0	1	1	1	1	-79dB
X	**1**	**1**	**X**	**X**	**X**	**X**	**X**	Mute

5.3.10 Speaker and subwoofer level control (15,16,17,18,19)

Table 16. Speaker and subwoofer level control (15,16,17,18,19)

MSB							LSB	Function
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
								Gain/Attenuation
	0	0	0	1	1	1	1	+15dB
	:	:	:	:	:	:	:	:
	0	0	0	0	0	0	1	+ 1dB
	0	0	0	0	0	0	0	0dB
	0	0	1	0	0	0	0	0dB
	0	0	1	0	0	0	1	- 1dB
	:	:	:	:	:	:	:	:
	0	1	0	0	0	0	0	-16dB
	:	:	:	:	:	:	:	:
	0	1	1	0	0	0	0	-32dB
	:	:	:	:	:	:	:	:
	1	0	0	0	0	0	0	-48dB
	:	:	:	:	:	:	:	:
	1	0	1	0	0	0	0	-64dB
	:	:	:	:	:	:	:	
	1	0	1	1	1	1	1	-79dB
	1	**1**	**X**	**X**	**X**	**X**	**X**	Mute
								Soft-step on/off
0								On
1								Off

5.3.11 Testing audio processor (20)

Table 17. Testing audio processor (20)

MSB							LSB	Function
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
								Audio processor test-mode
							0	off
							1	on
								Test-multiplexer
			0	0	0	0		Spectrum Analyzer Filter 62Hz
			1	0	0	0		Spectrum Analyzer Filter 157Hz
			0	0	0	1		Spectrum Analyzer Filter 396Hz
			1	0	0	1		Spectrum Analyzer Filter 1kHz
			0	0	1	0		Spectrum Analyzer Filter 2.51kHz
			1	0	1	0		Spectrum Analyzer Filter 6.34kHz
			X	0	1	1		Spectrum Analyzer Filter 16kHz
			0	1	0	0		Switch-Ron measurement setup (Level input)
			1	1	0	0		not used
			X	1	0	1		200kHz Oscillator
			X	1	1	0		NB-Hold
			X	**1**	**1**	**1**		internal reference
								Clock
		0						external
		1						internal
								AZ function
	0							off
	1							on
								SC-Clock
0								Fast mode
1								Normal mode

*Note: This byte is used for testing or evaluation purposes only and must not set to other values than "**11111110**" in the application!*

6 Package information

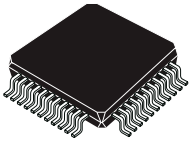
In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*.

ECOPACK® is an ST trademark.

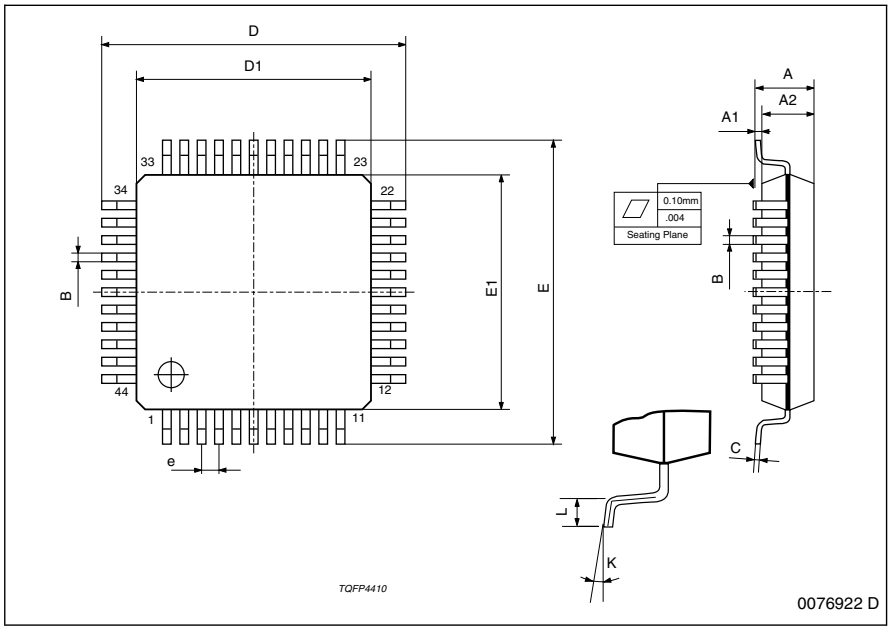
Figure 21. TQFP44 mechanical data and package dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.30	0.37	0.45	0.012	0.015	0.018
C	0.09		0.20	0.004		0.008
D	11.80	12.00	12.20	0.464	0.472	0.480
D1	9.80	10.00	10.20	0.386	0.394	0.401
D3		8.00			0.315	
E	11.80	12.00	12.20	0.464	0.472	0.480
E1	9.80	10.00	10.20	0.386	0.394	0.401
E3		8.00			0.315	
e		0.80			0.031	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
k	0° (min.), 3.5° (typ.), 7° (max.)					

OUTLINE AND MECHANICAL DATA



TQFP44 (10 x 10 x 1.4mm)



GAPGPS00794

7 Revision history

Table 18. Document revision history

Date	Revision	Changes
20-Sep-2003	1	Initial release.
30-Jun-2011	2	Document reformatted. Updated order code in the *Table 1: Device summary on page 1*.
24-Sep-2013	3	Updated disclaimer.