

TDA7416

Car radio signal processor

Features

- 3 stereo inputs
- 1 pseudo differential stereo input
- Volume control
- 7 band equalizer filter control
- High-pass filter for subwoofer application
- Direct mute and soft mute
- 4 independent speaker outputs
- Soft-step speaker control
- Subwoofer output with soft step
- 7 band spectrum analyzer
- Full mixing capability
- HPF2 with ZeroCross
- I²C bus interface

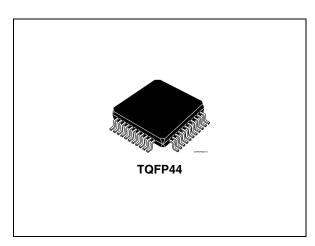


Table 1. Device summary

Order code	Package	Packing
E-TDA7416	TQFP44	Tray

Description

The device includes a high performance audio processor with 7 bands equalizer and spectrum analyzer.

The digital control allows a programming in a wide range of all the filter characteristics.

Contents TDA7416

Contents

1	Bloc	k diagra	am	6
2	Pins	connec	ction	7
3	Elec	trical sp	pecifications	8
	3.1	Supply	/	8
	3.2	Therm	al data	8
	3.3	Absolu	ute maximum ratings	8
	3.4	ESD .		8
	3.5	Electri	cal characteristics	9
4	Desc	cription	of the audio processor part	13
	4.1	Audio	processor features	13
	4.2	Input s	stages	14
		4.2.1	Pseudo-differential stereo input (IN1)	14
		4.2.2	Single-ended stereo inputs	15
	4.3	AutoZe	ero	15
		4.3.1	AutoZero remain	15
	4.4	Loudn	ess	15
		4.4.1	Attenuation	15
		4.4.2	Peak frequency	16
		4.4.3	Loudness filter order	16
		4.4.4	Flat mode	16
	4.5	Soft-m	ute	17
	4.6	Soft-st	ep volume and speaker	17
	4.7	Equalia	zer filter	18
		4.7.1	Attenuation	18
		4.7.2	Center frequency	18
		4.7.3	Quality Factors	19
		4.7.4	Superposition of all equalizer filters	19
		4.7.5	DC-mode of equalizer band 1 (62/100 Hz)	20
	4.8	Subwo	pofer application	20
	4.9	Spectr	rum analyzer	21

	4.10	AC cou	ıpling	22
	4.11	Front s	peaker attenuator and mixing	22
	4.12	Audio p	processor testing	23
	4.13	Applica	ation diagram	23
5	I2C b	us inte	rface	24
	5.1	Interfac	ce protocol	24
		5.1.1	Auto increment	
		5.1.2	Transmitted data (send mode)	24
		5.1.3	Reset condition	25
	5.2	Subado	dress (receive mode)	25
	5.3	Data by	yte specification	26
		5.3.1	Input selector (0)	26
		5.3.2	Loudness (1)	26
		5.3.3	Volume (2)	27
		5.3.4	Equalizer (3,4,5,6,7,8,9)	28
		5.3.5	Mixing programming (10)	29
		5.3.6	Soft-mute and HPF2 (11)	30
		5.3.7	Subwoofer configuration / spectrum analyzer / high-pass (12)	31
		5.3.8	Configuration audio processor I (13)	32
		5.3.9	Mixer level control (14)	33
		5.3.10	Speaker and subwoofer level control (15,16,17,18,19)	33
		5.3.11	Testing audio processor (20)	34
6	Pack	age info	ormation	35
7	Revis	sion his	tory	36



List of tables TDA7416

List of tables

Table 1.	Device summary	1
Table 2.	Supply	
Table 3.	Thermal data	8
Table 4.	Absolute maximum ratings	8
Table 5.	Electrical characteristics	9
Table 6.	Subaddress (receive mode)	25
Table 7.	Input selector (0)	26
Table 8.	Loudness (1)	26
Table 9.	Volume (2)	
Table 10.	Equalizer (3,4,5,6,7,8,9)	28
Table 11.	Mixing programming (10)	29
Table 12.	Soft-mute and HPF2 (11)	30
Table 13.	Subwoofer configuration / spectrum analyzer / high-pass (12)	31
Table 14.	Configuration audio processor I (13)	32
Table 15.	Mixer level control (14)	33
Table 16.	Speaker and subwoofer level control (15,16,17,18,19)	33
Table 17.	Testing audio processor (20)	34
Tahla 18	Document revision history	36



TDA7416 List of figures

List of figures

Figure 1.	Block diagram	. 6
Figure 2.	Pins connection (top view)	. 7
Figure 3.	Input stages	14
Figure 4.	Loudness attenuation @ fP = 400 Hz	15
Figure 5.	Loudness center frequencies @ Attn. = 15 dB	16
Figure 6.	1 st and 2 nd order loudness @ Attn. = 15 dB, f _P = 400 Hz	16
Figure 7.	Soft-mute timing	17
Figure 8.	Soft-step timing for volume	17
Figure 9.	Equalizer filter control @ fCenter = 1kHz, Q = 1.0	18
Figure 10.	Center frequencies @ Gain = 15dB, Q = 1.0	18
Figure 11.	Quality factors @ boost = 15dB, fCenter = 1kHz	19
Figure 12.	Superposition of all EQ bands @ boost = 15dB	19
Figure 13.	EQ band1, normal- and DC-mode @ boost = 15 dB, fCenter = 62 Hz	20
Figure 14.	Subwoofer application with low-pass @ 80/120/160Hz and high-pass @ 90/135/180Hz .	20
Figure 15.	Spectrum analyzer block diagram	21
Figure 16.	Timing spectrum analyzer	21
Figure 17.	AC/DC coupling	22
Figure 18.	Output selector	22
Figure 19.	Application diagram	23
Figure 20.	Interface protocol	24
Figure 21.	TQFP44 mechanical data and package dimensions	35

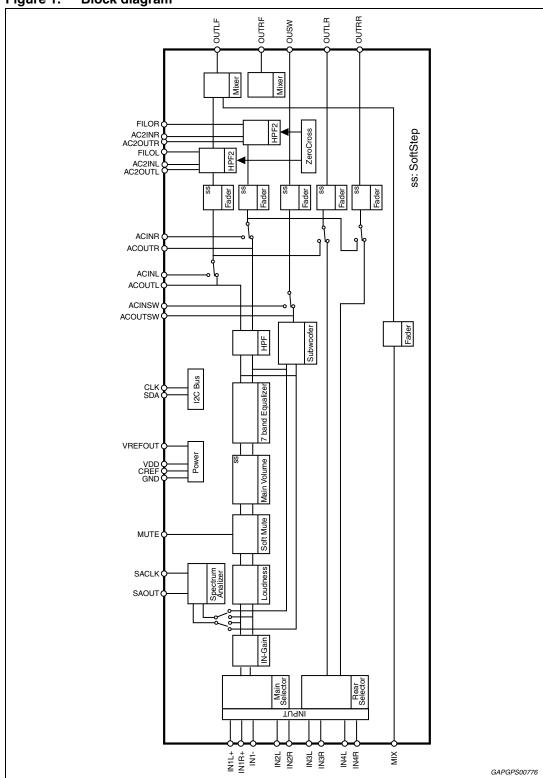


Doc ID 9837 Rev 3 5/37

Block diagram TDA7416

1 Block diagram

Figure 1. Block diagram

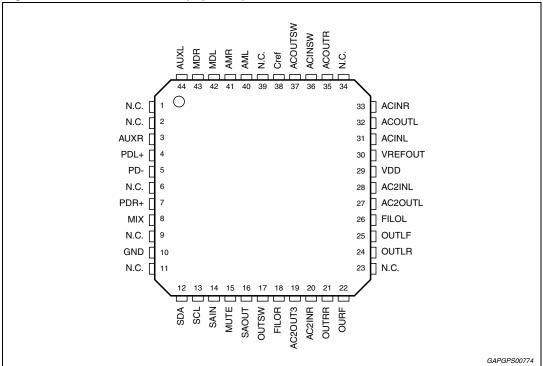


577

TDA7416 Pins connection

2 Pins connection

Figure 2. Pins connection (top view)



3 Electrical specifications

3.1 Supply

Table 2. Supply

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
V _S	Supply voltage		7.5	9	10	V
I _S	Supply current	V _S = 9 V	35	45	55	mA
SVRR	Ripple rejection @ 1kHz	Audio processor (all Filters flat)	-	60	-	dB

3.2 Thermal data

Table 3. Thermal data

Symbol	Description	Value	Unit
R _{th j-pins}	Thermal resistance junction-to-pins max	65	°C/W

3.3 Absolute maximum ratings

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V _s	Operating supply voltage	10.5	V
T _{amb}	Operating temperature range	-40 to 85	°C
T _{stg}	Storage temperature range	-55 to +150	°C

3.4 **ESD**

All pins are protected against ESD according to the MIL883 standard.

3.5 Electrical characteristics

 V_S = 9 V; T_{amb} = 25 °C; R_L = 10 k Ω ; all gains = 0 dB; f = 1 kHz; unless otherwise specified.

Table 5. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Тур.	Max.	Unit
Input sel	ector					
R _{in}	Input resistance	All single-ended Inputs	70	100	130	kΩ
V _{CL}	Clipping level	-	1.8	2.2		V _{RMS}
S _{IN}	Input separation	-	80	100		dB
G _{IN MIN}	Min. input gain	-	-1	0	1	dB
G _{IN MAX}	Max. input gain	-	13	15	17	dB
G _{STEP}	Step resolution	-	0.5	1	1.5	dB
	DC atoms	Adjacent gain steps	-5	1	5	mV
V_{DC}	DC steps	G _{MIN} to G _{MAX}	-10	1	10	mV
V _{offset}	Remaining offset with AutoZero	-	-	0.5	-	mV
Different	al stereo inputs					
R _{in}	Input resistance (see Figure 3)	Differential	70	100	130	kΩ
OMPD	0	V _{CM} = 1 V _{RMS} @ 1 kHz	46	70	-	dB
CMRR	Common mode rejection ratio	V _{CM} = 1 V _{RMS} @ 10 kHz	46	60	-	dB
e _{NO}	Output-noise @ speaker-outputs	20Hz - 20kHz, flat; all stages 0dB	-	11	-	μV
Mixing co	ontrol					
M _{LEVEL}	Mixing ratio	Main / mix-source	-	-6/-6	-	dB
G _{MAX}	Max. gain	-	13	15	17	dB
A _{MAX}	Max. attenuation	-	-83	-79	-75	dB
A _{STEP}	Attenuation step	-	0.5	1	1.5	dB
Loudnes	s control					
A _{STEP}	Step resolution	-	0.5	1	1.5	dB
A _{MAX}	Max. attenuation	-	-21	-19	-17	dB
		f _{P1}	180	200	220	Hz
ı	Deals fraguency	f _{P2}	360	400	440	Hz
f _{Peak}	Peak frequency	f _{P3}	540	600	660	Hz
		f _{P4}	720	800	880	Hz
Volume o	ontrol					
G _{MAX}	Max. gain	-	18	20	22	dB
A _{MAX}	Max. attenuation	-	-83	-79	-75	dB
A _{STEP}	Step resolution	-	0	0.5	1	dB



Doc ID 9837 Rev 3

9/37

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Тур.	Max.	Unit
	Attancetion and agent	G = -20 to +20 dB	-0.75	0	+0.75	dB
E _A	Attenuation set error	G = -80 to -20 dB	-4	0	3	dB
E _T	Tracking error	-	-	-	2	dB
V	DC stone	Adjacent attenuation steps	-	0.1	3	mV
V _{DC}	DC steps	From 0dB to G _{MIN}	-	0.5	5	mV
Soft-mute						
A _{MUTE}	Mute attenuation	-	80	100	-	dB
		T1	-	0.48	1	ms
T _D	Delay time	T2	-	0.96	2	ms
		T3	70	123	170	ms
V _{TH low}	Low threshold for SM-Pin 1)	-	-	-	1	V
V _{TH high}	High threshold for SM - Pin	-	2.5	-	-	V
R _{PU}	Internal pull-up resistor	-	32	45	58	kΩ
V _{PU}	Internal pull-up Voltage	-	-	3.3	-	V
Equalizer	control					
C _{RANGE}	Control range	-	<u>+</u> 14	<u>+</u> 15	<u>+</u> 16	dB
A _{STEP}	Step resolution	-	0.5	1	1.5	dB
f	Center frequency hand 1	f _{C1a}	55	62	69	Hz
'C1	Center frequency band i	f _{C1b}	90	100	110	Hz
f _{C2}	Center frequency band 2	f _{C2}	141	157	173	Hz
f _{C3}	Center frequency band 3	f _{C3}	365	396	437	Hz
f _{C4}	Center frequency band 4	f _{C4}	0.9	1	1.1	kHz
f _{C5}	Center frequency band 5	f _{C5}	2.25	2.51	2.76	kHz
foo	Center frequency hand 6	f _{C6a}	3.6	4	4.4	kHz
1C6	Center requeries baria o	f _{C6b}	5.70	6.34	6.98	kHz
fo-	Center frequency hand 7	f _{C7a}	13.5	15	16.5	kHz
107	Center requeries baria 7	f _{C7b}	14.4	16	17.6	kHz
		Q ₁	0.9	1	1.1	
0	Quality factor	Q_2	1.26	1.4	1.54	
3	TD Delay time TH low Low threshold for SM-Pin 1) TH high High threshold for SM - Pin RPU Internal pull-up resistor VPU Internal pull-up Voltage Qualizer control RANGE Control range ASTEP Step resolution fC1 Center frequency band 1 fC2 Center frequency band 2 fC3 Center frequency band 3 fC4 Center frequency band 4	Q_3	1.62	1.8	1.98	
		Q ₄	1.98	2.2	2.44	
DCarr	DC-gain Band 1	DC = off	-1	0	+1	dB
GAIN	50 gain, bana 1	DC = on, 15dB boost		4		dB

10/37 Doc ID 9837 Rev 3

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Тур.	Max.	Unit
Spectrum	n analyzer control		· ·	<u>I</u>	<u>I</u>	I
V _{SAOut}	Output voltage range	-	0		3.3	V
f _{C1}	Center frequency band 1	f _{C1}	55	62	69	Hz
f _{C2}	Center frequency band 2	f _{C2}	141	157	173	Hz
f _{C3}	Center frequency band 3	f _{C3}	356	396	436	Hz
f _{C4}	Center frequency band 4	f _{C4}	0.9	1	1.1	kHz
f _{C5}	Center frequency band 5	f _{C5}	2.26	2.51	2.76	kHz
f _{C6}	Center frequency band 6	f _{C6}	5.70	6.34	6.98	kHz
f _{C7}	Center frequency band 7	f _{C7}	14.4	16	17.6	kHz
	Overliky feeten	Q ₁	1.62	1.8	1.98	
Q	Quality factor	Q_2	3.15	3.5	3.85	
f _{SACIk}	Clock frequency	-	1	-	100	kHz
t _{SAdel}	Analog output delay time	-	2	-	-	μs
t _{repeat}	Spectrum analyzer repeat time	-	50	-	-	ms
t _{intres}	Internal reset time	-	-	3	-	ms
HPF2			1			
V _{TH}	Zero crossing threshold	-	-	±20	-	mV
E _{MAX}	Max. effect	-	-	22	-	dB
E _{MIN}	Min. effect	-	-	4	-	dB
E _{STEP}	Step resolution	-	1.5	2	2.5	dB
Speaker a	attenuators					
R _{in}	Input Impedance	-	35	50	65	kΩ
G _{MAX}	Max. gain	-	13	15	17	dB
A _{MAX}	Max. attenuation	-	-83	-79	-75	dB
A _{STEP}	Step resolution	-	0.5	1	1.5	dB
A _{MUTE}	Output mute attenuation	-	80	90	-	dB
E _E	Attenuation set error	-	-	-	3	dB
V _{DC}	DC steps	Adjacent Attenuation Steps	-	0.5	5	mV
M _R	Mixing ratio	Signal/Mix _{In}	-	50/50	-	%
Audio ou	tputs	-			1	1
V _{CLIP}	Clipping level	Thd=0.3%	1.8	2.2	-	V _{RMS}
RL	Output load resistance	-	2	-	-	kΩ
C _L	Output load capacitance	-	-	-	10	nF
_					ļ	ļ

577

Doc ID 9837 Rev 3

11/37

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Тур.	Max.	Unit
V_{DC}	DC voltage level	-	4.3	4.5	4.7	V
High-pas	s					
		f _{HP1}	81	90	99	Hz
f	High-pass corner frequency	f _{HP2}	122	135	148	Hz
f _{HP}	Trigit-pass corner frequency	f _{HP3}	162	180	198	Hz
		f _{HP4}	194	215	236	Hz
Subwoof	er attenuator					
R _{in}	Input impedance	-	35	50	65	kΩ
G _{MAX}	Max. gain	-	14	15	16	dB
A _{ATTN}	Max. attenuation	-	-83	-79	-75	dB
A _{STEP}	Step resolution	-	0.5	1	1.5	dB
A _{MUTE}	Output mute attenuation	-	80	90	-	dB
E _E	Attenuation set error		-	-	2	dB
V _{DC}	DC steps	Adjacent Attenuation Steps	-	1	5	mV
Subwoof	er low-pass					
		f _{LP1}	72	80	88	Hz
f_LP	Low-pass corner frequency	f_{LP2}	108	120	132	Hz
		f _{LP3}	144	160	176	Hz
General						
		BW = 20 Hz - 20 kHz	_			
		output muted		3	15	μV
e _{NO}	Output noise	BW = 20 Hz - 20 kHz all gains = 0dB single-ended inputs	-	15	20	μV μV
S/N	Signal-to-noise ratio	all gains = 0 dB flat; $V_O = 2 V_{RMS}$	-	103	-	dB
O/IN	oignal-to-noise fallo	All EQ-bands at +12dB; $Q = 1.0$ a-weighted; $V_Q = 2.6V_{RMS}$	-	87	-	dB
		V _{IN} = 1V _{RMS} ; all stages 0dB	-	0.01	0.1	%
d	Distortion	V _{OUT} = 1V _{RMS} ; Bass & treble = 12dB	-	0.05	0.1	%
S _C	Channel separation left/right	-	80	90	-	dB

4 Description of the audio processor part

4.1 Audio processor features

- Input multiplexer
 - 1 pseudo differential CDC stereo input, programmable as single-ended input
 - 3 single-ended stereo inputs
 - Input gain adjust 0 to 15 dB with 1 dB steps
 - direct mute
 - internal offset-cancellation (AutoZero)
- Mixing stage
 - mixable mix input to Front speaker outputs
 - Input controls +15 to -79 dB with 1 dB steps
 - direct mute
 - Loudness
 - programmable center frequency and filter slope
 - 19 dB with 1dB steps
 - selectable flat-mode (constant attenuation)

Volume

- +32 to -79.5 dB with 0.5 dB step resolution
- soft-step control with programmable blend times
- 100 dB range

Equalizer

- seven bands
- 2nd order frequency response
- center frequency programmable for lowest and highest filter
- programmable quality factor in four steps for each filter
- -15 to 15 dB range with 1dB resolution

Spectrum analyzer

- seven bandpass filters
- 2nd order frequency response
- programmable quality factor for different visual appearance
- analog output
- controlled by external serial clock

High-pass

- 2nd order butterworth high-pass with programmable cut-off frequency
- selectable flat-mode

Speaker

- 4 independent soft-step speaker controls, +15 to -79 dB with 1 dB steps
- mute
- 4 independent programmable mix inputs with 50% mixing ratio
- Subwoofer



Doc ID 9837 Rev 3

- single-ended monaural output
- independent soft-step level control +15 to -79 dB with 1 dB steps

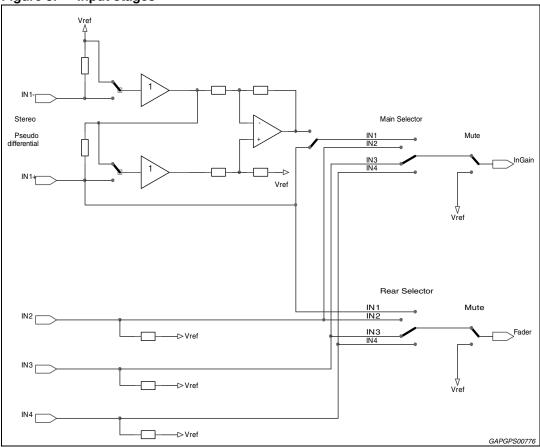
Mute functions

- direct mute
- digitally controlled Soft-mute with 3 programmable mute-times
- Effect
 - Gain effect or high-pass effect fixed external components

4.2 Input stages

In the basic configuration one pseudo-differential, three single-ended stereo are available.





4.2.1 Pseudo-differential stereo input (IN1)

The IN1- input is implemented as a buffered pseudo-differential stereo stage with 100 k Ω input-impedance at each input pin. This input is also configurable as single-ended stereo input. The common input-pin, IN1- features a fast charge switch to speed up the charge time of external capacitors. This switch is released the first time the input-selector data-byte (0) is accessed.

577

14/37 Doc ID 9837 Rev 3

4.2.2 Single-ended stereo inputs

All single-ended inputs have an input impedance of 100 k Ω .

4.3 AutoZero

The AutoZero allows a reduction of the number of pins as well as external components by canceling any offset generated by or before the In-Gain-stage (Please notice that externally generated offsets, e.g. generated through the leakage current of the coupling capacitors, are not canceled).

The auto-zeroing is started every time the DATA-BYTE 0 is selected and needs max. 0.3 ms for the alignment. To avoid audible clicks the Audioprocessor have to be muted by soft-mute or hard-mute during this time.

4.3.1 AutoZero remain

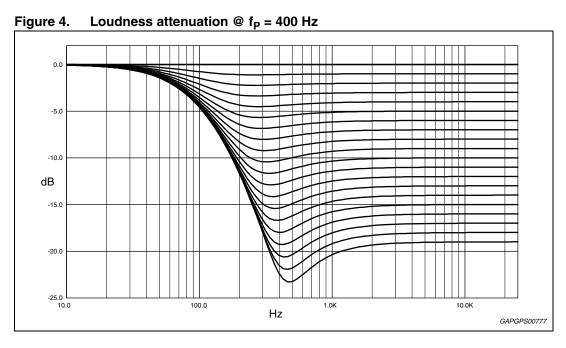
In some cases, for example if the μP is executing a refresh cycle of the IIC-Busprogramming, it is not useful to start a new AutoZero action because no new source is selected and an undesired mute would appear at the out-puts. For such applications the TDA7416 could be switched in the AutoZero remain-mode (Bit 6(I1) of the subaddressbyte). If this bit is set to high, the DATABYTE 0 could be loaded without invoking the AutoZero and the old adjustment-value remains.

4.4 Loudness

There are four parameters programmable in the loudness stage.

4.4.1 Attenuation

Figure 4 shows the attenuation as a function of frequency at $f_P = 400 \text{ Hz}$



57

Doc ID 9837 Rev 3

15/37

Peak frequency 4.4.2

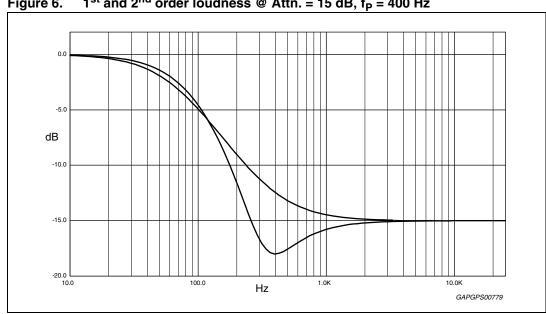
Figure 5 shows the four possible peak-frequencies at 200, 400, 600 and 800Hz

dΒ -10.0 -15.0 Hz GAPGPS00778

Figure 5. Loudness center frequencies @ Attn. = 15 dB

Loudness filter order 4.4.3

Different shapes of 1st and 2nd-order loudness



 1^{st} and 2^{nd} order loudness @ Attn. = 15 dB, f_P = 400 Hz Figure 6.

4.4.4 Flat mode

In flat mode the loudness stage works as a 0dB to -19dB attenuator.

16/37 Doc ID 9837 Rev 3

4.5 Soft-mute

The digitally controlled soft-mute stage allows muting/demuting the signal with a I^2C bus programmable slope. The mute process can either be activated by the soft-mute pin or by the I^2C bus. This slope is realized in a special S-shaped curve to mute slow in the critical regions (see *Figure 7*).

For timing purposes the Bit0 of the I²C bus output register is set to 1 from the start of muting until the end of de-muting.

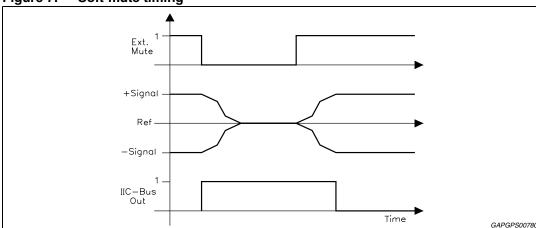


Figure 7. Soft-mute timing

 Please notice that a started Mute-action is always terminated and could not be interrupted by a change of the mute -signal.

4.6 Soft-step volume and speaker

When the speaker-level is changed audible clicks could appear at the output. The root cause of those clicks could either be a DC-Offset before the speaker-stage or the sudden change of the envelope of the audio signal. With the soft-step feature both kinds of clicks could be reduced to a minimum and are no more audible. The blend-time from one step to the next is programmable in four steps.

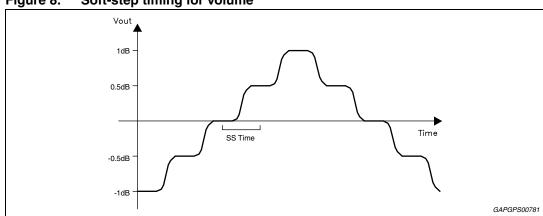


Figure 8. Soft-step timing for volume

For steps more than 0.5dB (Volume) or 1dB (Speaker) the soft-step mode should be deactivated because
it could generate a hard 1dB step during blending.

5/

Doc ID 9837 Rev 3

4.7 Equalizer filter

There are three parameters programmable in the equalizer filter:

4.7.1 Attenuation

Figure 9 shows the boost and cut response as a function of frequency at a center frequency of 1kHz.

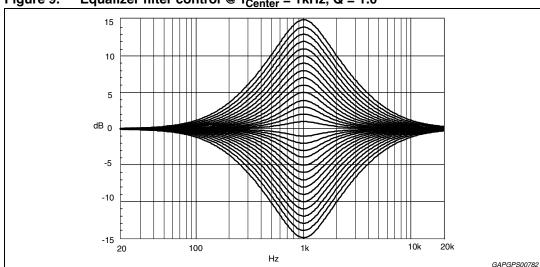


Figure 9. Equalizer filter control @ $f_{Center} = 1kHz$, Q = 1.0

4.7.2 Center frequency

This parameter is programmable in the filter stage 1(62/100Hz), 6(4/6.34kHz) and 7(15/16kHz) only.

Figure 10 shows the center frequencies 62, 156, 396, 1000, 2510, 6340 and 15000 Hz of the 7 equalizer filters.

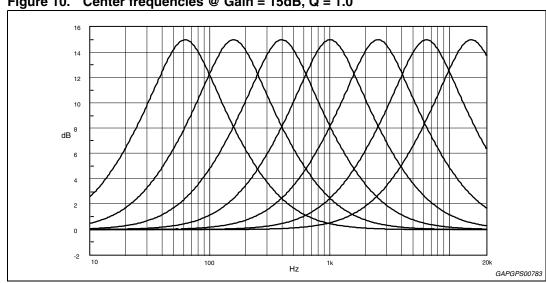


Figure 10. Center frequencies @ Gain = 15dB, Q = 1.0

18/37 Doc ID 9837 Rev 3

4.7.3 Quality Factors

 $\textit{Figure 11} \ \text{shows the four possible quality factors 1, 1.4, 1.8 and 2.2}$

16 14 12 16 10 100 Hz 1k 20k GAPGPS00784

Figure 11. Quality factors @ boost = 15dB, f_{Center} = 1kHz

4.7.4 Superposition of all equalizer filters

Figure 12 shows the superposition of all equalizer filter curves for different quality factors. The gain for all filters is +15dB.

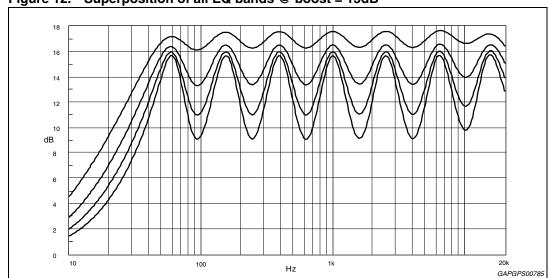
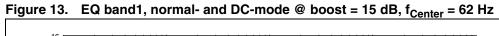


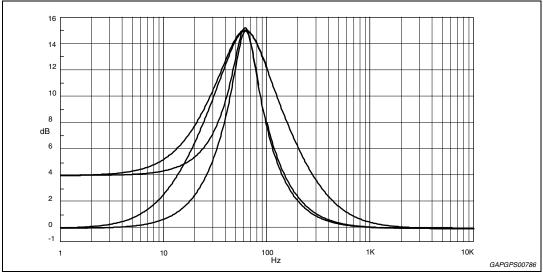
Figure 12. Superposition of all EQ bands @ boost = 15dB

577

4.7.5 DC-mode of equalizer band 1 (62/100 Hz)

In this mode, the DC-gain 4dB when set to 15dB boost.

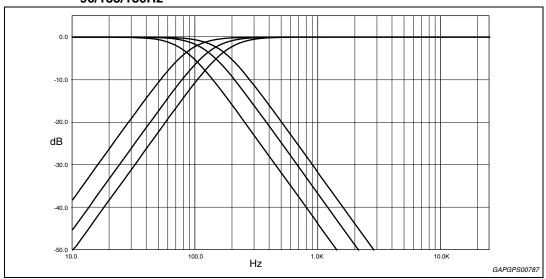




^{1.} The center frequency, Q, DC-mode and boost/cut can be set fully independently for each filter.

Subwoofer application 4.8

Figure 14. Subwoofer application with low-pass @ 80/120/160Hz and high-pass @ 90/135/180Hz



Both filters, the low-pass as well as the high-pass filter, have butterworth characteristic so that their cut-off frequencies are not equal but shifted by the factor 1.125 to get a flat frequency response.

20/37 Doc ID 9837 Rev 3

4.9 Spectrum analyzer

A fully integrated seven band spectrum analyzer with programmable quality factor is present in the TDA7416 (*Figure 15*).

The spectrum analyzer consists of seven band pass filters with rectifier and sample capacitor which stores the maximum peak signal level since the last read cycle. This peak signal level can be read by a microprocessor at the SAout-pin. To allow easy interfacing to an analog port of the microprocessor, the output voltage at this pin is referred to device ground.

The microprocessor starts a read cycle with the negative going clock edge at the SAclk input. On the following positive clock edges, the peak signal level for the band pass filters is subsequently switched to SAout. Each analog output data is valid after the time t_{SAdel} . A reset of the sample capacitors is induced whenever SAclk remains high for the time t_{intres} . Note that a proper reset requires the clock signal SAclk to be held at high potential. *Figure 15* shows the block diagram and *Figure 16* illustrates the read cycle timing of the spectrum analyzer.

Figure 15. Spectrum analyzer block diagram

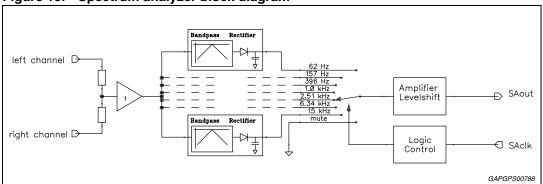
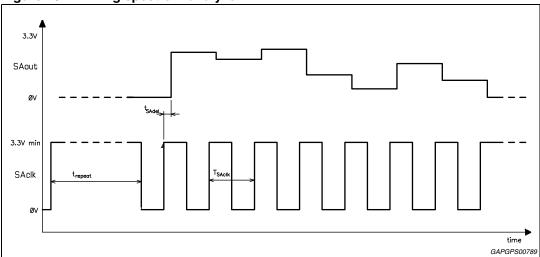


Figure 16. Timing spectrum analyzer



577

4.10 AC coupling

In some applications additional signal manipulations are desired. For this purpose an AC-coupling is placed before the speaker (fader)-attenuators, which can be activated or internally shorted by I²C bus. In short condition the input-signal of the speaker-attenuator is available at the AC-outputs. The input-impedance of this AC-inputs is 50k. In addition there are Mix inputs available. With this inputs it is possible to mix an external signal to every speaker with a mixing ratio of 50% (see *Figure 16*).

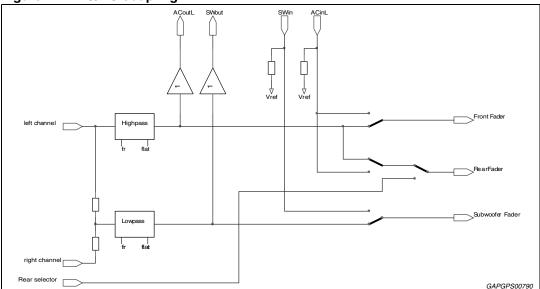
The source of front and rear speaker can be set independently.

As source is choosable:

internal dc coupling (not recommended)

external ac coupling using ACin pins

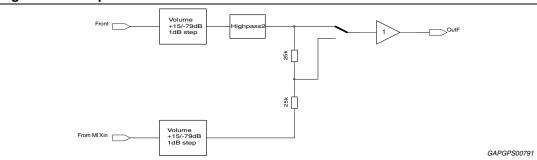
Figure 17. AC/DC coupling



4.11 Front speaker attenuator and mixing

A Mixing-stage is placed after front speaker-attenuator and can be set independently to mixing-mode. Having a full volume for the Mix-signal the stage offers a wide flexibility to adapt the mixing levels.

Figure 18. Output selector



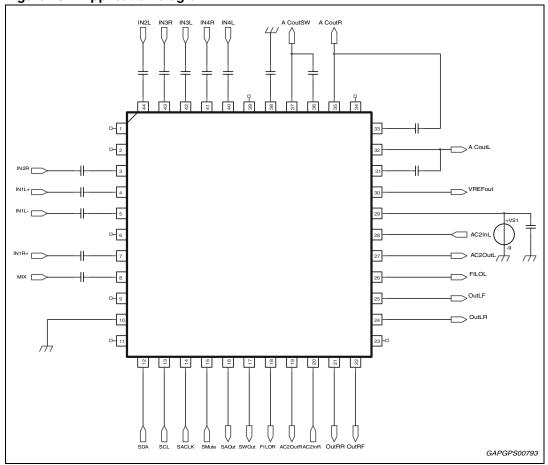
22/37 Doc ID 9837 Rev 3

4.12 Audio processor testing

During the test mode, which can be activated by setting bit I_2 of the subaddress byte and D_0 of the audioprocessor testing byte, several internal signals are available at the Mix pin. During this mode the input resistance of 100 kOhm is disconnected from the pin. The internal signals available are shown in the Data-byte specification.

4.13 Application diagram

Figure 19. Application diagram



5/

I2C bus interface TDA7416

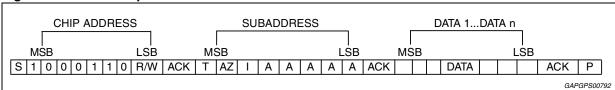
5 I²C bus interface

5.1 Interface protocol

The interface protocol comprises:

- a start condition (S)
- a chip address byte (the LSB bit determines read / write transmission)
- a subaddress byte
- a sequence of data (N-bytes + acknowledge)
- a stop condition (P)

Figure 20. Interface protocol



S = Start

R/W = "0" -> Receive-Mode (Chip could be programmed by μ P) "1" -> Transmission-Mode (Data could be received by μ P)

ACK = Acknowledge

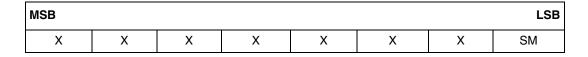
P = Stop

Max clock speed 500kbits/s

5.1.1 Auto increment

If bit I in the subaddress byte is set to "1", the auto increment of the subaddress is enabled.

5.1.2 Transmitted data (send mode)



SM = Soft-mute activated

X = Not Used

The transmitted data is automatically updated after each ACK.

Transmission can be repeated without new chip address.

TDA7416 I2C bus interface

5.1.3 Reset condition

A power-on-reset is invoked if the supply voltage is below than 3.5V. After that, the following data is written automatically into the registers of all subaddresses:

MSB							LSB
1	1	1	1	1	1	1	0

The programming after POR is marked bold-face / underlined in the programming tables. With this programming all the outputs are muted to V_{REF} ($V_{OUT} = V_{DD}/2$).

5.2 Subaddress (receive mode)

Table 6. Subaddress (receive mode)

1MSB						LSB	Francisco	
l ₂	I ₁	I ₀	A ₄	A ₃	A ₂	A ₁	A ₀	- Function
								Audio processor Testmode
0								off
1								on
								AutoZero remain
	0							off
	1							on
								Auto-increment mode
		0						off
		1						on
								Subaddress
			0	0	0	0	0	Source Selector
			0	0	0	0	1	Loudness
			0	0	0	1	0	Volume
			0	0	0	1	1	EQ Filter 1 (62/100Hz)
			0	1	1	0	0	EQ Filter 2 (157Hz)
			0	0	1	0	1	EQ Filter 3 (396Hz)
			0	0	1	1	0	EQ Filter 4 (1kHz)
			0	0	1	1	1	EQ Filter 5 (2.51kHz)
			0	1	0	0	0	EQ Filter 6 (4/6.34kHz)
			0	1	0	0	1	EQ Filter 7 (15/16kHz)
			0	1	0	1	0	Mixing Programming
			0	1	0	1	1	Soft-mute
			0	1	1	0	0	Subwoofer / Spectrum analyzer / High-pass
			0	1	1	0	1	Configuration Audio processor I
			0	1	1	1	0	Mixing Level Control
			0	1	1	1	1	Speaker attenuator LF
			1	0	0	0	0	Speaker attenuator RF
			1	0	0	0	1	Speaker attenuator LR
			1	0	0	1	0	Speaker attenuator RR
			1	0	0	1	1	Subwoofer attenuator
			1	0	1	0	0	Testing Audio processor

I2C bus interface TDA7416

5.3 Data byte specification

The status after power-on-reset is marked bold-face / underlined in the programming tables.

5.3.1 Input selector (0)

Table 7. Input selector (0)

MSB							LSB	Function
D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	Function
								Source selector
					Х	0	0	BUS/PD
					Х	0	1	AUX
					Х	1	0	MD
					Χ	1	1	AM/FM
								Input gain
	0	0	0	0				0dB
	0	0	0	1				1dB
	:	:	:	:				:
	1	1	1	0				14dB
	1	1	1	1				<u>15dB</u>
								Mute
0								off
1								<u>on</u>

5.3.2 Loudness (1)

Table 8. Loudness (1)

MSB							LSB	Function
D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	Function
								Attenuation
			0	0	0	0	0	0 dB
			0	0	0	0	1	-1 dB
			:	:	:	:	:	:
			0	1	1	1	0	-14 dB
			0	1	1	1	1	-15 dB
			:	:	:	:	:	:
			1	0	0	1	1	-19 dB
			:	:	:	:	:	not allowed
								Center frequency
	0	0						200Hz
	0	1						400Hz
	1	0						600Hz
	1	1						<u>800Hz</u>
								Loudness order
0								First order
1								Second order

TDA7416 I2C bus interface

5.3.3 Volume (2)

Table 9. Volume (2)

MSB							LSB	Function
D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	Function
								Gain/Attenuation
0	0	0	0	0	0	0	0	(+32.0dB)
0	0	0	0	0	0	0	1	(+31.5dB)
:	:	:	:	:	:	:	:	:
0	0	0	1	1	0	0	0	+20.0dB
0	0	0	1	1	0	0	1	+19.5dB
0	0	0	1	1	0	1	0	+19.0dB
:	:	:	:	:	:	:	:	:
0	0	1	1	1	1	1	1	+0.5dB
0	1	0	0	0	0	0	0	0.0dB
0	1	0	0	0	0	0	1	-0.5dB
:	:	:	:	:	:	:	:	:
1	1	Χ	1	1	1	1	0	<u>-79.0dB</u>
1	1	Χ	1	1	1	1	1	-79.5dB

Note:

It is not recommended to use a gain more than 20dB for system performance reason. In general, the max. gain should be limited by software to the maximum value, which is needed for the system.

I2C bus interface TDA7416

5.3.4 Equalizer (3,4,5,6,7,8,9)

Table 10. Equalizer (3,4,5,6,7,8,9)

MSB							LSB	Function
D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	Function
			0 0 : 0 0 1 1 : 1	0 0 : 1 1 1 1 :	0 0 : 1 1 1 1 :	0 0 : 1 1 1 1 :	0 1 : 0 1 1 0 : 1	Equalizer cut/boost level -15dB -14dB : -1dB 0dB 0dB +1dB : +14dB :
	0 0 1 1	0 1 0 1	•	0			, and the second	Equalizer Q-Factor 2.2 1.8 1.4 1.0
0 1								Equalizer center frequency (only Subaddresses 3,8,9) 62Hz(addr 3)/4kHz(addr 8)/15kHz(addr 9) 100Hz(addr 3)/6.24kHz(addr 8)/16kHz(addr 9)
0 1								DC mode EQ Band 1 (62/100 Hz, Subaddress. 4!) on off

TDA7416 I2C bus interface

5.3.5 Mixing programming (10)

Table 11. Mixing programming (10)

MSB							LSB	Function
D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	Function
							0 1	Mixing Mute enable
			0	0 1	0 0 1 1	0 1 0 1		Rear Source Selector BUS'(PD) AUX MD AM/FM Mixing Target Speaker LF off Speaker LF on Speaker RF off
	0 1	X X	1					Speaker RF on ZeroCross on HPF2 on off
0 1								Spectrum Analyzer Detect Point After EQ Before EQ

I2C bus interface TDA7416

5.3.6 Soft-mute and HPF2 (11)

Table 12. Soft-mute and HPF2 (11)

MSB							LSB	Function
D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	Function
								Soft-mute
							0	On (Mute)
							1	Off
								Soft-mute time
					0	0		Mute time = 0.48ms
					0	1		Mute time = 0.96ms
					1	X		Mute time = 123ms
								Secondary high-pass enable
				0				Filter available
				1				No Filter (Gain)
								Secondary high-pass effect (with ZeroCross)
0	0	0	0					4 dB
0	0	0	1					6 dB
0	0	1	0					8 dB
0	0	1	1					10 dB
0	1	0	0					12 dB
0	1	0	1					14 dB
0	1	1	0					16 dB
0	1	1	1					18dB
1	Χ	Χ	0					20dB
1	Χ	0	1					22dB
1	X	1	1					<u>0dB</u>

Note: It is recommended to set D3(Filter available or not) during initial mute.

TDA7416 I2C bus interface

5.3.7 Subwoofer configuration / spectrum analyzer / high-pass (12)

Table 13. Subwoofer configuration / spectrum analyzer / high-pass (12)

MSB				<u> </u>			LSB	Function
D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	runction
								Subwoofer Filter
						0	0	off
						0	1	80Hz
						1	0	<u>120Hz</u>
						1	1	160Hz
								Subwoofer Coupling
				Χ	0			AC using SW _{In} pin
				<u>X</u>	<u>1</u>			<u>DC</u>
								Spectrum Analyzer Q-Factor
			0					3.5
			1					1.8
								High-pass enable
		0						Filter off
		1						Filter on
								High-pass cut-off frequency
0	0							90Hz
0	1							135Hz
1	0							180Hz
1	1							225Hz

I2C bus interface TDA7416

5.3.8 Configuration audio processor I (13)

Table 14. Configuration audio processor I (13)

MSB							LSB	Function
D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	runction
							0	PD input mode single ended pseudo differential
						0		PD Input Gain -6 dB 0 dB
					0 1			Soft-step volume off on
			0 0 1 1	0 1 0 1				Soft-step time 320µs 1.28ms 5.12ms 20.4ms
		0 1						Loudness flat filter ON
	0 1							Front AC speaker AC coupling (ACin) DC coupling
0 1								Rear effect No effect signal Equalizing signal

TDA7416 I2C bus interface

5.3.9 Mixer level control (14)

Table 15. Mixer level control (14)

MSB							LSB	Function
D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	runction
								Gain/Attenuation
1	0	0	0	1	1	1	1	+15dB
	:	:	:	:	:	:	:	:
1	0	0	0	0	0	0	1	+ 1dB
1	0	0	0	0	0	0	0	0dB
0	0	0	0	0	0	0	0	0dB
0	0	0	0	0	0	0	1	- 1dB
:	:	:	:	:	:	:	:	:
0	0	0	0	1	1	1	1	-15dB
0	0	0	1	0	0	0	0	-16dB
:	:	:	:	:	:	:	:	:
0	1	0	0	1	1	1	0	-78dB
0	1	0	0	1	1	1	1	-79dB
X	1	1	X	Х	Х	X	X	Mute

5.3.10 Speaker and subwoofer level control (15,16,17,18,19)

Table 16. Speaker and subwoofer level control (15,16,17,18,19)

MSB							LSB	Function
D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	runction
								Gain/Attenuation
	0	0	0	1	1	1	1	+15dB
	:	:	:	:	:	:	:	:
	0	0	0	0	0	0	1	+ 1dB
	0	0	0	0	0	0	0	0dB
	0	0	1	0	0	0	0	0dB
	0	0	1	0	0	0	1	- 1dB
	:	:	:	:	:	:	:	:
	0	1	0	0	0	0	0	-16dB
	:	:	:	:	:	:	:	:
	0	1	1	0	0	0	0	-32dB
	:	:	:	:	:	:	:	:
	1	0	0	0	0	0	0	-48dB
	:	:	:	:	:	:	:	:
	1	0	1	0	0	0	0	-64dB
	:	:	:	:	:	:	:	
	1	0	1	1	1	1	1	-79dB
	1	1	X	X	X	X	X	<u>Mute</u>
								Soft-step on/off
0								On
1								<u>Off</u>

I2C bus interface TDA7416

5.3.11 Testing audio processor (20)

Table 17. Testing audio processor (20)

MSB							LSB	Function
D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	Function
							0	Audio processor test-mode off on
			0 1 0 1 0 1 X 0	0 0 0 0 0 0 0	0 0 0 0 1 1 1 0	0 0 1 1 0 0 1 0		Test-multiplexer Spectrum Analyzer Filter 62Hz Spectrum Analyzer Filter 157Hz Spectrum Analyzer Filter 396Hz Spectrum Analyzer Filter 1kHz Spectrum Analyzer Filter 2.51kHz Spectrum Analyzer Filter 6.34kHz Spectrum Analyzer Filter 16kHz Switch-Ron measurement setup (Level input) not used
			X X	1 1 1	0 1 1	1 0 1		200kHz Oscillator NB-Hold internal reference
		0 1						Clock external internal
	0 1							AZ function off on
0 1								SC-Clock Fast mode Normal mode

Note: This byte is used for testing or evaluation purposes only and must not set to other values than "1111110" in the application!

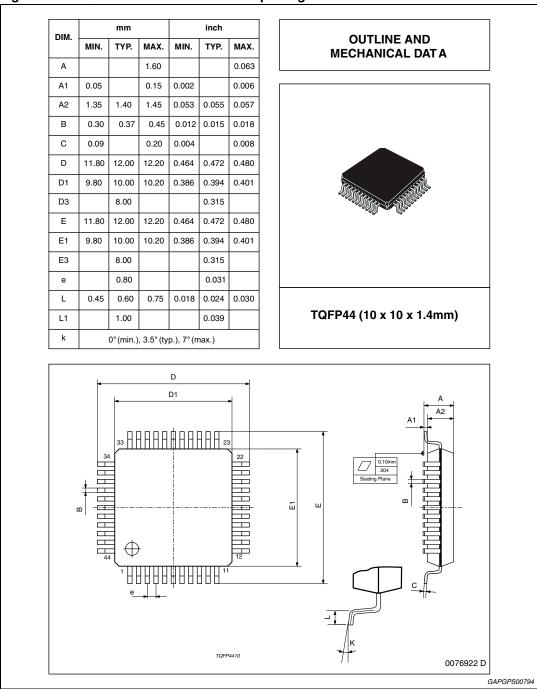
TDA7416 Package information

6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com.

 $\mathsf{ECOPACK}^{\mathbb{B}}$ is an ST trademark.

Figure 21. TQFP44 mechanical data and package dimensions



57

Doc ID 9837 Rev 3 35/37

Revision history TDA7416

7 Revision history

Table 18. Document revision history

Date	Revision	Changes
20-Sep-2003	1	Initial release.
30-Jun-2011	2	Document reformatted. Updated order code in the <i>Table 1: Device summary on page 1</i> .
24-Sep-2013	3	Updated disclaimer.

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST's terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST'S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

ST PRODUCTS ARE NOT DESIGNED OR AUTHORIZED FOR USE IN: (A) SAFETY CRITICAL APPLICATIONS SUCH AS LIFE SUPPORTING, ACTIVE IMPLANTED DEVICES OR SYSTEMS WITH PRODUCT FUNCTIONAL SAFETY REQUIREMENTS; (B) AERONAUTIC APPLICATIONS; (C) AUTOMOTIVE APPLICATIONS OR ENVIRONMENTS, AND/OR (D) AEROSPACE APPLICATIONS OR ENVIRONMENTS. WHERE ST PRODUCTS ARE NOT DESIGNED FOR SUCH USE, THE PURCHASER SHALL USE PRODUCTS AT PURCHASER'S SOLE RISK, EVEN IF ST HAS BEEN INFORMED IN WRITING OF SUCH USAGE, UNLESS A PRODUCT IS EXPRESSLY DESIGNATED BY ST AS BEING INTENDED FOR "AUTOMOTIVE, AUTOMOTIVE SAFETY OR MEDICAL" INDUSTRY DOMAINS ACCORDING TO ST PRODUCT DESIGN SPECIFICATIONS. PRODUCTS FORMALLY ESCC, QML OR JAN QUALIFIED ARE DEEMED SUITABLE FOR USE IN AEROSPACE BY THE CORRESPONDING GOVERNMENTAL AGENCY.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

© 2013 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com



Doc ID 9837 Rev 3 37/37