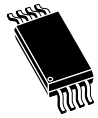
M95M04-A125 M95M04-A145

Datasheet

Automotive 4 Mbit serial SPI bus EEPROM



TSSOP8

169 mil width

SO8N

150 mil width

Product status link
M95M04-A125
M95M04-A145

Features

- AEC-Q100 grade 0 conform qualification
- Compatible with the serial peripheral interface (SPI) bus
- Memory array
  - 4 Mbits (512 Kbytes) of EEPROM
  - Page size: 512 bytes
  - Write protection by block: 1/4, 1/2 or whole memory
- Additional write lockable page (identification page)
- Extended temperature and voltage range
  - Up to 145 °C (V_{CC} from 2.9 V to 5.5 V)
- Maximum clock frequency
  - 10 MHz full range of V_{CC}
- Schmitt trigger inputs for noise filtering
- Short write cycle time
  - Byte write within 4 ms
  - Page write within 4 ms
- ESD Protection (human body model)
  - 4000 V
- Packages
  - RoHS-compliant and halogen-free (ECOPACK2)
  - TSSOP8 package ECOPACK2
  - SO8N package ECOPACK2

1 Description

The M95M04-A125 and M95M04-A145 are 4 Mbit serial EEPROM automotive grade devices operating up to 145 °C. They are compliant with the very high level of reliability defined by the automotive standard AEC-Q100 grade 0.

The devices are accessed by a simple serial SPI compatible interface running at up to 10 MHz.

The memory array is based on advanced true EEPROM technology (electrically erasable programmable memory). The M95M04-A125 and M95M04-A145 are byte-alterable memories (524288 × 8 bits) organized as 1024 pages of 512 bytes in which the data integrity is significantly improved with an embedded Error Correction Code logic.

The M95M04-A125 and M95M04-A145 offer an additional identification page (512 bytes) in which the ST device identification can be read. This page can also be used to store sensitive application parameters that can later be permanently locked in read-only mode.

Figure 1. Logic diagram

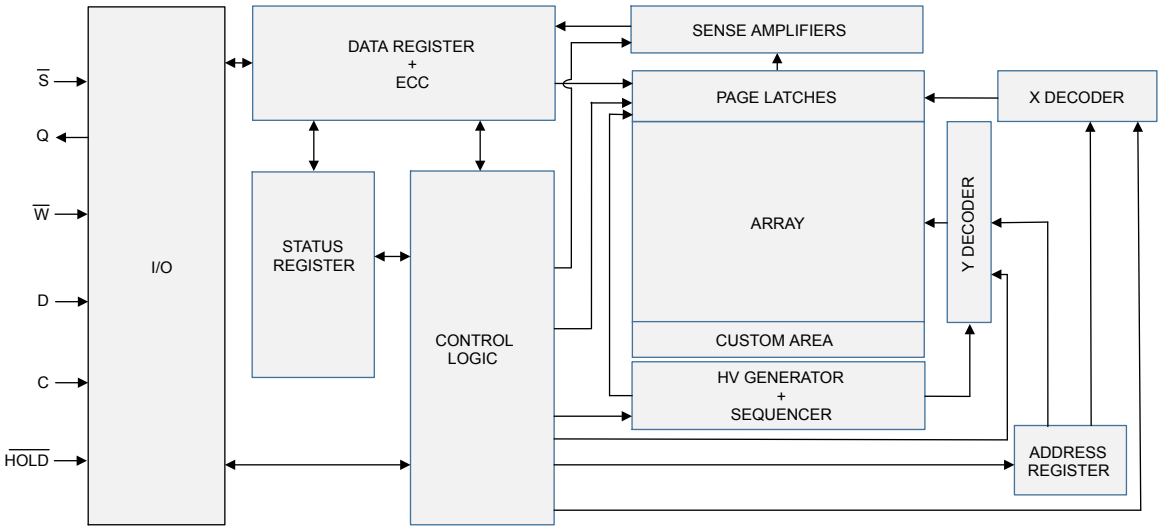
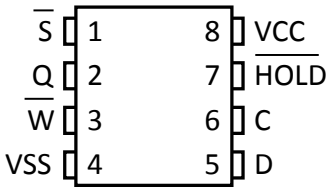


Figure 2. 8-pin package connections



1. See Section 9 Package information section for package dimensions and how to identify pin-1.

Table 1. Signal names

Signal name	Description
C	Serial clock
D	Serial data input
Q	Serial data output
$\overline{S}$	Chip select
$\overline{W}$	Write protect
$\overline{HOLD}$	Hold
V_{CC}	Supply voltage
V_{SS}	Ground

2 Signal description

All input signals must be held high or low (according to voltages of V_{IH} or V_{IL}, as specified in Table 14). These signals are described below.

2.1 Serial data output (Q)

This output signal is used to transfer data serially out of the device during a read operation. Data is shifted out on the falling edge of serial clock (C), most significant bit (MSB) first. In all other cases, the serial data output is in high impedance.

2.2 Serial data input (D)

This input signal is used to transfer data serially into the device. D input receives instructions, addresses, and the data to be written. Values are latched on the rising edge of serial clock (C), most significant bit (MSB) first.

2.3 Serial clock (C)

This input signal allows to synchronize the timing of the serial interface. Instructions, addresses, or data present at serial data input (D) are latched on the rising edge of serial clock (C). Data on serial data output (Q) changes after the falling edge of serial clock (C).

2.4 Chip select ($\overline{S}$)

Driving chip select ($\overline{S}$) low selects the device in order to start communication. Driving chip select ($\overline{S}$) high deselects the device and serial data output (Q) enters the high impedance state.

2.5 Hold ($\overline{HOLD}$)

The hold ($\overline{HOLD}$) signal is used to pause any serial communications with the device without deselecting the device.

2.6 Write protect ($\overline{W}$)

This pin is used to write-protect the status register.

2.7 V_{SS} ground

V_{SS} is the reference for all signals, including the V_{CC} supply voltage.

2.8 V_{CC} supply voltage

V_{CC} is the supply voltage pin. Refer to Section 3.1 Active power and standby power modes and to Section 5.1 Supply voltage (VCC).

3 Operating features

3.1 Active power and standby power modes

When chip select ($\overline{S}$) is low, the device is selected and in the active power mode.

When chip select ($\overline{S}$) is high, the device is deselected. If a write cycle is not currently in progress, the device then goes in to the standby power mode, and the device consumption drops to I_{CC1}, as specified in Table 14.

3.2 SPI modes

The device can be driven by a microcontroller with its SPI peripheral running in either of the two following modes:

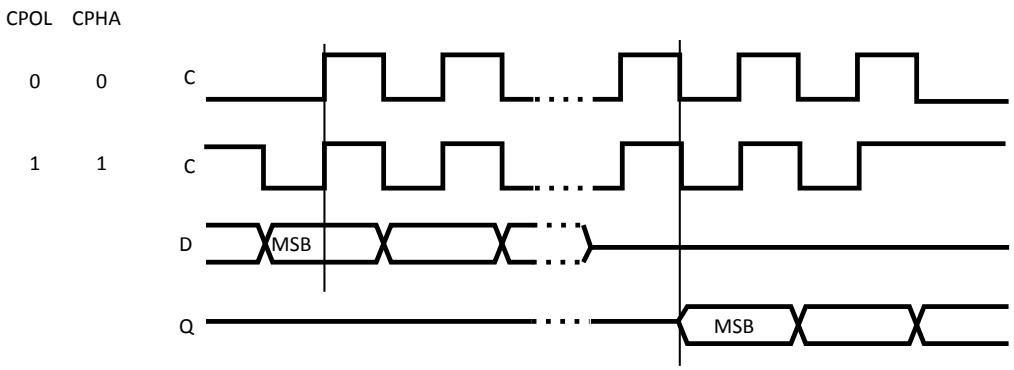
- CPOL=0, CPHA=0
- CPOL=1, CPHA=1

For these two modes, input data is latched in on the rising edge of serial clock (C), and output data is available from the falling edge of serial clock (C).

The difference between the two modes, as shown in Figure 3, is the clock polarity when the bus master is in stand-by mode and not transferring data:

- C remains at 0 for (CPOL=0, CPHA=0)
- C remains at 1 for (CPOL=1, CPHA=1)

Figure 3. SPI modes supported

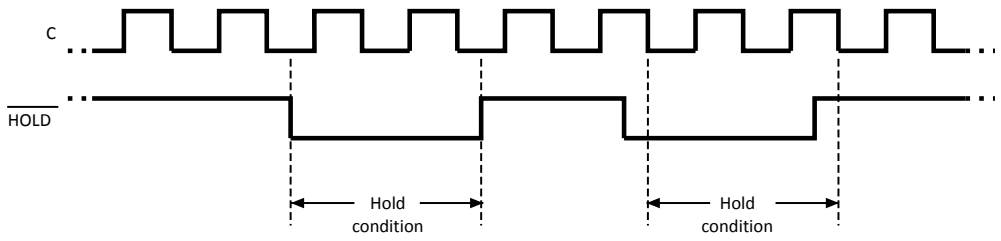


3.3 Hold mode

The hold ($\overline{\text{HOLD}}$) signal is used to pause any serial communications with the device without resetting the clocking sequence.

The hold mode starts when the hold ($\overline{\text{HOLD}}$) signal is driven low and the serial clock (C) is low (as shown in Figure 4). During the hold mode, the serial data output (Q) is high impedance, and the signals present on serial data input (D) and serial clock (C) are not decoded. The hold mode ends when the hold ($\overline{\text{HOLD}}$) signal is driven high and the serial clock (C) is or becomes low.

Figure 4. Hold mode activation



Deselecting the device while it is in hold mode resets the paused communication.

3.4 Protocol control and data protection

3.4.1 Protocol control

The chip select ($\overline{\text{S}}$) input offers a built-in safety feature, as the $\overline{\text{S}}$ input is edge-sensitive as well as level-sensitive: after power-up, the device is not selected until a falling edge has first been detected on chip select ($\overline{\text{S}}$). This ensures that chip select ($\overline{\text{S}}$) must have been high prior to going low, in order to start the first operation.

For Write commands (WRITE, WRSR, WRID, LID) to be accepted and executed:

- the write enable latch (WEL) bit must be set by a write enable (WREN) instruction
- a falling edge and a low state on chip select ($\overline{\text{S}}$) during the whole command must be decoded
- instruction, address and input data must be sent as multiple of eight bits
- the command must include at least one data byte
- chip select ($\overline{\text{S}}$) must be driven high exactly after a data byte boundary

Write command can be discarded at any time by a rising edge on chip select ($\overline{\text{S}}$) outside of a byte boundary.

To execute read commands (READ, RDSR, RDID, RDLS), the device must decode:

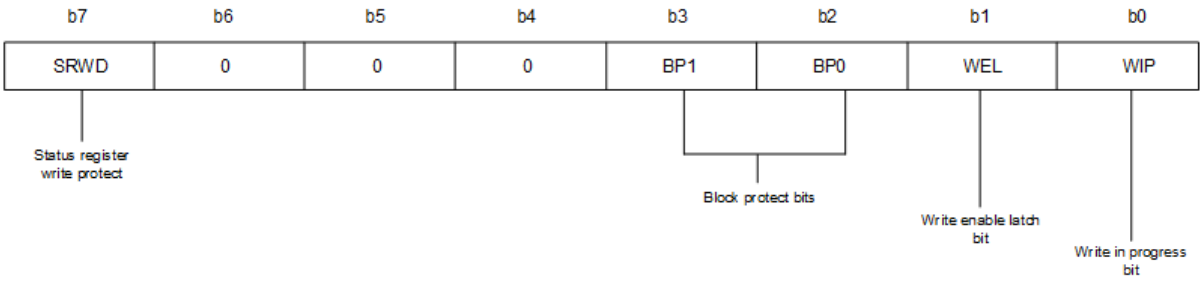
- a falling edge and a low level on chip select ($\overline{\text{S}}$) during the whole command
- instruction and address as multiples of eight bits (byte)

From this step, data bits are shifted out until the rising edge on chip select ($\overline{\text{S}}$).

3.4.2 Status register and data protection

The status register format is shown in Figure 5 and the status and control bits of the status register are as follows:

Figure 5. Status register format



Note: Bits b6, b5, and b4 are always read as 0.

WIP bit

The WIP bit (write in progress) is a read-only flag that indicates the ready/busy state of the device. When a write command (WRITE, WRSR, WRID) has been decoded and a write cycle (t_W) is in progress, the device is busy and the WIP bit is set to 1. When WIP=0, the device is ready to decode a new command.

During a write cycle, reading continuously the WIP bit allows to detect when the device becomes ready (WIP=0) to decode a new command.

Note: During a write lock ID, the device is busy but the WIP bit stays stable set to 0.

WEL bit

The WEL bit (write enable latch) bit is a flag that indicates the status of the internal write enable latch. When WEL is set to 1, the Write instructions (WRITE, WRSR, WRID, LID) are executed; when WEL is set to 0, any decoded Write instruction is not executed.

The WEL bit is set to 1 with the WREN instruction. The WEL bit is reset to 0 after the following events:

- Write disable (WRDI) instruction completion
- Write instructions (WRITE, WRSR, WRID, LID) completion including the write cycle time t_W
- Power-up

BP1, BP0 bits

The block protect bits (BP1, BP0) are non-volatile. BP1,BP0 bits define the size of the memory block to be protected against write instructions, as defined in Figure 5. These bits are written with the write status register (WRSR) instruction, provided that the status register is not protected (refer to “SRWD bit and W input signal”).

Table 2. **Write-protected block size**

Status register bits		Protected block	Protected array addresses
BP1	BP0		
0	0	None	None
0	1	Upper quarter	6.00.00h - 7.FF.FFh
1	0	Upper half	4.00.00h - 7.FF.FFh
1	1	Whole memory	0.00.00h - 7.FF.FFh plus Identification page

SRWD bit and $\overline{W}$ input signal

The status register write disable (SRWD) bit is operated in conjunction with the write protect pin ($\overline{W}$) signal. When the SRWD bit is written to 0, it is possible to write the status register, regardless of whether the pin write protect ($\overline{W}$) is driven high or low.

When the SRWD bit is written to 1, two cases have to be considered, depending on the state of the $\overline{W}$ input pin:

- Case 1: if pin $\overline{W}$ is driven high, it is possible to write the status register.
- Case 2: if pin $\overline{W}$ is driven low, it is not possible to write the status register (WRSR is discarded) and therefore SRWD,BP1,BP0 bits cannot be changed (the size of the protected memory block defined by BP1,BP0 bits is frozen).

Case 2 can be entered in either sequence:

- Writing SRWD bit to 1 after driving pin $\overline{W}$ low, or
- Driving pin $\overline{W}$ low after writing SRWD bit to 1.

The only way to exit case 2 is to pull pin $\overline{W}$ high.

Note: if pin $\overline{W}$ is permanently tied high, the status register cannot be write-protected.

The protection features of the device are summarized in Table 3.

Table 3. **Protection modes**

SRWD bit	W signal	Status
0	X	Status register is writable
1	1	
1	0	Status Register is write-protected

3.5 Identification page

The M95M04-A125 and M95M04-A145 offer an identification page (512 bytes) in addition to the 4 Mbits memory. The identification page contains two fields:

- Device identification: the three first byte are programmed by STMicroelectronics with the device identification code, as shown in Table 4.
- Application parameters: the bytes after the device identification code are available for application specific data.

Note: If the end application does not need to read the device identification code, this field can be overwritten and used to store application-specific data. Once the application-specific data are written in the Identification page, the whole Identification page should be permanently locked in Read-only mode.

The read, write, lock identification page instructions are detailed in Section 4 Instructions.

Table 4. **Device identification bytes**

Address in identification page	Content	Value
00h	ST manufacturer code	20h
01h	SPI family code	00h
02h	Memory density code	13h (4 Mbit)

4 Instructions

Each command is composed of bytes (MSBit transmitted first), initiated with the instruction byte, as summarized in Table 5.

If an invalid instruction is sent (one not contained in Table 5), the device automatically enters a Wait state until deselected.

Table 5. Instruction set

Instruction	Description	Instruction format
WREN	Write enable	0000 0110
WRDI	Write disable	0000 0100
RDSR	Read status register	0000 0101
WRSR	Write status register	0000 0001
READ	Read from memory array	0000 0011
WRITE	Write to memory array	0000 0010
RDID	Read identification page	1000 0011
WRID	Write identification page	1000 0010
RDLS	Reads the identification page lock status.	1000 0011
LID	Locks the identification page in read-only mode.	1000 0010

For read and write commands to memory array and identification page, the address is defined by three bytes as explained in Table 6.

Table 6. Significant bits within the address bytes

Instruction	Upper address byte								Middle address byte								Lower address byte							
	b23	b22	b21	b20	b19	b18	b17	b16	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
READ or WRITE	X(1)	X	X	X	X	A18(2)	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
RDID or WRID	X	X	X	X	X	X	X	X	X	X	X	X	X	0	X	A8	A7	A6	A5	A4	A3	A2	A1	A0
RDLS or LID	X	X	X	X	X	X	X	X	X	X	X	X	X	1	X	X	X	X	X	X	X	X	X	X

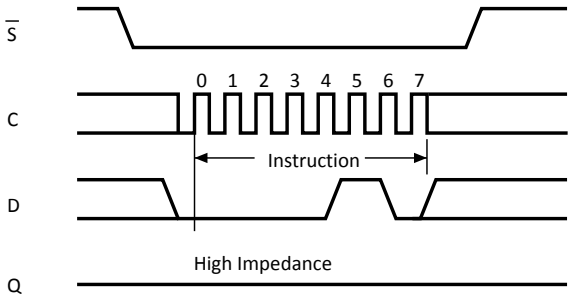
1. *X: bit is Don't care*
2. *A: Significant address bit*

4.1 Write enable (WREN)

The WREN instruction must be decoded by the device before a write instruction (WRITE, WRSR, WRID or LID).

As shown in Figure 6, to send this instruction to the device, chip select ($\overline{S}$) is driven low, the bits of the instruction byte are shifted in (MSB first) on serial data input (D) after what the chip select ($\overline{S}$) input is driven high and the WEL bit is set (status register bit).

Figure 6. Write enable (WREN) sequence



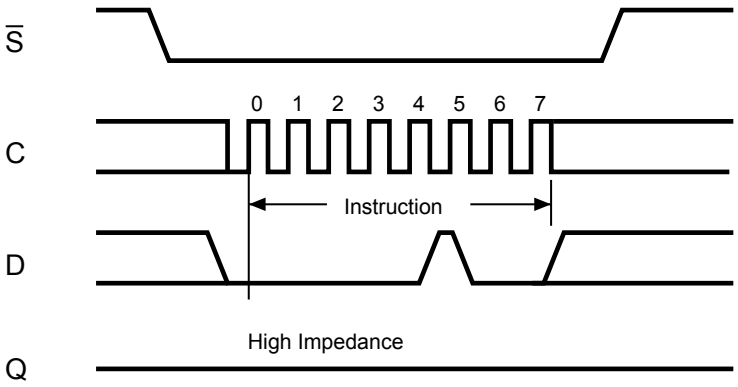
4.2 Write disable (WRDI)

One way of resetting the WEL bit (in the status register) is to send a write disable instruction to the device.

As shown in Figure 7, to send this instruction to the device, chip select ($\overline{S}$) is driven low, and the bits of the instruction byte are shifted in (MSB first), on serial data input (D), after what the chip select ($\overline{S}$) input is driven high and the WEL bit is reset (status register bit).

If a write cycle is currently in progress, the WRDI instruction is decoded and executed and the WEL bit is reset to 0 with no effect on the ongoing write cycle.

Figure 7. Write disable (WRDI) sequence



4.3 Read status register (RDSR)

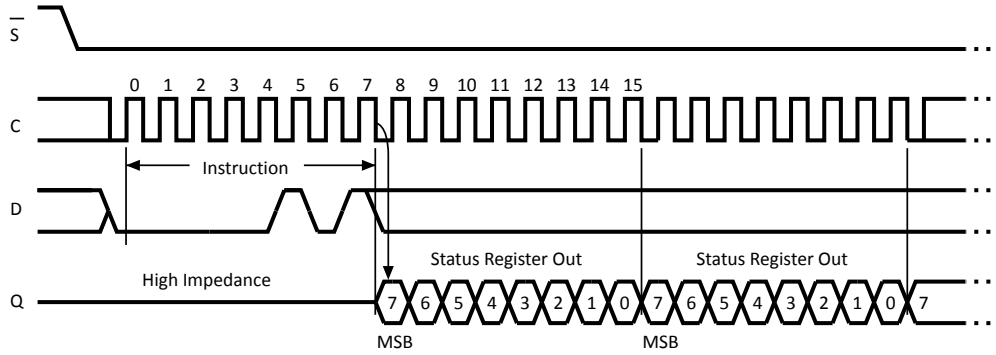
The read status register (RDSR) instruction is used to read the content of the status register.

As shown in Figure 8, to send this instruction to the device, chip select ($\overline{S}$) is first driven low. The bits of the instruction byte are shifted in (MSB first) on serial data Input (D), the status register content is then shifted out (MSB first) on serial data output (Q).

If chip select ($\overline{S}$) continues to be driven low, the status register content is continuously shifted out.

The status register can always be read, even if a Write cycle (t_W) is in progress. The status register functionality is detailed in Section 3.4.2 Status register and data protection.

Figure 8. Read status register (RDSR) sequence



4.4 Write status register (WRSR)

The write status register (WRSR) instruction allows new values to be written to the status register. Before it can be accepted, a write enable (WREN) instruction must previously have been executed.

The write status register (WRSR) instruction is entered (MSB first) by driving chip select ($\overline{S}$) low, sending the instruction code followed by the data byte on serial data input (D), and driving the chip select ($\overline{S}$) signal high.

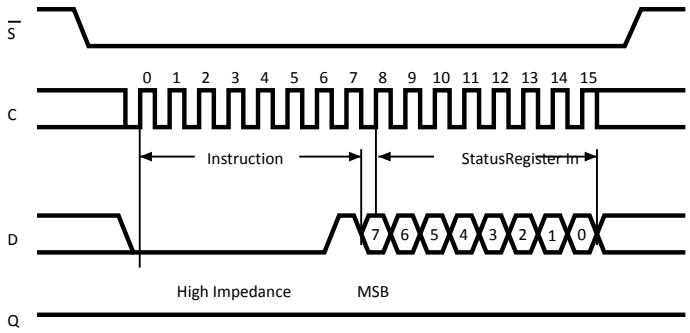
The contents of the SRWD and BP1, BP0 bits are updated after the completion of the WRSR instruction, including the write cycle (t_W).

The write status register (WRSR) instruction has no effect on the b6, b5, b4, b1 and b0 bits in the status register (see Section 3.4.2).

The status register functionality is detailed in Section 3.4.2 Status register and data protection.

The instruction is not accepted, and is not executed, if a write cycle is currently in progress.

Figure 9. Write status register (WRSR) sequence



4.5 Read from memory array (READ)

The READ instruction is used to read the content of the memory.

As shown in Figure 10, to send this instruction to the device, chip select ($\overline{S}$) is first driven low.

The bits of the instruction byte and address bytes are shifted in (MSB first) on serial data input (D) and the addressed data byte is then shifted out (MSB first) on serial data output (Q). The first addressed byte can be any byte within any page.

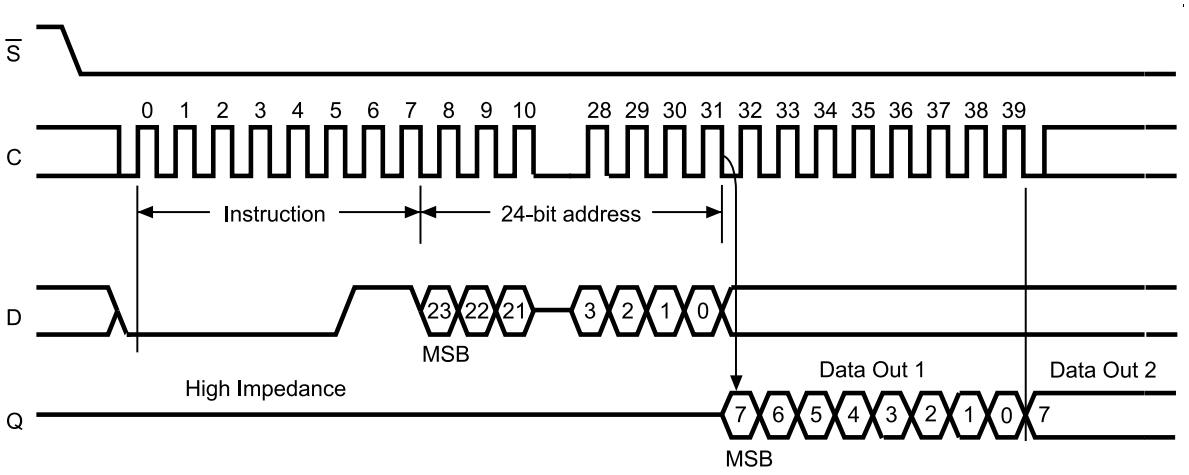
If chip select ($\overline{S}$) continues to be driven low, the internal address register is automatically incremented, and the next byte of data is shifted out. The whole memory can therefore be read with a single READ instruction.

When the highest address is reached, the address counter rolls over to zero, allowing the read cycle to be continued indefinitely.

The read cycle is terminated by driving chip select ($\overline{S}$) high at any time when the data bits are shifted out on serial data output (Q).

The instruction is not accepted, and is not executed, if a write cycle is currently in progress.

Figure 10. Read from memory array (READ) sequence



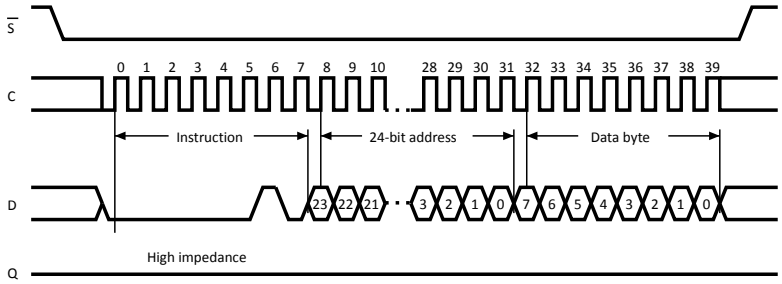
1. Depending on the memory size, as shown in Table 6, the most significant address bits are don't care.

4.6 Write to memory array (WRITE)

The WRITE instruction is used to write new data in the memory.

As shown in Figure 11, to send this instruction to the device, chip select ($\overline{S}$) is first driven low. The bits of the instruction byte, address byte, and at least one data byte are then shifted in (MSB first), on serial data input (D). The instruction is terminated by driving chip select ($\overline{S}$) high at a data byte boundary. Figure 11 shows a single byte write.

Figure 11. Byte write (WRITE) sequence



Note: Depending on the memory size, as shown in Table 6, the most significant address bits are "Don't Care".

A page write is used to write several bytes inside a page, with a single internal write cycle.

For a page write, chip select ($\overline{S}$) has to remain low, as shown in Figure 12, so that the next data bytes are shifted in. Each time a new data byte is shifted in, the least significant bits of the internal address counter are incremented. If the address counter exceeds the page boundary (the page size is 512 bytes), the internal address pointer rolls over to the beginning of the same page where next data bytes will be written. If more than 512 byte are received, only the last 512 bytes are written.

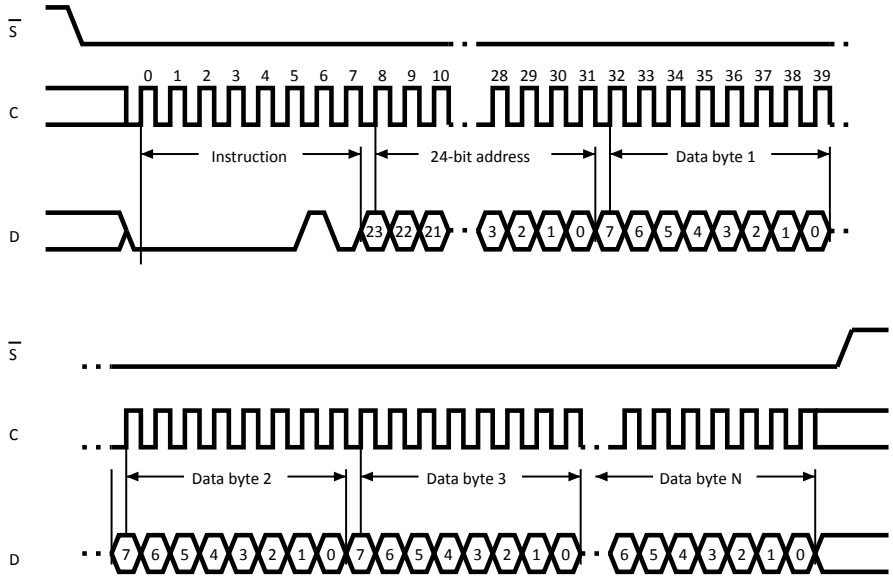
For both byte write and page write, the self-timed write cycle starts from the rising edge of chip select ($\overline{S}$), and continues for a period t_W (as specified in Table 15 and in Table 16).

The instruction is discarded, and is not executed, under the following conditions:

- if a write cycle is already in progress
- if the addressed page is in the region protected by the block protect (BP1 and BP0) bits
- if one of the conditions defined in Section 3.4.1 Protocol control is not satisfied

Note: The self-timed write cycle t_W is internally executed as a sequence of two consecutive events: [erase addressed byte(s)], followed by [program addressed byte(s)]. An erased bit is read as "0" and a programmed bit is read as "1".

Figure 12. Page write (WRITE) sequence



Note: Depending on the memory size, as shown in Table 6, the most significant address bits are "Don't Care".

4.7 Read identification page (RDID)

The read identification page instruction is used to read the identification page (additional page of 512 bytes which can be written and later permanently locked in read-only mode).

The chip select ($\overline{S}$) signal is first driven low, the bits of the instruction byte and address bytes are then shifted in (MSB first) on serial data input (D). Address bit A10 must be 0 and the other upper address bits are Don't Care (it might be easier to define these bits as 0. The data byte pointed to by the lower address bits [A8:A0] is shifted out (MSB first) on serial data output (Q).

The first byte addressed can be any byte within the identification page.

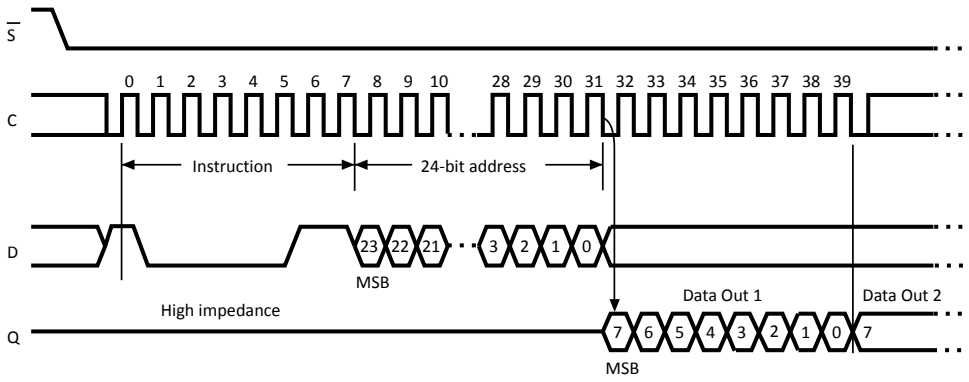
If chip select ($\overline{S}$) continues to be driven low, the internal address register is automatically incremented and the byte of data at the new address is shifted out.

Note that there is no roll over feature in the identification page. The address of bytes to read must not exceed the page boundary.

The read cycle is terminated by driving chip select ($\overline{S}$) high. The rising edge of the chip select ($\overline{S}$) signal can occur at any time when the data bits are shifted out.

The instruction is not accepted, and is not executed, if a write cycle is currently in progress.

Figure 13. Read identification page sequence



The first three bytes of the identification page offer information about the device itself. Refer to Section 3.5 Identification page for more information.

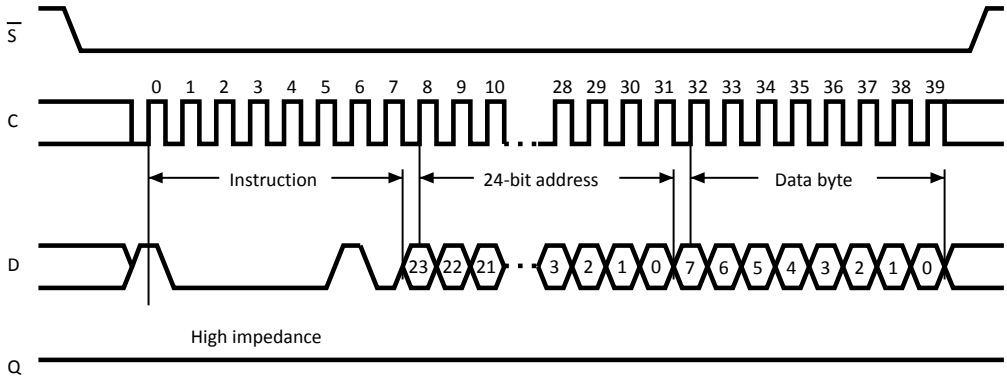
4.8 Write identification page (WRID)

The write identification page instruction is used to write the identification page (additional page of 512 bytes, which can also be permanently locked in read-only mode).

The chip select signal ($\overline{S}$) is first driven low, and then the bits of the instruction byte, address bytes, and at least one data byte are shifted in (MSB first) on serial data input (D). Address bit A10 must be 0 and the other upper address bits are "Don't Care" (it might be easier to define these bits as 0. The lower address bits [A8:A0] define the byte address inside the identification page.

The self-timed write cycle starts from the rising edge of chip select ($\overline{S}$), and continues for a period t_W (as specified in Table 15 and in Table 16).

Figure 14. Write identification page sequence



Note: The first three bytes of the identification page offer the device identification code (refer to Section 3.5 Identification page for more information). Using the WRID command on these first three bytes overwrites the device identification code.

The instruction is discarded, and is not executed, under the following conditions:

- If a write cycle is already in progress
- If the block protect bits (BP1,BP0) = (1,1)
- If one of the conditions defined in Section 3.4.1 Protocol control is not satisfied.

4.9 Read lock status (RDLS)

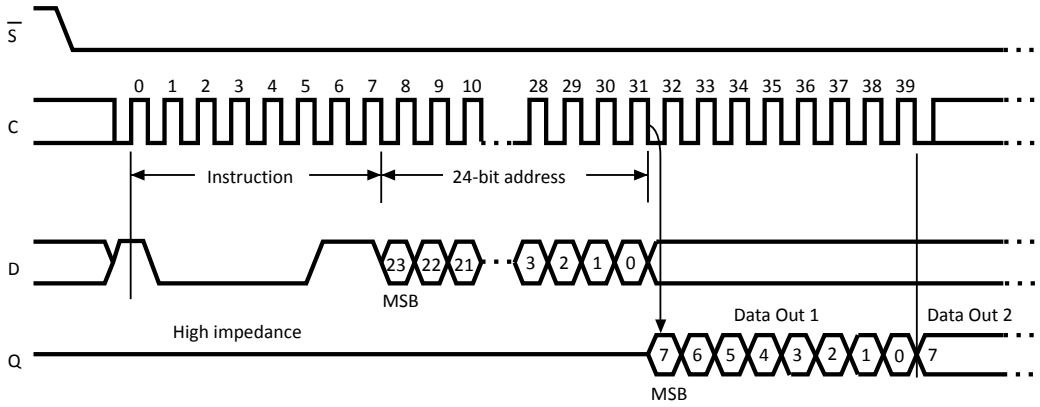
The read lock status instruction is used to read the lock status.

To send this instruction to the device, chip select ($\overline{S}$) first has to be driven low. The bits of the instruction byte and address bytes are then shifted in (MSB first) on serial data input (D). Address bit A10 must be 1; all other address bits are "Don't Care" (it might be easier to define these bits as 0. The lock bit is the LSB (least significant bit) of the byte read on serial data output (Q). It is at '1' when the lock is active and at '0' when the lock is not active. If chip select ($\overline{S}$) continues to be driven low, the same data byte is shifted out.

The read cycle is terminated by driving chip select ($\overline{S}$) high. The instruction sequence is shown in Figure 15.

The read lock status instruction is not accepted and not executed if a write cycle is currently in progress.

Figure 15. Read lock status sequence

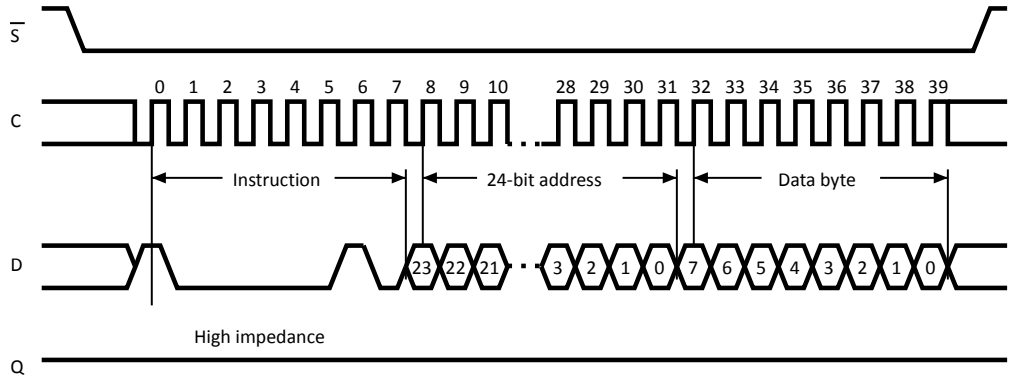


4.10 Lock identification page (LID)

The lock identification page (LID) command is used to permanently lock the identification page in read-only mode.

The LID instruction is issued by driving chip select ($\overline{S}$) low, sending (MSB first) the instruction code, the address and a data byte on serial data input (D), and driving chip select ($\overline{S}$) high. In the address sent, A10 must be equal to 1. All other address bits are "Don't Care" (it might be easier to define these bits as 0. The data byte sent must have the b0 bit equal to 1 (b0 = 1) and the others value of the bits b7 to b1 are "Don't Care". The data byte sent must be equal to the binary value xxxx xxx1, where x = Don't care. The LID instruction is terminated by driving chip select (S) high at a data byte boundary, otherwise, the instruction is not executed.

Figure 16. Lock ID sequence



Driving chip select ($\overline{S}$) high at a byte boundary of the input data triggers the self-timed write cycle which duration is t_W (specified in Table 15 and in Table 16). The instruction sequence is shown in Figure 16.

The instruction is discarded, and is not executed, under the following conditions:

- If a write cycle is already in progress
- If the block protect bits (BP1,BP0) = (1,1)
- If one of the conditions defined in Section 3.4.1 Protocol control is not satisfied.

5 Application design recommendations

5.1 Supply voltage (V_{CC})

5.1.1 Operating supply voltage (V_{CC})

Prior to selecting the memory and issuing instructions to it, a valid and stable V_{CC} voltage within the specified [$V_{CC(min)}$, $V_{CC(max)}$] range must be applied (see Table 9 and Table 10).

This voltage must remain stable and valid until the end of the transmission of the instruction and, for a write instruction, until the completion of the internal Write cycle (t_W). In order to secure a stable DC supply voltage, it is recommended to decouple the V_{CC} line with a suitable capacitor (usually of the order of 10 nF to 100 nF) close to the V_{CC}/V_{SS} package pins.

5.1.2 Power-up conditions

When the power supply is turned on, V_{CC} continuously rises from V_{SS} to V_{CC}. During this time, the chip select ($\overline{S}$) line is not allowed to float but should follow the V_{CC} voltage. The $\overline{S}$ line must be connected to V_{CC} via a suitable pull-up resistor (see Figure 17).

The V_{CC} voltage has to rise continuously from 0 V up to the minimum V_{CC} operating voltage defined in Table 14.

In order to prevent inadvertent write operations during power-up, a power-on-reset (POR) circuit is included.

At power-up, the device does not respond to any instruction until V_{CC} reaches the internal threshold voltage (this threshold is defined in the Table 14 as VRES).

When V_{CC} passes over the POR threshold, the device is reset and in the following state:

- in the standby power mode
- deselected
- Status register values:
  - Write enable Latch (WEL) bit is reset to 0.
  - Write in progress (WIP) bit is reset to 0.
  - SRWD, BP1 and BP0 bits remain unchanged (non-volatile bits).
- not in the hold condition

As soon as the V_{CC} voltage has reached a stable value within [V_{CC}(min), V_{CC}(max)] range, the device is ready for operation.

5.1.3 Power-down

At power down, the power-on-reset (POR) circuit resets and locks the device as soon as the V_{CC} reached the internal threshold voltage.

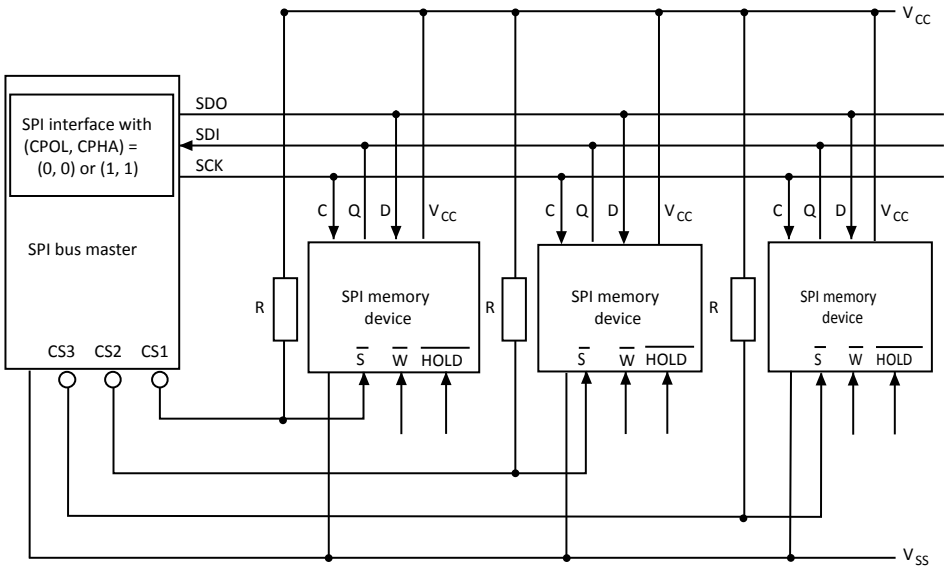
During power-down (continuous decrease in the V_{CC} supply voltage below the minimum V_{CC} operating voltage defined in Table 14), the device must be:

- deselected (chip select ($\overline{S}$) should be allowed to follow the voltage applied on V_{CC}),
- in standby power mode (there should not be any internal write cycle in progress).

5.2 Implementing devices on SPI bus

Figure 17 shows an example of three devices, connected to the SPI bus master. Only one device is selected at a time, so that only the selected device drives the serial data output (Q) line. All the other devices outputs are then in high impedance.

Figure 17. Bus master and memory devices on the SPI bus



Note: The write protect ($\overline{W}$) and hold ($\overline{HOLD}$) signals must be driven high or low as appropriate.

A pull-up resistor connected on each $\overline{S}$ input (represented in Figure 17) ensures that each device is not selected if the bus master leaves the $\overline{S}$ line in the high impedance state.

5.3 Cycling with error correction code (ECCx4)

The error correction code (ECC) is an internal logic function which is transparent for the SPI communication protocol.

The ECC logic is implemented on each group of four EEPROM bytes (a group of four bytes is located at addresses [4*N, 4*N+1, 4*N+2, 4*N+3], where N is an integer).

Even if the ECC function is performed on groups of four bytes, a single byte can be written/cycled independently. In this case, the ECC function also writes/cycles the three other bytes located in the same group (a group of four bytes is located at addresses [4*N, 4*N+1, 4*N+2, 4*N+3], where N is an integer). As a consequence, the maximum cycling budget is defined at group level and the cycling can be distributed over the 4 bytes of the group: the sum of the cycles seen by byte0, byte1, byte2 and byte3 of the same group must remain below the maximum value defined in Table 8.

6 Delivery state

The device is delivered with:

- the memory array set to all 1s (each byte = FFh),
- The status register bits set to '0' (byte = 00h),
- Identification page: the first three bytes define the device identification code (value defined in Table 4). The content of the following bytes is "Don’t care".

7 Absolute maximum ratings

Stressing the device outside the ratings listed in Table 7 may cause permanent damage to the device. These are stress ratings only, and operation of the device at these, or any other conditions outside those indicated in the operating sections of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 7. Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Unit
T_{STG}	Storage temperature	-65	150	°C
T_{AMR}	Ambient operating temperature	-40	150	°C
T_{LEAD}	Lead temperature during soldering	See note (1)		°C
V_O	Voltage on Q pin	-0.50	V_{CC} + 0.5	V
V_I	Input voltage	-0.50	6.5	V
I_{OL}	DC output current (Q = 0)	-	5	mA
I_{OH}	DC output current (Q = 1)	-	5	mA
V_{CC}	Supply voltage	- 0.50	6.5	V
V_{ESD}	Electrostatic pulse (human body model)(2)	-	4000	V

1. *Compliant with JEDEC Std J-STD-020 (for small body, Sn-Pb or Pb-free assembly), the ST ECOPACK 7191395 specification, and the European directive on Restrictions of Hazardous Substances (RoHS directive 2011/65/EU of July 2011).*
2. *Positive and negative pulses applied on pin pairs, in accordance with AEC-Q100-002 (compliant with ANSI/ESDA/JEDEC JS-001, C1=100 pF, R1=1500 Ω, R2=500 Ω)*

8 DC and AC parameters

This section summarizes the operating conditions and the DC/AC characteristics of the device.

Table 8. Cycling performance by groups of 4 bytes

Symboil	Parameter	Conditions	Min.	Max.	Unit
NCycle	Write cycles endurance(1)(2)	TA ≤ 25 °C, 2.9 V ≤ V_{CC} ≤ 5.5 V	-	1 000 000	Write cycles(3)
		TA ≤ 85 °C, 2.9 V ≤ V_{CC} ≤ 5.5 V	-	500 000	
		TA ≤ 125 °C, 2.9 V ≤ V_{CC} ≤ 5.5 V	-	200 000	
		TA ≤ 145 °C(4), 2.9 V ≤ V_{CC} ≤ 5.5 V	-	100 000	

1. *The write cycle endurance is defined for groups of four data bytes located at addresses [4*N, 4*N+1, 4*N+2, 4*N+3] where N is an integer, or for the status register byte (refer also to Cycling with error correction code (ECCx4)). The write cycle endurance is evaluated by characterization – not tested in production.*
2. *In case of intensive write status register in the application, contact you local ST sales*
3. *A write cycle is executed when either a page write, a byte write, a WRSR, or a WRID instruction is decoded. When using the byte write, the page write or the WRID, refer also to Cycling with error correction code (ECCx4).*
4. *For temperature range 4 only.*

Table 9. Operating conditions (voltage range W, temperature range 4)

Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{CC}	Supply voltage	-	2.9	5.5	V
T_A	Ambient operating temperature	-	-40	145	°C
f_C	Operating clock frequency	5.5 V ≥ V_{CC} ≥ 2.9 V, capacitive load on Q pin ≤ 100 pF	-	10	MHz

Table 10. Operating conditions (voltage range W, temperature range 3)

Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{CC}	Supply voltage	-	2.9	5.5	V
T_A	Ambient operating temperature	-	-40	125	°C
f_C	Operating clock frequency	5.5 V ≥ V_{CC} ≥ 2.9 V, capacitive load on Q pin ≤ 100 pF	-	10	MHz

Table 11. AC measurement conditions

Symbol	Parameter	Min.	Max.	Unit
C_L	Load capacitance	-	100	pF
-	Input rise and fall times	-	25	ns
-	Input pulse voltages	0.2 V_{CC} to 0.8 V_{CC}		V
-	Input and output timing reference voltages	0.3 V_{CC} to 0.7 V_{CC}		V

Figure 18. **AC measurement I/O waveform**

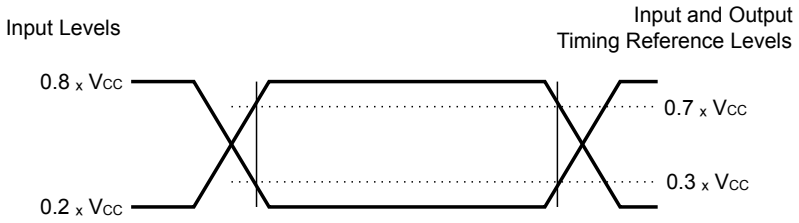


Table 12. **Memory cell data retention**

Parameter	Test conditions	Data retention performance per cell
Data retention(1)	2.9 V ≤ V_{CC} ≤ 5.5 V	10 years at 55 °C after max cycling

1. *The data retention endurance is evaluated by characterization – not tested in production.*

Table 13. **Capacitance**

Symbol	Parameter	Test conditions (1)	Min.	Max.	Unit
C_{OUT}	Output capacitance (Q)	V_{OUT} = 0 V	-	8	pF
C_{IN}	Input capacitance (D)	V_{IN} = 0 V	-	8	pF
	Input capacitance (other pins)	V_{IN} = 0 V	-	6	pF

1. *Sampled only, not 100% tested, at TA = 25 °C and at a frequency of 5 MHz.*

Table 14. DC characteristics

Symbol	Parameter	Specific test conditions (in addition to conditions specified in Table 9)	Min.	Max.	Unit
I_{LI}	Input leakage current	$V_{IN} = V_{SS}$ or V_{CC}	-	2	µA
I_{LO}	Output leakage current	$\overline{S} = V_{CC}$, $V_{OUT} = V_{SS}$ or V_{CC}	-	3	
I_{CC}	Supply current (Read)	V_{CC} = 3.6 V, f_C = 10 MHz, C = 0.1 V_{CC}/0.9 V_{CC}, Q = open	-	2	mA
		V_{CC} = 5.5 V, f_C = 10 MHz, C = 0.1 V_{CC}/0.9 V_{CC}, Q = open	-	3	
I_{CC0}(1)	Supply current (Write)	2.9 V < V_{CC} < 5.5 V, during t_W, $\overline{S} = V_{CC}$	-	2(2)	mA
I_{CC1}	Supply current (Standby power mode)	t° = amb, V_{CC} = 3.6 V, S = V_{CC} $V_{IN} = V_{SS}$ or V_{CC}	-	2	µA
		t° = amb, V_{CC} = 5.5 V, S = V_{CC} $V_{IN} = V_{SS}$ or V_{CC}	-	3	
		t° = 125 °C, V_{CC} = 3.6 V, S = V_{CC} $V_{IN} = V_{SS}$ or V_{CC}	-	10	
		t° = 125 °C, V_{CC} = 5.5 V, S = V_{CC} $V_{IN} = V_{SS}$ or V_{CC}	-	15	
		t° = 145 °C, V_{CC} = 3.6 V, S = V_{CC} $V_{IN} = V_{SS}$ or V_{CC}	-	20	
		t° = 145 °C, V_{CC} = 5.5 V, S = V_{CC} $V_{IN} = V_{SS}$ or V_{CC}	-	30	
V_{IL}	Input low voltage	-	–0.45	0.3 V_{CC}	V
V_{IH}	Input high voltage	-	0.7 V_{CC}	V_{CC}+1	
V_{OL}	Output low voltage	I_{OL} = 2 mA	-	0.4	
V_{OH}	Output high voltage	I_{OH} = –2 mA	0.8 V_{CC}	-	
V_{RES}(1)	Internal reset threshold voltage	-	0.5	1.5	

1. *Average value during the write cycle (t_W)*
2. *Characterized only, not 100% tested.*

Table 15. AC characteristics (5 MHz)

Symbol	Alt.	Parameter	Min.	Max.	Unit
f_C	f_{SCK}	Clock frequency	-	5	MHz
t_{SLCH}	t_{CSS1}	$\overline{S}$ active setup time	60	-	ns
t_{SHCH}	t_{CSS2}	$\overline{S}$ not active setup time	60	-	
t_{SHSL}	t_{CS}	$\overline{S}$ deselect time	90	-	
t_{CHSH}	t_{CSH}	$\overline{S}$ active hold time	60	-	
t_{CHSL}	-	$\overline{S}$ not active hold time	60	-	
t_{CH}(1)	t_{CLH}	Clock high time	80	-	
t_{CL}(1)	t_{CLL}	Clock low time	80	-	
t_{CLCH}(2)	t_{RC}	Clock rise time	-	2	µs
t_{CHCL}(2)	t_{FC}	Clock fall time	-	2	
t_{DVCH}	t_{DSU}	Data in setup time	20	-	ns
t_{CHDX}	t_{DH}	Data in hold time	20	-	
t_{HHCH}	-	Clock low hold time after HOLD not active	60	-	
t_{HLCH}	-	Clock low hold time after HOLD active	60	-	
t_{CLHL}	-	Clock low set-up time before HOLD active	0	-	
t_{CLHH}	-	Clock low set-up time before HOLD not active	0	-	
t_{SHQZ}(2)	t_{DIS}	Output disable time	-	80	
t_{CLQV}(3)	t_V	Clock low to output valid	-	80	
t_{CLQX}	t_{HO}	Output hold time	0	-	
t_{QLQH}(2)	t_{RO}	Output rise time	-	80	
t_{QHQL}(2)	t_{FO}	Output fall time	-	80	
t_{HHQV}	t_{LZ}	HOLD high to output valid	-	80	
t_{HLQZ}(2)	t_{HZ}	HOLD low to output high-Z	-	80	
t_W	t_{WC}	Write time	-	4(4)	ms

1. *t_{CH} + t_{CL} must never be lower than the shortest possible clock period, $1/f_C$(max).*
2. *Value evaluated by characterization – not tested in production.*
3. *t_{CLQV} must be compatible with t_{CL} (clock low time): if t_{SU} is the Read setup time of the SPI bus master, t_{CL} must be equal to (or greater than) t_{CLQV}+t_{SU}.*
4. *Write time for LID instruction is 10 ms.*

Table 16. AC characteristics (10 MHz)

Symbol	Alt.	Parameter	Min.	Max.	Unit
f_C	f_{SCK}	Clock frequency	-	10	MHz
t_{SLCH}	t_{CSS1}	S active setup time	30	-	ns
t_{SHCH}	t_{CSS2}	S not active setup time	30	-	
t_{SHSL}	t_{CS}	S deselect time	40	-	
t_{CHSH}	t_{CSH}	S active hold time	30	-	
t_{CHSL}	-	S not active hold time	30	-	
t_{CH}(1)	t_{CLH}	Clock high time	40	-	
t_{CL}(1)	t_{CLL}	Clock low time	40	-	
t_{CLCH}(2)	t_{RC}	Clock rise time	-	2	µs
t_{CHCL}(2)	t_{FC}	Clock fall time	-	2	
t_{DVCH}	t_{DSU}	Data in setup time	10	-	ns
t_{CHDX}	t_{DH}	Data in hold time	10	-	
t_{HHCH}	-	Clock low hold time after HOLD not active	30	-	
t_{HLCH}	-	Clock low hold time after HOLD active	30	-	
t_{CLHL}	-	Clock low set-up time before HOLD active	0	-	
t_{CLHH}	-	Clock low set-up time before HOLD not active	0	-	
t_{SHQZ}(2)	t_{DIS}	Output disable time	-	40	
t_{CLQV}(3)	t_V	Clock low to output valid	-	40	
t_{CLQX}	t_{HO}	Output hold time	0	-	
t_{QLQH}(2)	t_{RO}	Output rise time	-	40	
t_{QHQL}(2)	t_{FO}	Output fall time	-	40	
t_{HHQV}	t_{LZ}	HOLD high to output valid	-	40	
t_{HLQZ}(2)	t_{HZ}	HOLD low to output high-Z	-	40	
t_W	t_{WC}	Write time	-	4(4)	ms

1. *t_{CH} + t_{CL} must never be lower than the shortest possible clock period, $1/f_C$(max).*
2. *Value evaluated by characterization – not tested in production.*
3. *t_{CLQV} must be compatible with t_{CL} (clock low time): if t_{SU} is the Read setup time of the SPI bus master, t_{CL} must be equal to (or greater than) t_{CLQV}+t_{SU}.*
4. *Write time for LID instruction is 10 ms.*

Figure 19. **Serial input timing**

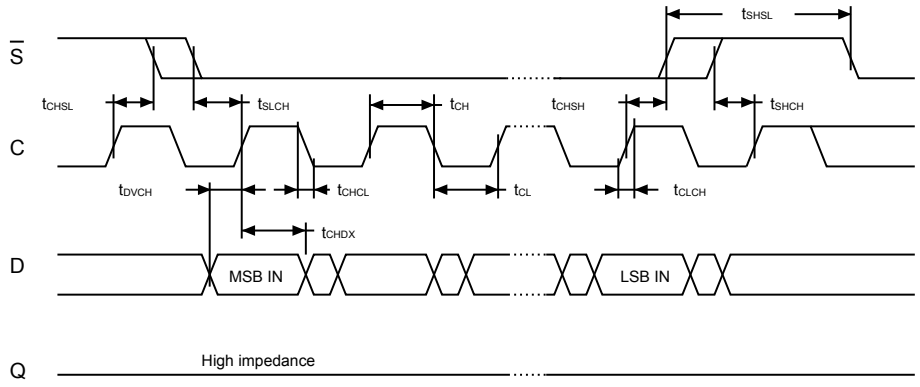


Figure 20. **Hold timing**

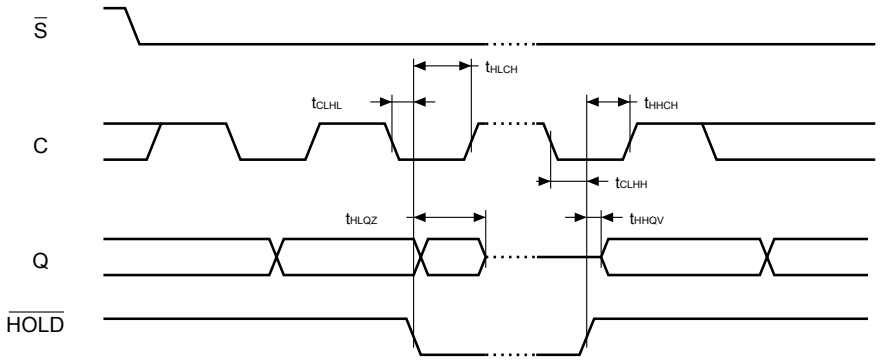
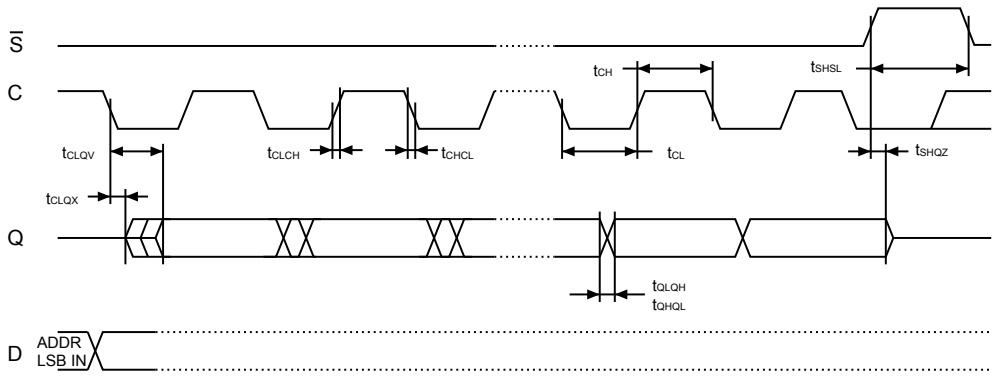


Figure 21. **Serial output timing**



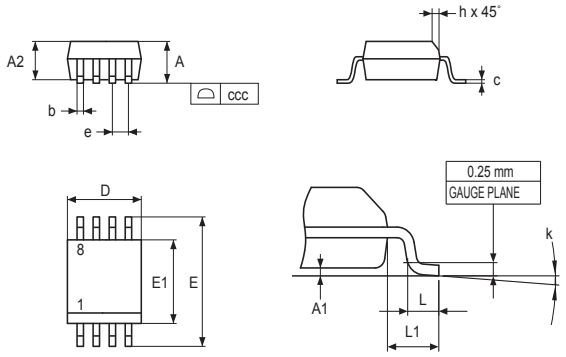
9 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

9.1 SO8N package information

SO8N is an 8-lead, 4.9 x 6 mm, plastic small outline, 150 mils body width, package.

Figure 22. SO8N – Outline



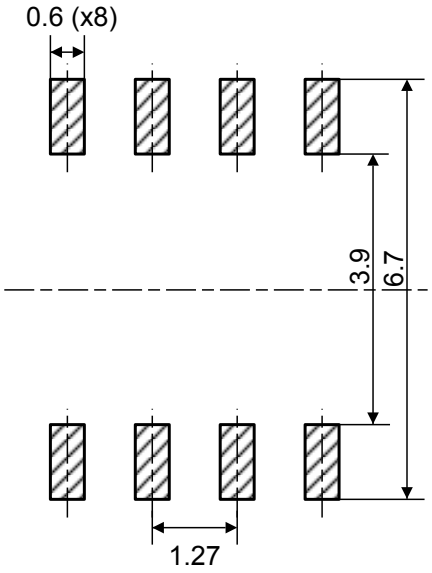
1. Drawing is not to scale.

Table 17. SO8N – Mechanical data

Symbol	millimeters			inches [1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	1.750	-	-	0.0689
A1	0.100	-	0.250	0.0039	-	0.0098
A2	1.250	-	-	0.0492	-	-
b	0.280	-	0.480	0.0110	-	0.0189
c	0.170	-	0.230	0.0067	-	0.0091
D	4.800	4.900	5.000	0.1890	0.1929	0.1969
E	5.800	6.000	6.200	0.2283	0.2362	0.2441
E1	3.800	3.900	4.000	0.1496	0.1535	0.1575
e	-	1.270	-	-	0.0500	-
h	0.250	-	0.500	0.0098	-	0.0197
k	0°	-	8°	0°	-	8°
L	0.400	-	1.270	0.0157	-	0.0500
L1	-	1.040	-	-	0.0409	-
ccc	-	-	0.100	-	-	0.0039

1. *Values in inches are converted from mm and rounded to four decimal digits.*

Figure 23. **SO8N - Recommended footprint**

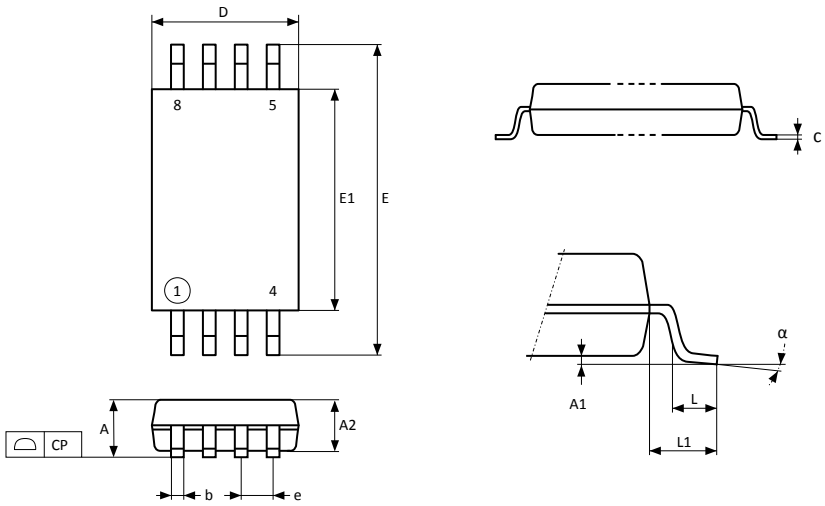


1. Dimensions are expressed in millimeters.

9.2 TSSOP8 package information

TSSOP8 is an 8-lead thin shrink small outline, 3 x 6.4 mm, 0.65 mm pitch, package.

Figure 24. TSSOP8 – Outline



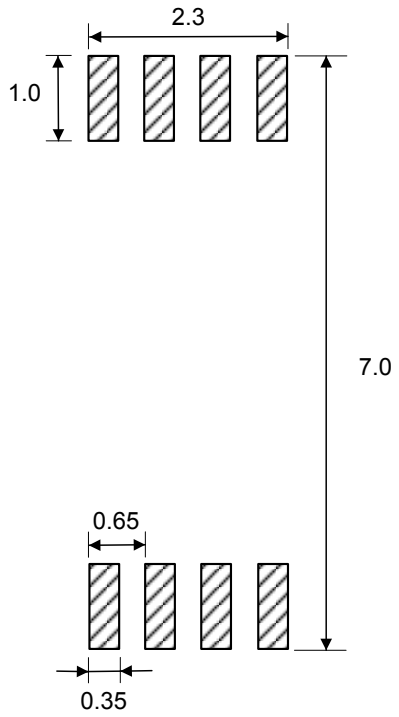
1. Drawing is not to scale.

Table 18. TSSOP8 – Mechanical data

Symbol	millimeters			inches (1)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	1.200	-	-	0.0472
A1	0.050	-	0.150	0.0020	-	0.0059
A2	0.800	1.000	1.050	0.0315	0.0394	0.0413
b	0.190	-	0.300	0.0075	-	0.0118
c	0.090	-	0.200	0.0035	-	0.0079
CP	-	-	0.100	-	-	0.0039
D	2.900	3.000	3.100	0.1142	0.1181	0.1220
e	-	0.650	-	-	0.0256	-
E	6.200	6.400	6.600	0.2441	0.2520	0.2598
E1	4.300	4.400	4.500	0.1693	0.1732	0.1772
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
α	0°	-	8°	0°	-	8°

1. *Values in inches are converted from mm and rounded to four decimal digits.*

Figure 25. **TSSOP8 – Recommended footprint**



1. Dimensions are expressed in millimeters.

10 Ordering information

Table 19. Ordering information scheme

Example:	M95	M04-D	W	DW	4	T	P	/V
Device type								
M95 = SPI serial access EEPROM								
Device function								
M04-D = 4 Mbits (512 Kbytes) plus identification page								
Operating voltage								
W = V_{CC} = 2.9 V to 5.5 V								
Package(1)								
MN = SO8 (150 mil width)								
DW = TSSOP8 (169 mil width)								
Device grade								
3 = -40 to 125 °C. Automotive grade. Device tested with high reliability certified flow								
4 = -40 to 145 °C. Automotive grade. Device tested with high reliability certified flow(2)								
Option								
T = Tape and reel packing								
blank = tube packing								
Planting technology								
P or G = ECOPACK2								
Process								
/V = Manufacturing technology code								

1. *All packages are ECOPACK2 (RoHS compliant and free of brominated, chlorinated and antimonyoxide flame retardants).*
2. *The high reliability certified flow (HRCF) is described in quality note QNEE9801. Please ask your nearest ST sales office for a copy.*

Note: For a list of available options (speed, package, etc.) or for further information on any aspect of the devices, please contact your nearest ST sales office.

Engineering samples

Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Revision history

Table 20. **Document revision history**

Date	Revision	Changes
04-Jan-2017	1	Initial release.
27-Apr-2020	2	Updated: • Features, Section 3.4.2 Status register and data protection, Section 4.10 Lock identification page (LID), Section 5.3 Cycling with error correction code (ECCx4) • Figure 1. Logic diagram • Table 6. Significant bits within the address bytes, Table 7. Absolute maximum ratings, Table 8. Cycling performance by groups of 4 bytes, Table 9. Operating conditions (voltage range W, temperature range 4), Table 10. Operating conditions (voltage range W, temperature range 3) , Table 14. DC characteristics, Table 15. AC characteristics (5 MHz), Table 16. AC characteristics (10 MHz), Table 19. Ordering information scheme Added: • Table 11. AC measurement conditions, Figure 20. Hold timing, Table 12. Memory cell data retention, Table 13. Capacitance Removed: Table 13. DC characteristics (voltage range W, temperature range 3), Table 17. AC characteristics (20 MHz)
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