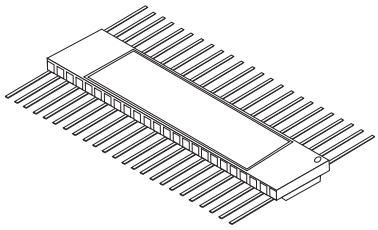
54VCXH162245

Rad-hard 3.6 V, 16-bit transceiver with series output resistors on A side

Datasheet - production data



Flat-48

Features

- 1.65 V to 3.6 V inputs and outputs
- High speed A outputs:
  - t_{PD} = 3.4 ns at V_{CC} = 3.0 to 3.6 V
  - t_{PD} = 4.3 ns at V_{CC} = 2.3 to 2.7 V
- Symmetrical impedance A output:
  - $|I_{OH}| = I_{OL}$ = 12 mA (min.) at V_{CC} = 3.0 V
  - $|I_{OH}| = I_{OL}$ = 8 mA (min.) at V_{CC} = 2.3 V
- High speed B outputs:
  - t_{PD} = 2.5 ns (max.) at V_{CC} = 3.0 to 3.6 V
  - t_{PD} = 3.2 ns (max.) at V_{CC} = 2.3 to 2.7 V
- Symmetrical impedance A output:
  - $|I_{OH}| = I_{OL}$ = 24 mA (min.) at V_{CC} = 3.0 V
  - $|I_{OH}| = I_{OL}$ = 18 mA (min.) at V_{CC} = 2.3 V
- Power down protection on inputs and outputs
- 26 Ω series resistors in A port output
- Operating voltage range:
  - V_{CC}(opr) = 1.65 V to 3.6 V
- Pin and function compatible with 54 series H162245
- Bus hold provided on both sides
- Cold spare function
- Latch-up performance exceeds 300 mA (JESD 17)
- ESD performance:
  - HBM > 2000 V (MIL STD 883 method 3015)
  - MM > 200 V
- 300 krad Mil1019.6 condition A (RHA QML qualification extension undergone)
- SEL-free and SET-free up to 110 Mev/cm2/mg
- QML qualified product
- SMD 5962-02508
- 100 mV typical input hysteresis
- Mass = 1.50 g

Description

The 54VCXH162245 is a low voltage CMOS 16-bit bus transceiver (3-state) fabricated with a sub-micron silicon gate and a five-layer metal wiring C²MOS technology. It is ideal for low power and very high speed (1.65 to 3.6 V) applications and can be interfaced to a 3.6 V signal environment for both inputs and outputs. This integrated circuit is intended for two-way asynchronous communication between data buses. The direction of data transmission is determined by digital input recorder (DIR) input. The two enable inputs, $n\overline{G}$, can be used to disable the device so that the buses are effectively isolated. The device circuits include 26 Ω series resistance in the A port outputs. These resistors reduce line noise in high-speed applications. Bus hold on data inputs is provided to eliminate the need for external pull-up or pull-down resistors. All inputs and outputs are equipped with protection circuits against static discharge, giving them 2 kV ESD immunity and transient excess voltage. All floating bus terminals during high Z state must be held HIGH or LOW.

This is information on a product in full production. www.st.com

Contents

1 Logic symbols and I/O equivalent circuit

Figure 1. IEC logic symbols

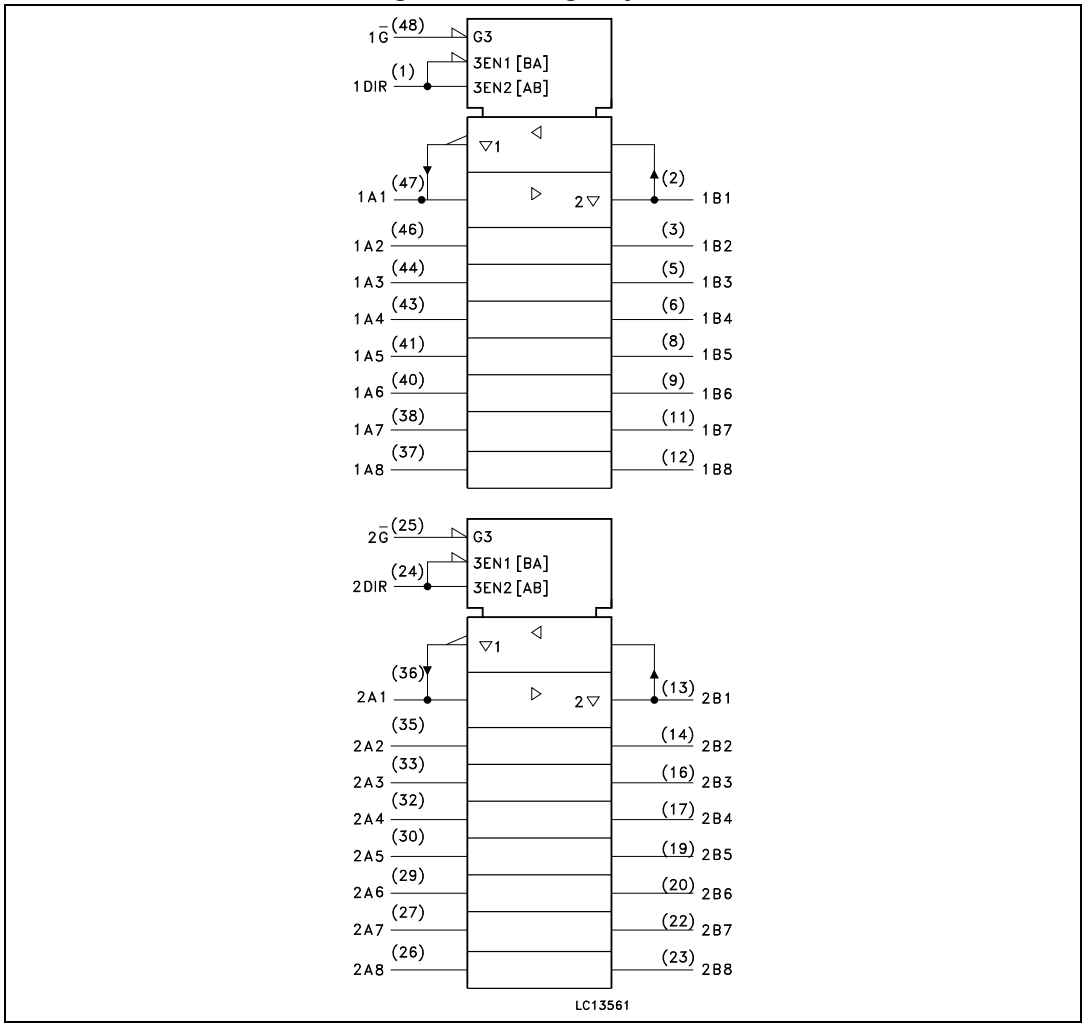
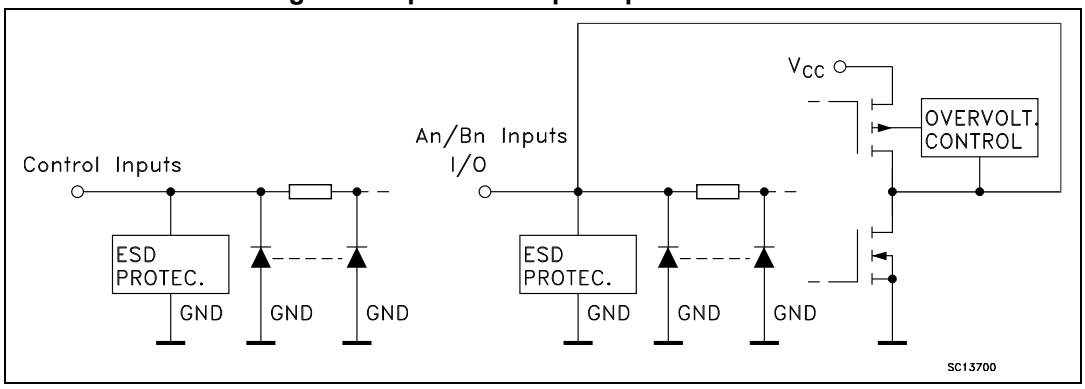


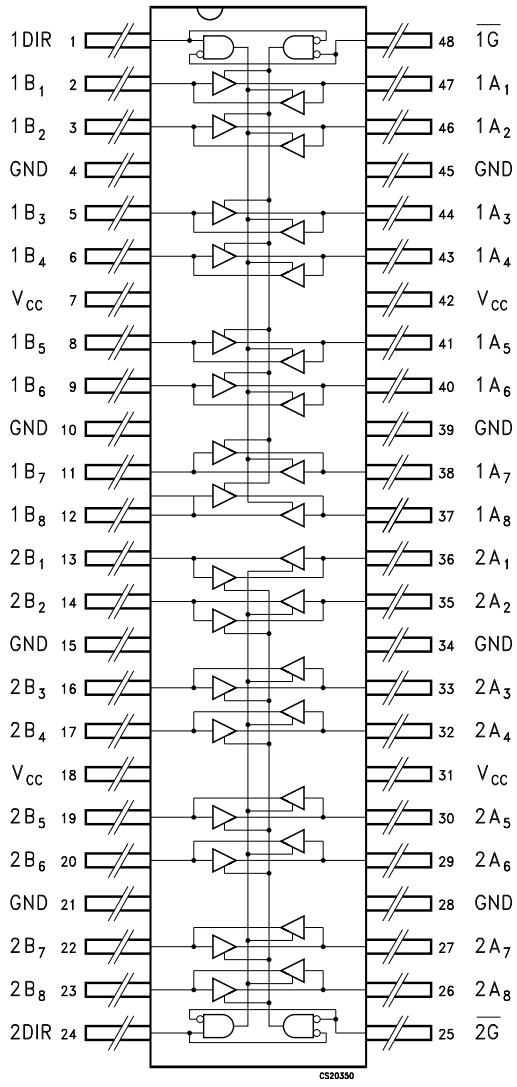
Figure 2. Input and output equivalent circuit



2 Pin settings

2.1 Pin connections

Figure 3. Pin connections (top through view)



2.2 Pin description

Table 1. Pin description

Pin n°	Symbol	Name and function
1	1DIR	Directional control
2, 3, 5, 6, 8, 9, 11, 12	1B1 to 1B8	Data inputs/outputs
13, 14, 16, 17, 19, 20, 22, 23	2B1 to 2B8	Data inputs/outputs
24	2DIR	Directional control
25	$2\overline{G}$	Output enable input
36, 35, 33, 32, 30, 29, 27, 26	2A1 to 2A8	Data inputs/outputs
47, 46, 44, 43, 41, 40, 38, 37	1A1 to 1A8	Data inputs/outputs
48	$1\overline{G}$	Output enable input
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0 V)
7, 18, 31, 42	V_{CC}	Positive supply voltage

2.3 Truth table

Table 2. Truth table

Inputs		Function		Output
$\overline{G}$	DIR	A bus	B bus	Yn
L	L	Output	Input	A = B
L	H	Input	Output	B = A
H	X(1)	Z(2)	Z(2)	Z(2)

1. X = do not care
2. Z = high impedance

3 Maximum ratings

Stressing the device above the rating listed in the “absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	-0.5 to +4.6	V
V_I	DC input voltage		
V_O	DC output voltage (OFF state)		
V_O	DC output voltage (high or low state)(1)	-0.5 to V_{CC} + 0.5	
I_{IK}	DC input diode current	- 50	mA
I_{OK}	DC output diode current(2)		
I_O	DC output current	± 50	
I_{CC} or I_{GND}	DC V_{CC} or ground current per supply pin	± 100	
P_D	Power dissipation	400	mW
T_{stg}	Storage temperature	-65 to +150	°C
T_L	Lead temperature (10 sec)	260	

1. I_O absolute maximum rating must be observed
2. V_O < GND, V_O > V_{CC}

Table 4. Recommended operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	1.8 to 3.6	V
V_I	Input voltage	-0.3 to 3.6	
V_O	Output voltage (OFF state)	0 to 3.6	
V_O	Output voltage (high or low state)	0 to V_{CC}	
I_{OH}, I_{OL}	High or low level output current - A side (V_{CC} = 3.0 to 3.6 V)	± 12	mA
I_{OH}, I_{OL}	High or low level output current - A side (V_{CC} = 2.3 to 2.7 V)	± 8	
I_{OH}, I_{OL}	High or low level output current - B side (V_{CC} = 3.0 to 3.6 V)	± 24	
I_{OH}, I_{OL}	High or low level output current - B side (V_{CC} = 2.3 to 2.7 V)	± 18	
T_{op}	Operating temperature	-55 to 125	°C

4 Electrical characteristics

Table 5. DC specifications at 2.7 V < V_{CC} < 3.6 V unless otherwise specified

Symbol	Parameter	Test condition		Value		Unit
		V_{CC} (V)		-55 to 125 °C		
				Min.	Max.	
V_{IH}	High level input voltage	2.7 to 3.6		2.0		V
V_{IL}	Low level input voltage				0.8	
V_{OH}	High level output voltage (A outputs)	2.7 to 3.6	I_O = -100 µA	V_{CC}-0.2		
		2.7	I_O = -6 mA	2.2		
		3.0	I_O = -8 mA	2.4		
			I_O = -12 mA	2.2		
V_{OH}	High level output voltage (B outputs)	2.7 to 3.6	I_O = -100 µA	V_{CC}-0.2		
		2.7	I_O = -12 mA	2.2		
		3.0	I_O = -18 mA	2.4		
			I_O = -24 mA	2.2		
V_{OL}	Low level output voltage (A outputs)	2.7 to 3.6	I_O = 100 µA		0.2	
		2.7	I_O = 6 mA		0.4	
		3.0	I_O = 8 mA		0.55	
			I_O = 12 mA		0.8	
V_{OL}	Low level output voltage (B outputs)	2.7 to 3.6	I_O = 100 µA		0.2	
		2.7	I_O = 12 mA		0.4	
		3.0	I_O = 18 mA		0.4	
			I_O = 24 mA		0.55	
I_I	Input leakage current	2.7 to 3.6	V_I = 0 to 3.6 V		± 5	µA
$I_{I(HOLD)}$	Input hold current	3.0	V_I = 0.8 V	75		
			V_I = 2 V	-75		
		3.6	V_I = 0 to 3.6 V		± 500	
I_{off}	Power off leakage current	0	V_I or V_O = 0 to 3.6 V		10	
I_{OZ}	High impedance output leakage current	2.7 to 3.6	V_I = V_{IH} or V_{IL} V_O = 0 to 3.6 V		± 10	
I_{CC}	Quiescent supply current	2.7 to 3.6	V_I = V_{CC} or GND		20	
			V_I or V_O = V_{CC} to 3.6 V		± 20	
ΔI_{CC}	I_{CC} incr. per input	2.7 to 3.6	V_{IH} = V_{CC} - 0.6 V		750	

Table 6. DC specifications at 2.3 V < V_{CC} ≤ 2.7 V unless otherwise specified

Symbol	Parameter	Test condition		Value		Unit
		V_{CC} (V)		-55 to 125 °C		
				Min.	Max.	
V_{IH}	High level input voltage	2.3 to 2.7		1.6		V
V_{IL}	Low level input voltage				0.7	
V_{OH}	High level output voltage	2.3 to 2.7	I_O = -100 µA	V_{CC}-0.2		
		2.3	I_O = -4 mA	2.0		
			I_O = -6 mA	1.8		
			I_O = -8 mA	1.7		
V_{OL}	Low level output voltage	2.3 to 2.7	I_O = 100 µA		0.2	
		2.3	I_O = 6 mA		0.4	
			I_O = 8 mA		0.6	
I_I	Input leakage current	2.3 to 2.7	V_I = V_{CC} or GND		± 5	µA
$I_{I(HOLD)}$	Input hold current	2.3	V_I = 0.7 V	45		
			V_I = 1.7 V	-45		
I_{off}	Power off leakage current	0	V_I or V_O = 0 to 3.6 V		10	
I_{OZ}	High impedance output leakage current	2.3 to 2.7	V_I = V_{IH} or V_{IL} V_O = 0 to 3.6 V		± 10	
I_{CC}	Quiescent supply current	2.3 to 2.7	V_I = V_{CC} or GND		20	
			V_I or V_O = V_{CC} to 3.6V		± 20	

Table 7. Dynamic switching characteristics at T_A = 25 °C, input $t_r = t_f$ = 2.0 ns, C_L = 30 pF, R_L = 500 Ω(1)

Symbol	Parameter	Test conditions		Value			Unit
		V_{CC} (V)		T_A = 25 °C			
				Min.	Typ.	Max.	
V_{OLP}	Low level ground bounce noise	3.3	$V_{IH} = V_{CC}$ V_{IL} = 0 V	-	-	1.25	V
V_{OLV}						-0.6	
V_{OHP}	High level V_{CC} bounce noise					1.35	
V_{OHV}						-1.25	

1. This test is for qualification only. Ground and V_{CC} bounce tests are performed on a non-switching (quiescent) output and are used to measure the magnitude of induced noise caused by other simultaneously switching outputs. The test is performed on a low noise bench test fixture. For the device under test, all outputs shall be loaded with 500 Ω load resistance and a minimum of 50 pF of load capacitance. Only chip capacitors and resistors shall be used.

The output load components shall be located as close as possible to the device outputs. It is suggested, that whenever possible, this distance be kept to less than 0.25 inches. Decoupling capacitors shall be placed in parallel from VCC to ground. The values of these decoupling capacitors shall be determined by the device manufacturer. The low and high level ground and VCC bounce noise is measured at the quiet output using a 1 GHz minimum bandwidth oscilloscope with a 50 Ω impedance.The device inputs shall be conditioned such that all outputs are at a low nominal VOH level.

The device inputs shall then be conditioned such that they switch simultaneously and the output under test remains at VOH as all other outputs possible are switched from VOH to VOL. VOHV and VOHP are then measured from the nominal VOH level to the largest negative and positive peaks, respectively. This is then repeated with the same outputs not under test switching from VOL to VOH.The device inputs shall be conditioned such that all outputs are at a low nominal VOL level. The device inputs shall then be conditioned such that they switch simultaneously and the output under test remains at VOL as all other outputs possible are switched from VOL to VOH. VOLP and VOLV are then measured from the nominal VOL level to the largest positive and negative peaks, respectively. This is then repeated with the same outputs not under test switching from VOH to VOL.

Table 8. AC electrical characteristics at C_L = 30 pF, R_L = 500 Ω, Input $t_r = t_f$ = 2.0 ns

Symbol	Parameter	Test conditions	Value		Unit
		V_{CC} (V)	-55 to 125 °C		
			Min.	Max.	
t_{PLH} t_{PHL} (A to B)	Propagation delay time (A to B)	2.3 to 2.7	1.0	4.0	ns
		3.0 to 3.6	0.8	3.6	
t_{PLH} t_{PHL} (B to A)	Propagation delay time (B to A)	2.3 to 2.7	1.0	4.9	
		3.0 to 3.6	0.8	4.0	
t_{PZL} t_{PZH} (A to B)	Output enable time (A to B)	2.3 to 2.7	1.0	5.8	
		3.0 to 3.6	0.8	4.3	
t_{PZL} t_{PZH} (B to A)	Output enable time (B to A)	2.3 to 2.7	1.0	6.8	
		3.0 to 3.6	0.8	4.8	
t_{PLZ} t_{PHZ} (A to B)	Output disable time (A to B)	2.3 to 2.7	1.0	4.8	
		3.0 to 3.6	0.8	5.6	
t_{PLZ} t_{PHZ} (B to A)	Output disable time (B to A)	2.3 to 2.7	1.0	5.7	
		3.0 to 3.6	0.8	7.0	
t_{OSLH} t_{OSHL}	Output to output skew time(1)(2)	2.3 to 2.7		0.5	
		3.0 to 3.6		0.5	

1. Skew is defined as the absolute value of the difference between the actual propagation delay for any two outputs of the same device switching in the same direction, either HIGH or LOW (t_{OSLH} = | t_{PLHm} - t_{PLHn}|, t_{OSHL} = | t_{PHLm} - t_{PHLn}|)
2. Parameter guaranteed by design

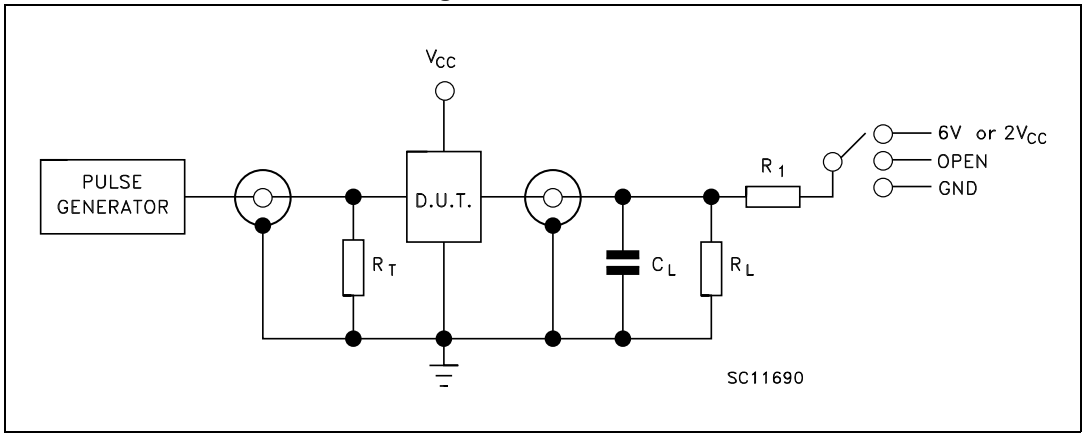
Table 9. Capacitive characteristics

Symbol	Parameter	Test conditions		Value			Unit
		V_{CC} (V)		T_A = 25 °C			
				Min.	Typ.	Max.	
C_{IN}	Input capacitance	2.5 or 3.3	V_{IN} = 0 or V_{CC}	-	4	-	pF
C_{OUT}	Output capacitance		V_{IN} = 0 or V_{CC}		8		
C_{PD}	Power dissipation capacitance(1)		f_{IN} = 10 MHz V_{IN} = 0 or V_{CC}		28		

1. C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to test circuit). Average operating current can be obtained by the following equation. $I_{CC(opr)}$ = C_{PD} x V_{CC} x f_{IN} + I_{CC}/16 (per circuit)

5 Test circuit

Figure 4. Test circuit



1. Legend:
   C_L = 30 pF or equivalent (includes jig and probe capacitance)
   $R_L = R_1$ = 500 Ω or equivalent
   $R_T = Z_{OUT}$ of pulse generator (typically 50 Ω)

Table 10. Test circuit

Test	Switch
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ} (V_{CC} = 3.0 to 3.6 V)	6 V
t_{PZL}, t_{PLZ} (V_{CC} = 2.3 to 2.7 V)	2 V_{CC}
t_{PZH}, t_{PHZ}	GND

6 Waveforms

Table 11. Waveform symbol value

Symbol	V_{CC}	
	3.0 to 3.6 V	2.3 to 2.7 V
V_{IH}	2.7 V	V_{CC}
V_M	1.5 V	$V_{CC}/2$
V_X	V_{OL} +0.3 V	V_{OL} +0.15 V
V_Y	V_{OH} -0.3 V	V_{OH} -0.15 V

Figure 5. Waveforms - propagation delay (f = 1 MHz; 50% duty cycle)

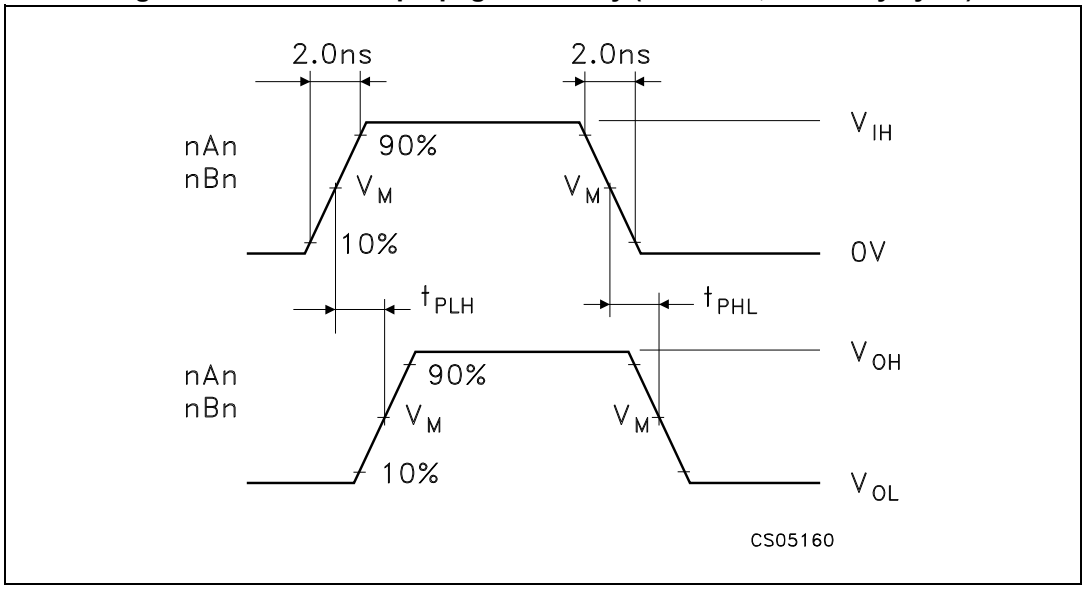
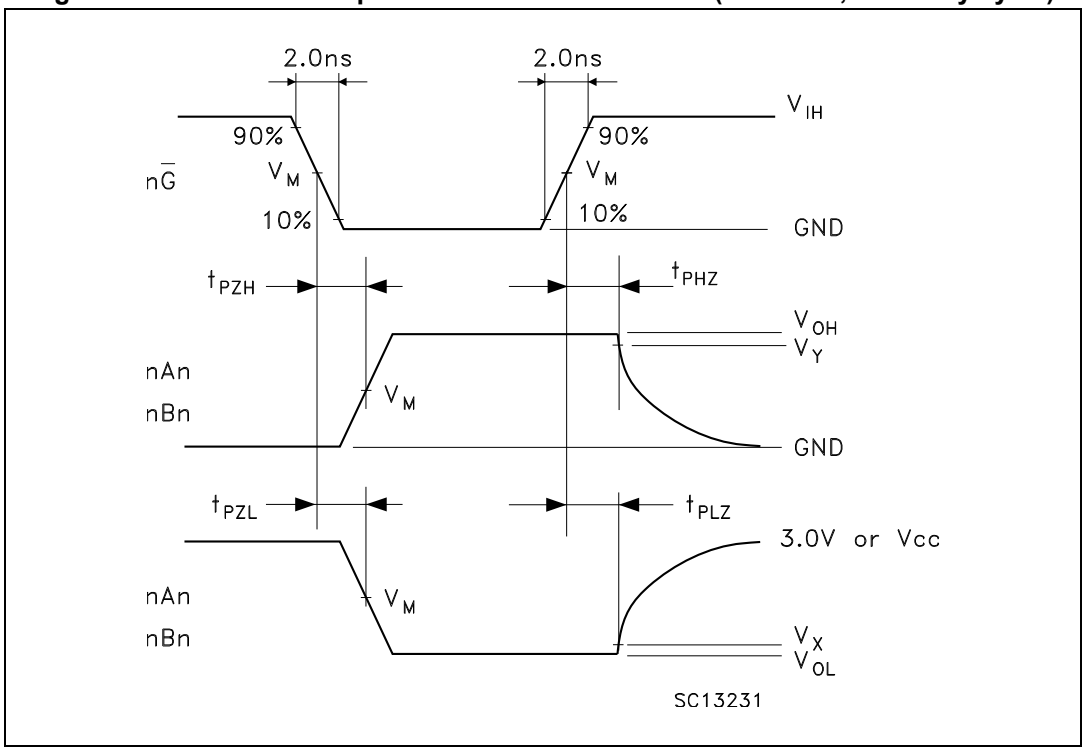


Figure 6. Waveforms - output enable and disable time (f = 1 MHz; 50% duty cycle)

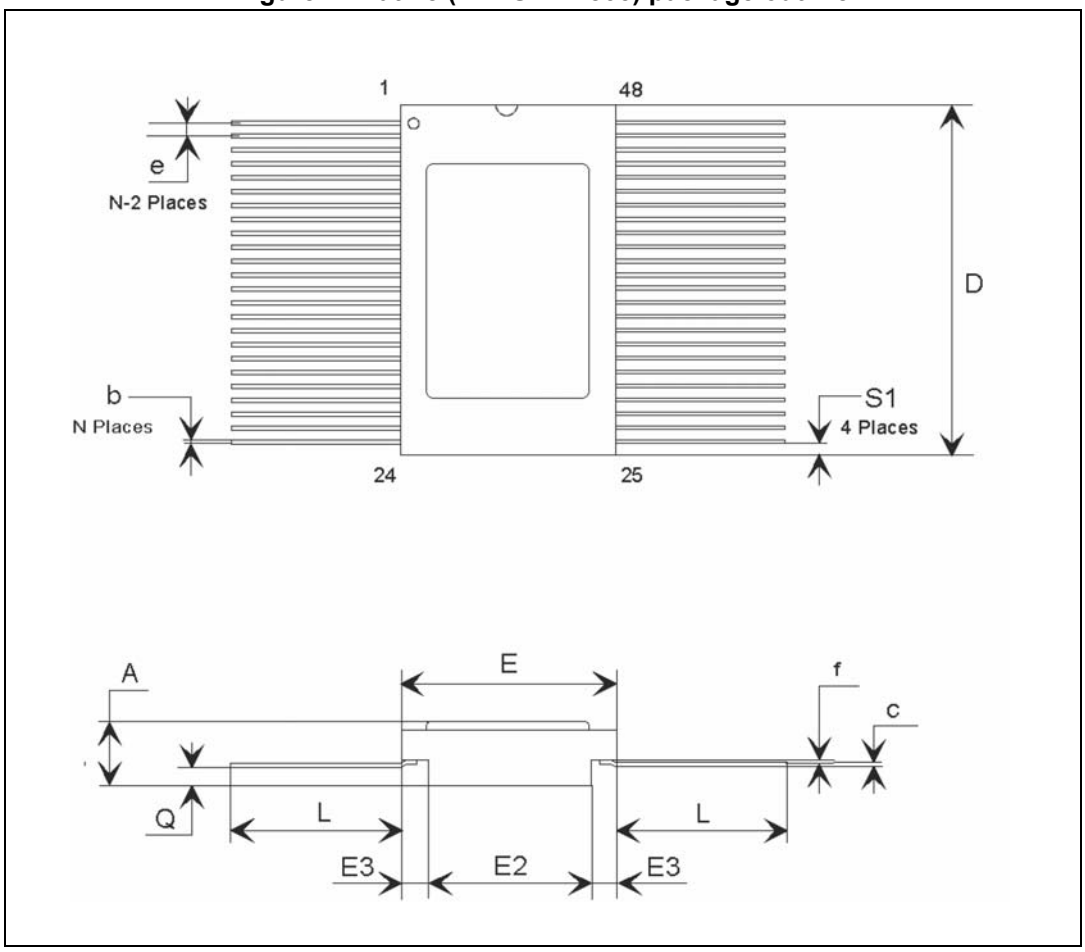


7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

7.1 Flat-48 (MIL-STD-1835) package information

Figure 7. Flat-48 (MIL-STD-1835) package outline



Note: 54VCXH162245 products are supplied in a ceramic body/metal lid hermetic Flat 48-pin space package

Table 12. Flat-48 (MIL-STD-1835) package mechanical data

Dim.	mm			inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.18	2.47	2.72	0.086	0.097	0.107
b	0.20	0.254	0.30	0.008	0.010	0.012
c	0.12	0.15	0.18	0.005	0.006	0.007
D	15.57	15.75	15.92	0.613	0.620	0.627
E	9.52	9.65	9.78	0.375	0.380	0.385
E2	6.22	6.35	6.48	0.245	0.250	0.255
E3	1.52	1.65	1.78	0.060	0.065	0.070
e		0.635			0.025	
f		0.20			0.008	
L	6.85	8.38	9.40	0.270	0.330	0.370
Q	0.66	0.79	0.92	0.026	0.031	0.036
S1	0.25	0.43	0.61	0.010	0.017	0.024

8 Ordering information

Table 13. Ordering information

Order code	SMD[1]	Quality level	Package	Marking[2]	Finishing	Packing
RHRXH162245K1		Engineering model	Flat-48	RHRXH162245K1	Gold	Strip pack
RHFXH162245K03V	5962F0250802VXC	QML-V flight	Flat-48	5962F0250802VXC		
RHFXH162245K05V	5962F0250802VYC	QML-V flight	Flat-48 with grounded lid	5962F0250802VYC		

1. Standard microcircuit drawing.
2. Specific marking only. Complete marking includes the following:

-ST logo

-Date code (date the package was sealed) in YYWWA (year, week, and lot index of week)

-Country of origin (FR=France)

Other information

Date code:

The date code is structured as engineering model: EM xyywwz

where:

x = 3 (EM only), assembly location Rennes (France)

yy = last two digits of the year

ww = week digits

z = lot index of the week

Product documentation

Each product shipment includes a set of associated documentation within the shipment box. This documentation depends on the quality level of the products, as detailed in the table below.

The certificate of conformance is provided on paper whatever the quality level. For QML parts, complete documentation, including the certificate of conformance, is provided on a CDROM.

Table 14. Product documentation

Quality level	Item
Engineering model	Certificate of conformance including: Customer name Customer purchase order number ST sales order number and item ST part number Quantity delivered Date code Reference to ST datasheet Reference to TN1181 on engineering models ST Rennes assembly lot ID
QML-V flight	Certificate of Conformance including: Customer name Customer purchase order number ST sales order number and item ST part number Quantity delivered Date code Serial numbers Group C reference Group D reference Reference to the applicable SMD ST Rennes assembly lot ID
	Quality control inspection (groups A, B, C, D, E)
	Screening electrical data in/out summary
	Precap report
	PIND (particle impact noise detection) test
	SEM (scanning electronic microscope) inspection report
	X-ray plates

9 Revision history

Table 15. Document revision history

Date	Revision	Changes
06-Jul-2004	1	First release
19-Jul-2004	2	Data on range -40 to 85°C removed on Tables 6, 7, 8, 9
17-May-2005	3	Mechanical data has been updated
19-Jun-2006	4	300 Krad bullet updated, new template, mechanical data updated
11-Apr-2007	5	Updated coverpage features
27-Jul-2007	6	Typo in *Table 12 on page 14*
17-Sep-2008	7	Updated cover page
23-Sep-2009	8	Updated *Table 13 on page 16*
29-Jul-2011	9	Added *1. on page 15* and in the “Pin connections” diagram on the coverpage
29-May-2013	10	*Table 1: Pin description*: replaced second pin 38 with pin 37
04-Feb-2020	11	Updated the cover page, *Table 4* and *Section 8: Ordering information*.

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, please refer to *www.st.com/trademarks*. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.