Low-Voltage CMOS 16-Bit Buffer

With 5 V-Tolerant Inputs and Outputs (3-State, Inverting)

The MC74LCX16240 is a high performance, inverting 16–bit buffer operating from a 2.3 V to 3.6 V supply. The device is nibble controlled. Each nibble has separate Output Enable inputs which can be tied together for full 16–bit operation. High impedance TTL compatible inputs significantly reduce current loading to input drivers while TTL compatible outputs offer improved switching noise performance. A $V_{\rm I}$ specification of 5.5 V allows MC74LCX16240 inputs to be safely driven from 5.0 V devices. The LCX16240 is suitable for memory address driving and all TTL level bus oriented transceiver applications.

Current drive capability is 24 mA at the outputs. The Output Enable (\overline{OEn}) inputs, when HIGH, disable the outputs by placing them in a HIGH Z condition.

The MC74LCX16240 contains sixteen inverting buffers with 3–state 5.0 V tolerant outputs. The device is nibble controlled with each nibble functioning identically, but independently. The control pins may be tied together to obtain full 16–bit operation. The 3–state outputs are controlled by an Output Enable (\overline{OEn}) input for each nibble. When \overline{OEn} is LOW, the outputs are on. When \overline{OEn} is HIGH, the outputs are in the high impedance state.

Features

- Designed for 2.3 to 3.6 V V_{CC} Operation
- 5.0 V Tolerant Interface Capability With 5.0 V TTL Logic
- Supports Live Insertion and Withdrawal
- I_{OFF} Specification Guarantees High Impedance When V_{CC} = 0 V
- LVTTL Compatible
- LVCMOS Compatible
- 24 mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current in All Three Logic States (10 μA) Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 500 mA
- ESD Performance: Human Body Model >2000 V; Machine Model >200 V
- These are Pb-Free Devices*



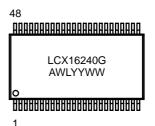
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TSSOP-48 DT SUFFIX CASE 1201

MARKING DIAGRAM



A = Assembly Location

WL = Wafer Lot
 YY = Year
 WW = Work Week
 G = Pb-Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 3 of this data sheet.

^{*}For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

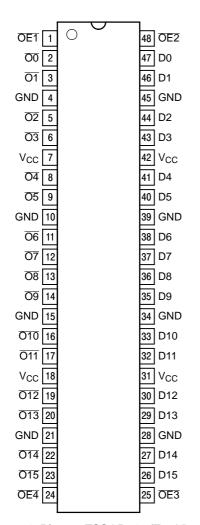


Table 1. PIN NAMES

Pins	Function
OEn	Output Enable Inputs
D0-D15	Inputs
O0-O15	Outputs

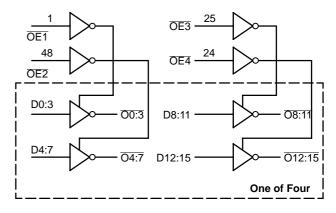


Figure 2. Logic Diagram

Figure 1. Pinout: TSSOP-48 (Top View)

TRUTH TABLE

OE1	D0:3	O0:3	OE2	D4:7	O4:7	OE3	D8:11	O8:11	OE4	D12:15	O12:15
L	L	Н	L	L	Н	L	L	Н	L	L	Н
L	Н	L	L	Н	L	L	Н	L	L	Н	L
Н	Х	Z	Н	Х	Z	Н	Х	Z	Н	Х	Z

H = High Voltage Level
L = Low Voltage Level
Z = High Impedance State
X = High or Low Voltage Level

X = High or Low Voltage Level and Transitions are Acceptable; for I_{CC} reasons, DO NOT FLOAT Inputs

ORDERING INFORMATION

Device Package		Shipping [†]		
MC74LCX16240DTR2 TSSOP-48*		2500 / Tape & Reel		
M74LCX16240DTR2G	TSSOP-48*	2500 / Tape & Reel		

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MAXIMUM RATINGS

Symbol	Parameter	Value	Condition	Unit
V _{CC}	DC Supply Voltage	-0.5 to +7.0		V
VI	DC Input Voltage	$-0.5 \le V_1 \le +7.0$		V
Vo	DC Output Voltage	$-0.5 \le V_{O} \le +7.0$	Output in 3-State	V
		$-0.5 \le V_{O} \le V_{CC} + 0.5$	Output in HIGH or LOW State (Note 1)	V
I _{IK}	DC Input Diode Current	-50	V _I < GND	mA
I _{OK}	DC Output Diode Current	-50	V _O < GND	mA
		+50	V _O > V _{CC}	mA
Io	DC Output Source/Sink Current	±50		mA
I _{CC}	DC Supply Current Per Supply Pin	±100		mA
I _{GND}	DC Ground Current Per Ground Pin	±100		mA
T _{STG}	Storage Temperature Range	-65 to +150		°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Тур	Max	Unit
V _{CC}	Supply Voltage	Operating Data Retention Only	2.0 1.5	2.5, 3.3 2.5, 3.3	3.6 3.6	V
VI	Input Voltage		0		5.5	V
Vo	Output Voltage	(HIGH or LOW State) (3-State)	0 0		V _{CC} 5.5	V
Іон	HIGH Level Output Current	$V_{CC} = 3.0 \text{ V} - 3.6 \text{ V}$ $V_{CC} = 2.7 \text{ V} - 3.0 \text{ V}$ $V_{CC} = 2.3 \text{ V} - 2.7 \text{ V}$			-24 -12 -8	mA
I _{OL}	LOW Level Output Current	$V_{CC} = 3.0 \text{ V} - 3.6 \text{ V}$ $V_{CC} = 2.7 \text{ V} - 3.0 \text{ V}$ $V_{CC} = 2.3 \text{ V} - 2.7 \text{ V}$			+24 +12 +8	mA
T _A	Operating Free–Air Temperature		-40		+85	°C
Δt/ΔV	Input Transition Rise or Fall Rate, V _{IN} from	n 0.8 V to 2.0 V, V _{CC} = 3.0 V	0		10	ns/V

^{*}This package is inherently Pb-Free.

^{1.} I_O absolute maximum rating must be observed.

DC ELECTRICAL CHARACTERISTICS

			T _A = −40°C	to +85°C	
Symbol	Characteristic	Condition	Min	Max	Unit
V_{IH}	HIGH Level Input Voltage (Note 2)	2.3 V ≤ V _{CC} ≤ 2.7 V	1.7		V
		2.7 V ≤ V _{CC} ≤ 3.6 V	2.0		1
V_{IL}	LOW Level Input Voltage (Note 2)	2.3 V ≤ V _{CC} ≤ 2.7 V		0.7	V
		2.7 V ≤ V _{CC} ≤ 3.6 V		0.8	
V _{OH}	HIGH Level Output Voltage	$2.3 \text{ V} \le \text{V}_{CC} \le 3.6 \text{ V}; \text{ I}_{OL} = 100 \mu\text{A}$	V _{CC} – 0.2		V
		$V_{CC} = 2.3 \text{ V; } I_{OH} = -8 \text{ mA}$	1.8		
		$V_{CC} = 2.7 \text{ V; } I_{OH} = -12 \text{ mA}$	2.2		
		$V_{CC} = 3.0 \text{ V}; I_{OH} = -18 \text{ mA}$	2.4		
		$V_{CC} = 3.0 \text{ V}; I_{OH} = -24 \text{ mA}$	2.2		
V _{OL}	LOW Level Output Voltage	$2.3 \text{ V} \le \text{V}_{CC} \le 3.6 \text{ V}; \text{ I}_{OL} = 100 \mu\text{A}$		0.2	V
		$V_{CC} = 2.3 \text{ V; } I_{OL} = 8 \text{ mA}$		0.6	
		V _{CC} = 2.7 V; I _{OL} = 12 mA		0.4	
		V _{CC} = 3.0 V; I _{OL} = 16 mA		0.4	
		V _{CC} = 3.0 V; I _{OL} = 24 mA		0.55	1
II	Input Leakage Current	$2.3 \text{ V} \le \text{V}_{CC} \le 3.6 \text{ V}; 0 \text{ V} \le \text{V}_{I} \le 5.5 \text{ V}$		±5.0	μΑ
I _{OZ}	3-State Output Current	$2.3 \le V_{CC} \le 3.6 \text{ V}; \text{ 0V} \le V_{O} \le 5.5 \text{ V};$ $V_{I} = V_{IH} \text{ or V}_{IL}$		±5.0	μΑ
I _{OFF}	Power-Off Leakage Current	$V_{CC} = 0 \text{ V}; V_{I} \text{ or } V_{O} = 5.5 \text{ V}$		10	μΑ
I _{CC}	Quiescent Supply Current	$2.3 \le V_{CC} \le 3.6 \text{ V}; V_I = \text{GND or } V_{CC}$		20	μΑ
		$2.3 \le V_{CC} \le 3.6 \text{ V}; 3.6 \le V_{I} \text{ or } V_{O} \le 5.5 \text{ V}$		±20	μΑ
ΔI_{CC}	Increase in I _{CC} per Input	$2.3 \le V_{CC} \le 3.6 \text{ V}; V_{IH} = V_{CC} - 0.6 \text{ V}$		500	μΑ

^{2.} These values of V_I are used to test DC electrical characteristics only.

AC CHARACTERISTICS $t_R = t_F = 2.5 ns; R_L = 500 \ \Omega$

			$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$						
				3 V ± 0.3 V 50 pF		2.7 V 50 pF	V _{CC} = 2.5 C _L =	V ± 0.2 V 30 pF	
Symbol	Parameter	Waveform	Min	Max	Min	Max	Min	Max	Unit
t _{PLH} t _{PHL}	Propagation Delay Input to Output	1	1.5 1.5	4.5 4.5	1.5 1.5	5.3 5.3	1.5 1.5	5.4 5.4	ns
t _{PZH} t _{PZL}	Output Enable Time to High and Low Level	2	1.5 1.5	5.4 5.4	1.5 1.5	6.0 6.0	1.5 1.5	7.0 7.0	ns
t _{PHZ} t _{PLZ}	Output Disable Time From High and Low Level	2	1.5 1.5	5.3 5.3	1.5 1.5	5.4 5.4	1.5 1.5	6.4 6.4	ns
t _{OSHL} t _{OSLH}	Output-to-Output Skew (Note 3)			1.0 1.0					ns

Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device.
 The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}); parameter guaranteed by design.

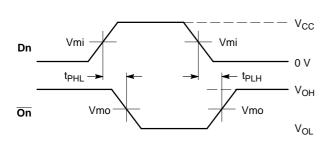
DYNAMIC SWITCHING CHARACTERISTICS

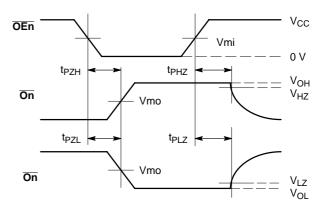
			T _A = +25°C			
Symbol	Characteristic	Condition	Min	Тур	Max	Unit
V _{OLP}	Dynamic LOW Peak Voltage (Note 4)	$V_{CC} = 3.3 \text{ V}, C_L = 50 \text{ pF}, V_{IH} = 3.3 \text{ V}, V_{IL} = 0 \text{ V}$ $V_{CC} = 2.5 \text{ V}, C_L = 30 \text{ pF}, V_{IH} = 2.5 \text{ V}, V_{IL} = 0 \text{ V}$		0.8 0.6		V V
V _{OLV}	Dynamic LOW Valley Voltage (Note 4)	$V_{CC} = 3.3 \text{ V}, C_L = 50 \text{ pF}, V_{IH} = 3.3 \text{ V}, V_{IL} = 0 \text{ V}$ $V_{CC} = 2.5 \text{ V}, C_L = 30 \text{ pF}, V_{IH} = 2.5 \text{ V}, V_{IL} = 0 \text{ V}$		-0.8 -0.6		V V

^{4.} Number of outputs defined as "n". Measured with "n-1" outputs switching from HIGH-to-LOW or LOW-to-HIGH. The remaining output is measured in the LOW state.

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Unit
C _{IN}	Input Capacitance	$V_{CC} = 3.3 \text{ V}, V_{I} = 0 \text{ V or } V_{CC}$	7	pF
C _{OUT}	Output Capacitance	$V_{CC} = 3.3 \text{ V}, V_{I} = 0 \text{ V or } V_{CC}$	8	pF
C _{PD}	Power Dissipation Capacitance	10 MHz, V_{CC} = 3.3 V, V_I = 0 V or V_{CC}	20	pF





WAVEFORM 1 - PROPAGATION DELAYS

 t_R = t_F = 2.5 ns, 10% to 90%; f = 1 MHz; t_W = 500 ns

WAVEFORM 2 - OUTPUT ENABLE AND DISABLE TIMES

 $t_R = t_F = 2.5 \text{ ns}, 10\% \text{ to } 90\%; f = 1 \text{ MHz}; t_W = 500 \text{ ns}$

Figure 3. AC Waveforms

Table 2. AC WAVEFORMS

	V _{cc}					
Symbol	3.3 V ± 0.3 V	2.7 V	2.5 V ± 0.2 V			
Vmi	1.5 V	1.5 V	V _{CC} / 2			
Vmo	1.5 V	1.5 V	V _{CC} / 2			
V _{HZ}	V _{OL} + 0.3 V	V _{OL} + 0.3 V	V _{OL} + 0.15 V			
V_{LZ}	V _{OH} – 0.3 V	V _{OH} – 0.3 V	V _{OH} – 015 V			

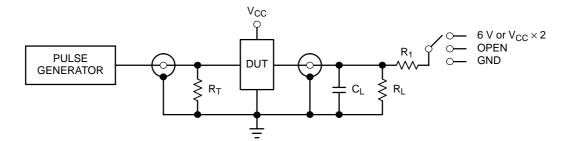


Figure 4. Test Circuit

Table 3. TEST CIRCUIT

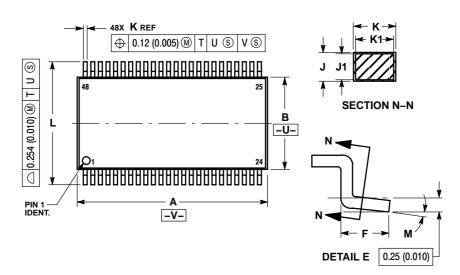
TEST	SWITCH
t _{PLH} , t _{PHL}	Open
t _{PZL} , t _{PLZ}	6 V at V_{CC} = 3.3 \pm 0.3 V 6 V at V_{CC} = 2.5 \pm 0.2 V
Open Collector/Drain t _{PLH} and t _{PHL}	6 V
t _{PZH} , t _{PHZ}	GND

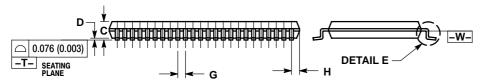
 C_L = 50 pF at V_{CC} = 3.3 ± 0.3 V or equivalent (includes jig and probe capacitance) C_L = 30 pF at V_{CC} = 2.5 ± 0.2 V or equivalent (includes jig and probe capacitance) R_L = R_1 = 500 Ω or equivalent

 $R_T^- = Z_{OUT}$ of pulse generator (typically 50 Ω)

PACKAGE DIMENSIONS

TSSOP-48 **DT SUFFIX** CASE 1201-01 **ISSUE A**





- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.

- 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSIONS A AND B DO NOT INCLUDE
 MOLD FLASH, PROTRUSIONS OR GATE
 BURRS. MOLD FLASH OR GATE BURRS
 SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
 4. DIMENSION K DOES NOT INCLUDE DAMBAR
 PROTRUSION. ALLOWABLE DAMBAR
 PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN
 EXCESS OF THE K DIMENSION AT MAXIMUM
 MATERIAL CONDITION.
 5. TERMINAL NUMBERS ARE SHOWN FOR
 REFERENCE ONLY.
 6. DIMENSIONS A AND B ARE TO BE
 DETERMINED AT DATUM PLANE W-

	MILLIN	IETERS	INCHES		
DIM	MIN	MAX	MIN	MAX	
Α	12.40	12.60	0.488	0.496	
В	6.00	6.20	0.236	0.244	
С		1.10		0.043	
D	0.05	0.15	0.002	0.006	
F	0.50	0.75	0.020	0.030	
G	0.50	BSC	0.0197 BSC		
Н	0.37		0.015		
J	0.09	0.20	0.004	0.008	
J1	0.09	0.16	0.004	0.006	
K	0.17	0.27	0.007	0.011	
K1	0.17	0.23	0.007	0.009	
L	7.95	8.25	0.313	0.325	
M	0 °	8 °	0 °	8 °	

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