DDR3 SDRAM SODIMM

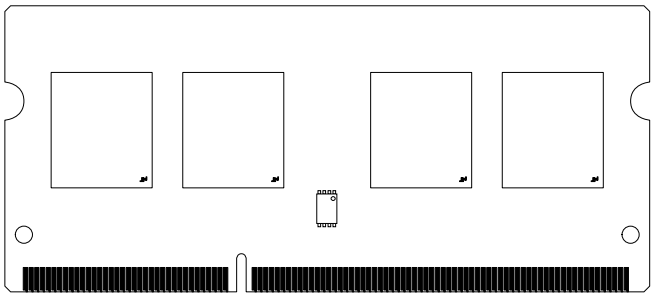
MT8JTF12864HZ – 1GB
MT8JTF25664HZ – 2GB
MT8JTF51264HZ – 4GB

Features

- DDR3 functionality and operations supported as defined in the component data sheet
- 204-pin, small-outline dual in-line memory module (SODIMM)
- Fast data transfer rates: PC3-12800, PC3-10600, PC3-8500, or PC3-6400
- 1GB (128 Meg x 64), 2GB (256 Meg x 64), 4GB (512 Meg x 64)
- V_{DD} = 1.5V ±0.075V
- V_{DDSPD} = 3.0–3.6V
- Nominal and dynamic on-die termination (ODT) for data, strobe, and mask signals
- Single-rank
- Serial presence-detect (SPD) EEPROM
- 8 internal device banks
- Fixed burst chop (BC) of 4 and burst length (BL) of 8 via the mode register set (MRS)
- Selectable BC4 or BL8 on-the-fly (OTF)
- Gold edge contacts
- Halogen-free
- Fly-by topology
- Terminated control, command, and address bus

Figure 1: 204-Pin SODIMM (MO-268 R/C B)

Module height: 30mm (1.181in)



Options	Marking
• Operating temperature	
– Commercial (0°C ≤ T_A ≤ +70°C)	None
• Package	
– 204-pin DIMM (halogen-free)	Z
• Frequency/CAS latency	
– 1.25ns @ CL = 11 (DDR3-1600)	-1G6
– 1.5ns @ CL = 9 (DDR3-1333)	-1G4
– 1.87ns @ CL = 7 (DDR3-1066)	-1G1

Table 1: Key Timing Parameters

Speed Grade	Industry Nomenclature	Data Rate (MT/s)							^tRCD (ns)	^tRP (ns)	^tRC (ns)
		CL = 11	CL = 10	CL = 9	CL = 8	CL = 7	CL = 6	CL = 5			
-1G6	PC3-12800	1600	1333	1333	1066	1066	800	667	13.125	13.125	48.125
-1G4	PC3-10600	–	1333	1333	1066	1066	800	667	13.125	13.125	49.125
-1G1	PC3-8500	–	–	–	1066	1066	800	667	13.125	13.125	50.625
-1G0	PC3-8500	–	–	–	1066	–	800	667	15	15	52.5
-80B	PC3-6400	–	–	–	–	–	800	667	15	15	52.5

Table 2: Addressing

Parameter	1GB	2GB	4GB
Refresh count	8K	8K	8K
Row address	16K A[13:0]	32K A[14:0]	64K A[15:0]
Device bank address	8 BA[2:0]	8 BA[2:0]	8 BA[2:0]
Device configuration	1Gb (128 Meg x 8)	2Gb (256 Meg x 8)	4Gb (512 Meg x 8)
Column address	1K A[9:0]	1K A[9:0]	1K A[9:0]
Module rank address	1 S0#	1 S0#	1 S0#

Table 3: Part Numbers and Timing Parameters – 1GB Modules

Base device: MT41J128M8,[1] 1Gb DDR3 SDRAM

Part Number[2]	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Clock Cycles (CL-^{t}RCD-^{t}RP)
MT8JTF12864HZ-1G6__	1GB	128 Meg x 64	12.8 GB/s	1.25ns/1600 MT/s	11-11-11
MT8JTF12864HZ-1G4__	1GB	128 Meg x 64	10.6 GB/s	1.5ns/1333 MT/s	9-9-9
MT8JTF12864HZ-1G1__	1GB	128 Meg x 64	8.5 GB/s	1.87ns/1066 MT/s	7-7-7

Table 4: Part Numbers and Timing Parameters – 2GB Modules

Base device: MT41J256M8,[1] 2Gb DDR3 SDRAM

Part Number[2]	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Clock Cycles (CL-^{t}RCD-^{t}RP)
MT8JTF25664HZ-1G6__	2GB	256 Meg x 64	12.8 GB/s	1.25ns/1600 MT/s	11-11-11
MT8JTF25664HZ-1G4__	2GB	256 Meg x 64	10.6 GB/s	1.5ns/1333 MT/s	9-9-9
MT8JTF25664HZ-1G1__	2GB	256 Meg x 64	8.5 GB/s	1.87ns/1066 MT/s	7-7-7

Table 5: Part Numbers and Timing Parameters – 4GB Modules

Base device: MT41J512M8,[1] 4Gb DDR3 SDRAM

Part Number[2]	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Clock Cycles (CL-^{t}RCD-^{t}RP)
MT8JTF51264HZ-1G6__	4GB	512 Meg x 64	12.8 GB/s	1.25ns/1600 MT/s	11-11-11
MT8JTF51264HZ-1G4__	4GB	512 Meg x 64	10.6 GB/s	1.5ns/1333 MT/s	9-9-9
MT8JTF51264HZ-1G1__	4GB	512 Meg x 64	8.5 GB/s	1.87ns/1066 MT/s	7-7-7

Notes:
1. The data sheet for the base device can be found on Micron's Web site.
2. All part numbers end with a two-place code (not shown) that designates component and PCB revisions. Consult factory for current revision codes. Example: MT8JTF51264HZ-1G6E1.

Pin Assignments

Table 6: Pin Assignments

204-Pin DDR3 SODIMM Front								204-Pin DDR3 SODIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	V_{REFDQ}	53	DQ19	105	V_{DD}	157	DQ42	2	V_{SS}	54	V_{SS}	106	V_{DD}	158	DQ46
3	V_{SS}	55	V_{SS}	107	A10	159	DQ43	4	DQ4	56	DQ28	108	BA1	160	DQ47
5	DQ0	57	DQ24	109	BA0	161	V_{SS}	6	DQ5	58	DQ29	110	RAS#	162	V_{SS}
7	DQ1	59	DQ25	111	V_{DD}	163	DQ48	8	V_{SS}	60	V_{SS}	112	V_{DD}	164	DQ52
9	V_{SS}	61	V_{SS}	113	WE#	165	DQ49	10	DQS0#	62	DQ3#	114	S0#	166	DQ53
11	DM0	63	DM3	115	CAS#	167	V_{SS}	12	DQS0	64	DQ3	116	ODT0	168	V_{SS}
13	V_{SS}	65	V_{SS}	117	V_{DD}	169	DQS6#	14	V_{SS}	66	V_{SS}	118	V_{DD}	170	DM6
15	DQ2	67	DQ26	119	A13	171	DQS6	16	DQ6	68	DQ30	120	NC	172	V_{SS}
17	DQ3	69	DQ27	121	NC	173	V_{SS}	18	DQ7	70	DQ31	122	NC	174	DQ54
19	V_{SS}	71	V_{SS}	123	V_{DD}	175	DQ50	20	V_{SS}	72	V_{SS}	124	V_{DD}	176	DQ55
21	DQ8	73	CKE0	125	NC	177	DQ51	22	DQ12	74	NC	126	V_{REFCA}	178	V_{SS}
23	DQ9	75	V_{DD}	127	V_{SS}	179	V_{SS}	24	DQ13	76	V_{DD}	128	V_{SS}	180	DQ60
25	V_{SS}	77	NC	129	DQ32	181	DQ56	26	V_{SS}	78	A15	130	DQ36	182	DQ61
27	DQS1#	79	BA2	131	DQ33	183	DQ57	28	DM1	80	A14	132	DQ37	184	V_{SS}
29	DQS1	81	V_{DD}	133	V_{SS}	185	V_{SS}	30	RESET#	82	V_{DD}	134	V_{SS}	186	DQS7#
31	V_{SS}	83	A12	135	DQS4#	187	DM7	32	V_{SS}	84	A11	136	DM4	188	DQS7
33	DQ10	85	A9	137	DQS4	189	V_{SS}	34	DQ14	86	A7	138	V_{SS}	190	V_{SS}
35	DQ11	87	V_{DD}	139	V_{SS}	191	DQ58	36	DQ15	88	V_{DD}	140	DQ38	192	DQ62
37	V_{SS}	89	A8	141	DQ34	193	DQ59	38	V_{SS}	90	A6	142	DQ39	194	DQ63
39	DQ16	91	A5	143	DQ35	195	V_{SS}	40	DQ20	92	A4	144	V_{SS}	196	V_{SS}
41	DQ17	93	V_{DD}	145	V_{SS}	197	SA0	42	DQ21	94	V_{DD}	146	DQ44	198	NF
43	V_{SS}	95	A3	147	DQ40	199	V_{DDSPD}	44	V_{SS}	96	A2	148	DQ45	200	SDA
45	DQS2#	97	A1	149	DQ41	201	SA1	46	DM2	98	A0	150	V_{SS}	202	SCL
47	DQS2	99	V_{DD}	151	V_{SS}	203	V_{TT}	48	V_{SS}	100	V_{DD}	152	DQS5#	204	V_{TT}
49	V_{SS}	101	CK0	153	DM5	–	–	50	DQ22	102	CK1	154	DQS5	–	–
51	DQ18	103	CK0#	155	V_{SS}	–	–	52	DQ23	104	CK1#	156	V_{SS}	–	–

Pin Descriptions

The pin description table below is a comprehensive list of all possible pins for all DDR3 modules. All pins listed may not be supported on this module. See Pin Assignments for information specific to this module.

Table 7: Pin Descriptions

Symbol	Type	Description
Ax	Input	**Address inputs:** Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BAx) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command. See the Pin Assignments Table for density-specific addressing information.
BAx	Input	**Bank address inputs:** Define the device bank to which an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA define which mode register (MR0, MR1, MR2, or MR3) is loaded during the LOAD MODE command.
CKx, CKx#	Input	**Clock:** Differential clock inputs. All control, command, and address input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#.
CKEx	Input	**Clock enable:** Enables (registered HIGH) and disables (registered LOW) internal circuitry and clocks on the DRAM.
DMx	Input	**Data mask (x8 devices only):** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH, along with that input data, during a write access. Although DM pins are input-only, DM loading is designed to match that of the DQ and DQS pins.
ODTx	Input	**On-die termination:** Enables (registered HIGH) and disables (registered LOW) termination resistance internal to the DDR3 SDRAM. When enabled in normal operation, ODT is only applied to the following pins: DQ, DQS, DQS#, DM, and CB. The ODT input will be ignored if disabled via the LOAD MODE command.
Par_In	Input	**Parity input:** Parity bit for Ax, RAS#, CAS#, and WE#.
RAS#, CAS#, WE#	Input	**Command inputs:** RAS#, CAS#, and WE# (along with S#) define the command being entered.
RESET#	Input (LVCMOS)	**Reset:** RESET# is an active LOW asychronous input that is connected to each DRAM and the registering clock driver. After RESET# goes HIGH, the DRAM must be reinitialized as though a normal power-up was executed.
Sx#	Input	**Chip select:** Enables (registered LOW) and disables (registered HIGH) the command decoder.
SAx	Input	**Serial address inputs:** Used to configure the temperature sensor/SPD EEPROM address range on the I^2C bus.
SCL	Input	**Serial clock for temperature sensor/SPD EEPROM:** Used to synchronize communication to and from the temperature sensor/SPD EEPROM on the I^2C bus.
CBx	I/O	**Check bits:** Used for system error detection and correction.
DQx	I/O	**Data input/output:** Bidirectional data bus.
DQSx, DQSx#	I/O	**Data strobe:** Differential data strobes. Output with read data; edge-aligned with read data; input with write data; center-aligned with write data.

Table 7: Pin Descriptions (Continued)

Symbol	Type	Description
SDA	I/O	**Serial data:** Used to transfer addresses and data into and out of the temperature sensor/SPD EEPROM on the I^2C bus.
TDQSx, TDQSx#	Output	**Redundant data strobe (x8 devices only):** TDQS is enabled/disabled via the LOAD MODE command to the extended mode register (EMR). When TDQS is enabled, DM is disabled and TDQS and TDQS# provide termination resistance; otherwise, TDQS# are no function.
Err_Out#	Output (open drain)	**Parity error output:** Parity error found on the command and address bus.
EVENT#	Output (open drain)	**Temperature event:**The EVENT# pin is asserted by the temperature sensor when critical temperature thresholds have been exceeded.
V_{DD}	Supply	**Power supply:** 1.5V ±0.075V. The component V_{DD} and V_{DDQ} are connected to the module V_{DD}.
V_{DDSPD}	Supply	**Temperature sensor/SPD EEPROM power supply:** 3.0–3.6V.
V_{REFCA}	Supply	**Reference voltage:** Control, command, and address $V_{DD}/2$.
V_{REFDQ}	Supply	**Reference voltage:** DQ, DM $V_{DD}/2$.
V_{SS}	Supply	Ground.
V_{TT}	Supply	**Termination voltage:** Used for control, command, and address $V_{DD}/2$.
NC	–	**No connect:** These pins are not connected on the module.
NF	–	**No function:** These pins are connected within the module, but provide no functionality.

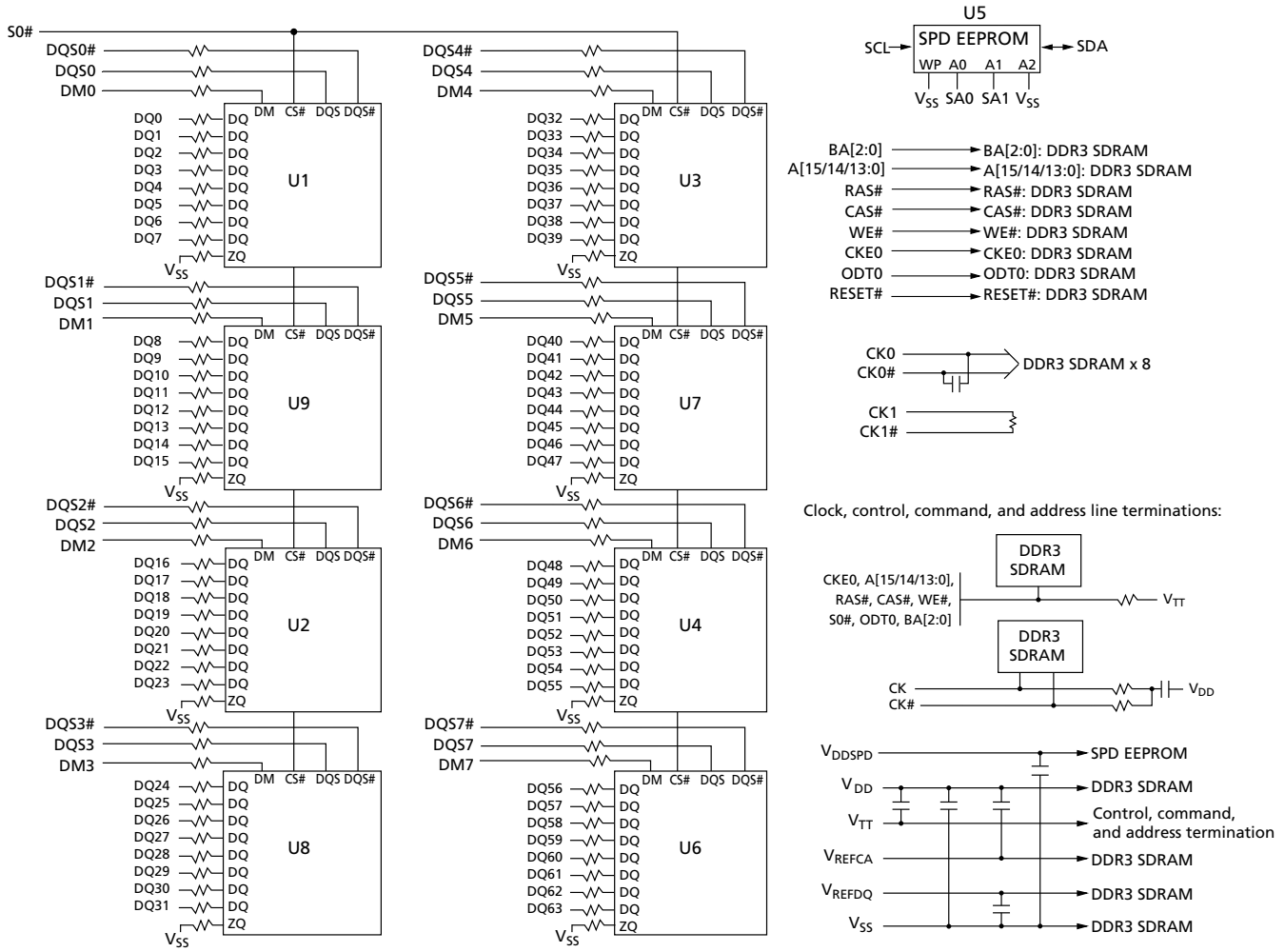
DQ Map

Table 8: Component-to-Module DQ Map

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U1	0	2	15	U2	0	22	50
	1	1	7		1	17	41
	2	6	16		2	18	51
	3	5	6		3	21	42
	4	7	18		4	23	52
	5	0	5		5	16	39
	6	3	17		6	19	53
	7	4	4		7	20	40
U3	0	34	141	U4	0	50	175
	1	36	130		1	53	166
	2	38	140		2	54	174
	3	33	131		3	49	165
	4	35	143		4	55	176
	5	32	129		5	48	163
	6	39	142		6	51	177
	7	37	132		7	52	164
U6	0	61	182	U7	0	45	148
	1	62	192		1	42	157
	2	57	183		2	44	146
	3	58	191		3	46	158
	4	60	180		4	40	147
	5	59	193		5	47	160
	6	56	181		6	41	149
	7	63	194		7	43	159
U8	0	29	58	U9	0	9	23
	1	26	67		1	10	33
	2	25	59		2	13	24
	3	31	70		3	11	35
	4	24	57		4	12	22
	5	30	68		5	15	36
	6	28	56		6	8	21
	7	27	69		7	14	34

Functional Block Diagram

Figure 2: Functional Block Diagram



Note: 1. The ZQ ball on each DDR3 component is connected to an external 240Ω ±1% resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.

General Description

DDR3 SDRAM modules are high-speed, CMOS dynamic random access memory modules that use internally configured 8-bank DDR3 SDRAM devices. DDR3 SDRAM modules use DDR architecture to achieve high-speed operation. DDR3 architecture is essentially an 8*n*-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR3 SDRAM module effectively consists of a single 8*n*-bit-wide, one-clock-cycle data transfer at the internal DRAM core and eight corresponding *n*-bit-wide, one-half-clock-cycle data transfers at the I/O pins.

DDR3 modules use two sets of differential signals: DQS, DQS# to capture data and CK and CK# to capture commands, addresses, and control signals. Differential clocks and data strobes ensure exceptional noise immunity for these signals and provide precise crossing points to capture input signals.

Fly-By Topology

DDR3 modules use faster clock speeds than earlier DDR technologies, making signal quality more important than ever. For improved signal quality, the clock, control, command, and address buses have been routed in a fly-by topology, where each clock, control, command, and address pin on each DRAM is connected to a single trace and terminated (rather than a tree structure, where the termination is off the module near the connector). Inherent to fly-by topology, the timing skew between the clock and DQS signals can be easily accounted for by using the write-leveling feature of DDR3.

Serial Presence-Detect EEPROM Operation

DDR3 SDRAM modules incorporate serial presence-detect. The SPD data is stored in a 256-byte EEPROM. The first 128 bytes are programmed by Micron to comply with JEDEC standard JC-45, "Appendix X: Serial Presence Detect (SPD) for DDR3 SDRAM Modules." These bytes identify module-specific timing parameters, configuration information, and physical attributes. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device occur via a standard I^2C bus using the DIMM's SCL (clock) SDA (data), and SA (address) pins. Write protect (WP) is connected to V_{SS}, permanently disabling hardware write protection. For further information refer to Micron technical note TN-04-42, "Memory Module Serial Presence-Detect."

Electrical Specifications

Stresses greater than those listed may cause permanent damage to the module. This is a stress rating only, and functional operation of the module at these or any other conditions outside those indicated in each device's data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

Table 9: Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units
V_{DD}	V_{DD} supply voltage relative to V_{SS}	–0.4	1.975	V
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}	–0.4	1.975	V

Table 10: Operating Conditions

Symbol	Parameter		Min	Nom	Max	Units	Notes
V_{DD}	V_{DD} supply voltage		1.425	1.5	1.575	V	
I_{VTT}	Termination reference current from V_{TT}		–600	–	600	mA	
V_{TT}	Termination reference voltage (DC) – command/address bus		0.49 × V_{DD} - 20mV	0.5 × V_{DD}	0.51 × V_{DD} + 20mV	V	1
I_I	Input leakage current; Any input 0V ≤ V_{IN} ≤ V_{DD}; V_{REF} input 0V ≤ V_{IN} ≤ 0.95V (All other pins not under test = 0V)	Address inputs, RAS#, CAS#, WE#, S#, CKE, ODT, BA, CK, CK#	–16	0	16	µA	
		DM	–2	0	2		
I_{OZ}	Output leakage current; 0V ≤ V_{OUT} ≤ V_{DD}; DQ and ODT are disabled; ODT is HIGH	DQ, DQS, DQS#	–5	0	5	µA	
I_{VREF}	V_{REF} supply leakage current; V_{REFDQ} = V_{DD}/2 or V_{REFCA} = V_{DD}/2 (All other pins not under test = 0V)		–8	0	8	µA	
T_A	Module ambient operating temperature	Commercial	0	–	70	°C	2, 3
		Industrial	–40	–	85	°C	
T_C	DDR3 SDRAM component case operating temperature	Commercial	0	–	95	°C	2, 3, 4
		Industrial	–40	–	95	°C	

Notes:
1. V_{TT} termination voltage in excess of the stated limit will adversely affect the command and address signals' voltage margin and will reduce timing margins.
2. T_A and T_C are simultaneous requirements.
3. For further information, refer to technical note TN-00-08: "Thermal Applications," available on Micron's Web site.
4. The refresh rate is required to double when 85°C < T_C ≤ 95°C.

DRAM Operating Conditions

Recommended AC operating conditions are given in the DDR3 component data sheets. Component specifications are available on Micron's web site. Module speed grades correlate with component speed grades, as shown below.

Table 11: Module and Component Speed Grades

DDR3 components may exceed the listed module speed grades; module may not be available in all listed speed grades

Module Speed Grade	Component Speed Grade
-2G1	-093
-1G9	-107
-1G6	-125
-1G4	-15E
-1G1	-187E
-1G0	-187
-80C	-25E
-80B	-25

Design Considerations

Simulations

Micron memory modules are designed to optimize signal integrity through carefully designed terminations, controlled board impedances, routing topologies, trace length matching, and decoupling. However, good signal integrity starts at the system level. Micron encourages designers to simulate the signal characteristics of the system's memory bus to ensure adequate signal integrity of the entire memory system.

Power

Operating voltages are specified at the DRAM, not at the edge connector of the module. Designers must account for any system voltage drops at anticipated power levels to ensure the required supply voltage is maintained.

I_{DD} Specifications

Table 12: DDR3 I_{DD} Specifications and Conditions – 1GB (Die Revision G)

Values are for the MT41J128M8 DDR3 SDRAM only and are computed from values specified in the 1Gb (128 Meg x 8) component data sheet

Parameter	Symbol	1600	1333	1066	Units
Operating current 0: One bank ACTIVATE-to-PRECHARGE	I_{DD0}	560	520	480	mA
Operating current 1: One bank ACTIVATE-to-READ-to-PRECHARGE	I_{DD1}	720	680	640	mA
Precharge power-down current: Slow exit	I_{DD2P0}	96	96	96	mA
Precharge power-down current: Fast exit	I_{DD2P1}	240	240	200	mA
Precharge quiet standby current	I_{DD2Q}	320	280	280	mA
Precharge standby current	I_{DD2N}	360	320	280	mA
Precharge standby ODT current	I_{DD2NT}	440	400	360	mA
Active power-down current	I_{DD3P}	380	240	240	mA
Active standby current	I_{DD3N}	360	320	320	mA
Burst read operating current	I_{DD4R}	1120	1000	880	mA
Burst write operating current	I_{DD4W}	1160	1000	880	mA
Refresh current	I_{DD5}	1360	1320	1280	mA
Self refresh temperature current: MAX T_C = 85°C	I_{DD6}	64	64	64	mA
Self refresh temperature current (SRT-enabled): MAX T_C = 95°C	I_{DD6ET}	80	80	80	mA
All banks interleaved read current	I_{DD7}	1960	1880	1560	mA
Reset current	I_{DD8}	112	112	112	mA

Table 13: DDR3 I_{DD} Specifications and Conditions – 2GB (Die Revision M)

Values are for the MT41J256M8 DDR3 SDRAM only and are computed from values specified in the 2Gb (256 Meg x 8) component data sheet

Parameter	Symbol	1600	1333	1066	Units
Operating current 0: One bank ACTIVATE-to-PRECHARGE	I_{DD0}	560	520	480	mA
Operating current 1: One bank ACTIVATE-to-READ-to-PRECHARGE	I_{DD1}	640	600	560	mA
Precharge power-down current: Slow exit	I_{DD2P0}	96	96	96	mA
Precharge power-down current: Fast exit	I_{DD2P1}	296	256	216	mA
Precharge quiet standby current	I_{DD2Q}	230	280	240	mA
Precharge standby current	I_{DD2N}	344	304	264	mA
Precharge standby ODT current	I_{DD2NT}	360	320	280	mA
Active power-down current	I_{DD3P}	400	360	320	mA
Active standby current	I_{DD3N}	440	400	360	mA
Burst read operating current	I_{DD4R}	1248	1128	1040	mA
Burst write operating current	I_{DD4W}	1160	1040	920	mA
Refresh current	I_{DD5}	1560	1520	1480	mA
Self refresh temperature current: MAX T_C = 85°C	I_{DD6}	96	96	96	mA
Self refresh temperature current (SRT-enabled): MAX T_C = 95°C	I_{DD6ET}	120	120	120	mA
All banks interleaved read current	I_{DD7}	1920	1800	1680	mA
Reset current	I_{DD8}	112	112	112	mA

Table 14: DDR3 I_{DD} Specifications and Conditions – 4GB (Die Revision D)

Values are for the MT41J512M8 DDR3 SDRAM only and are computed from values specified in the 4Gb (512 Meg x 8) component data sheet

Parameter	Symbol	1600	1333	1066	Units
Operating current 0: One bank ACTIVATE-to-PRECHARGE	I_{DD0}	600	520	480	mA
Operating current 1: One bank ACTIVATE-to-READ-to-PRECHARGE	I_{DD1}	696	656	616	mA
Precharge power-down current: Slow exit	I_{DD2P0}	160	160	160	mA
Precharge power-down current: Fast exit	I_{DD2P1}	296	256	240	mA
Precharge quiet standby current	I_{DD2Q}	376	336	312	mA
Precharge standby current	I_{DD2N}	400	360	320	mA
Precharge standby ODT current	I_{DD2NT}	400	360	320	mA
Active power-down current	I_{DD3P}	504	464	424	mA
Active standby current	I_{DD3N}	496	456	416	mA
Burst read operating current	I_{DD4R}	1496	1336	1176	mA
Burst write operating current	I_{DD4W}	1320	1160	1000	mA
Refresh current	I_{DD5}	1760	1680	1640	mA
Self refresh temperature current: MAX T_C = 85°C	I_{DD6}	176	176	176	mA
Self refresh temperature current (SRT-enabled): MAX T_C = 95°C	I_{DD6ET}	224	224	224	mA
All banks interleaved read current	I_{DD7}	2320	2000	1680	mA
Reset current	I_{DD8}	176	176	176	mA

Table 15: DDR3 I_{DD} Specifications and Conditions – 4GB (Die Revision E)

Values are for the MT41J512M8 DDR3 SDRAM only and are computed from values specified in the 4Gb (512 Meg x 8) component data sheet

Parameter	Symbol	1600	1333	1066	Units
Operating current 0: One bank ACTIVATE-to-PRECHARGE	I_{DD0}	440	376	352	mA
Operating current 1: One bank ACTIVATE-to-READ-to-PRECHARGE	I_{DD1}	528	496	472	mA
Precharge power-down current: Slow exit	I_{DD2P0}	144	144	144	mA
Precharge power-down current: Fast exit	I_{DD2P1}	256	224	208	mA
Precharge quiet standby current	I_{DD2Q}	256	224	216	mA
Precharge standby current	I_{DD2N}	256	323	224	mA
Precharge standby ODT current	I_{DD2NT}	312	280	256	mA
Active power-down current	I_{DD3P}	304	280	256	mA
Active standby current	I_{DD3N}	304	280	256	mA
Burst read operating current	I_{DD4R}	1256	1120	984	mA
Burst write operating current	I_{DD4W}	1000	880	760	mA
Refresh current	I_{DD5}	1880	1824	1792	mA
Self refresh temperature current: MAX T_C = 85°C	I_{DD6}	160	160	160	mA
Self refresh temperature current (SRT-enabled): MAX T_C = 95°C	I_{DD6ET}	200	200	200	mA
All banks interleaved read current	I_{DD7}	1760	1520	1280	mA
Reset current	I_{DD8}	160	160	160	mA

Serial Presence-Detect EEPROM

For the latest SPD data, refer to Micron's SPD page: www.micron.com/SPD.

Table 16: Serial Presence-Detect EEPROM DC Operating Conditions

All voltages referenced to V_{DDSPD}

Parameter/Condition	Symbol	Min	Max	Units
Supply voltage	V_{DDSPD}	3.0	3.6	V
Input low voltage: Logic 0; All inputs	V_{IL}	–0.45	V_{DDSPD} x 0.3	V
Input high voltage: Logic 1; All inputs	V_{IH}	V_{DDSPD} x 0.7	V_{DDSPD} + 1.0	V
Output low voltage: I_{OUT} = 3mA	V_{OL}	–	0.4	V
Input leakage current: V_{IN} = GND to V_{DD}	I_{LI}	0.1	2.0	µA
Output leakage current: V_{OUT} = GND to V_{DD}	I_{LO}	0.05	2.0	µA

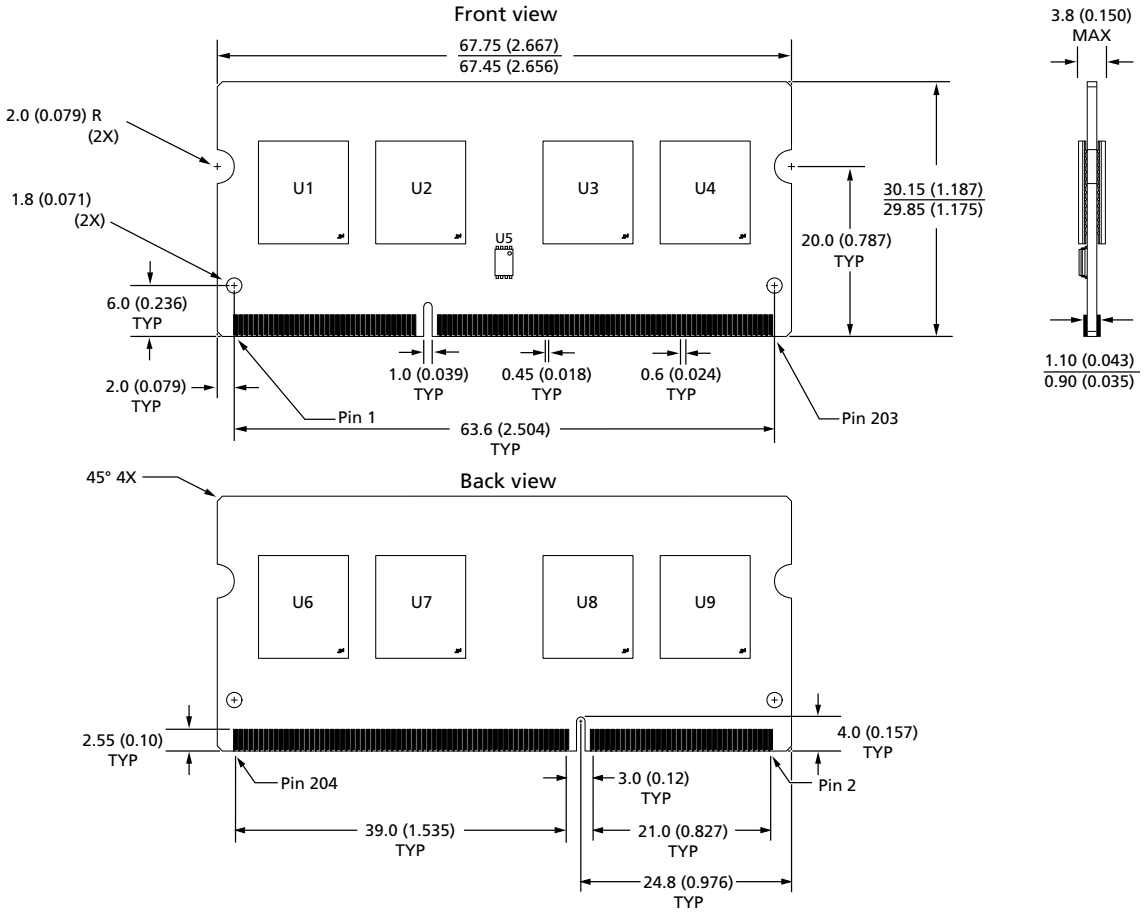
Table 17: Serial Presence-Detect EEPROM AC Operating Conditions

Parameter/Condition	Symbol	Min	Max	Units	Notes
Clock frequency	^{t}SCL	10	400	kHz	
Clock pulse width HIGH time	^{t}HIGH	0.6	–	µs	
Clock pulse width LOW time	^{t}LOW	1.3	–	µs	
SDA rise time	^{t}R	–	300	µs	1
SDA fall time	^{t}F	20	300	ns	1
Data-in setup time	^{t}SU:DAT	100	–	ns	
Data-in hold time	^{t}HD:DI	0	–	µs	
Data-out hold time	^{t}HD:DAT	200	900	ns	
Data out access time from SCL LOW	^{t}AA:DAT	0.2	0.9	µs	2
Start condition setup time	^{t}SU:STA	0.6	–	µs	3
Start condition hold time	^{t}HD:STA	0.6	–	µs	
Stop condition setup time	^{t}SU:STO	0.6	–	µs	
Time the bus must be free before a new transition can start	^{t}BUF	1.3	–	µs	
WRITE time	^{t}W	–	10	ms	

Notes:
1. Guaranteed by design and characterization, not necessarily tested.
2. To avoid spurious start and stop conditions, a minimum delay is placed between the falling edge of SCL and the falling or rising edge of SDA.
3. For a restart condition, or following a WRITE cycle.

Module Dimensions

Figure 3: 204-Pin DDR3 SODIMM



Notes:
1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.
2. The dimensional diagram is for reference only.

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