

DDR3 SDRAM Data Sheet Addendum

MT41J512M4 – 64 Meg x 4 x 8 Banks

MT41J256M8 – 32 Meg x 8 x 8 Banks

MT41J128M16 – 16 Meg x 16 x 8 Banks

Features

- $V_{DD} = V_{DDQ} = 1.5V \pm 0.075V$
- 1.5V center-terminated push/pull I/O
- Differential bidirectional data strobe
- 8n-bit prefetch architecture
- Differential clock inputs (CK, CK#)
- 8 internal banks
- Nominal and dynamic on-die termination (ODT) for data, strobe, and mask signals
- Programmable CAS READ latency (CL)
- Posted CAS additive latency (AL)
- Programmable CAS WRITE latency (CWL) based on t_{CK}
- Fixed burst length (BL) of 8 and burst chop (BC) of 4 (via the mode register set [MRS])
- Selectable BC4 or BL8 on-the-fly (OTF)
- Self refresh mode
- T_C of 0°C to 95°C
 - 64ms, 8192 cycle refresh at 0°C to 85°C
 - 32ms, 8192 cycle refresh at 85°C to 95°C
- Self refresh temperature (SRT)
- Write leveling
- Multipurpose register
- Output driver calibration

Options¹

- Configuration
 - 512 Meg x 4
 - 256 Meg x 8
 - 128 Meg x 16
- FBGA package (Pb-free) – x4, x8
 - 78-ball (8mm x 10.5mm) Rev. M, K
 - 78-ball (9mm x 11.5mm) Rev. D
- FBGA package (Pb-free) – x16
 - 96-ball (9mm x 14mm) Rev. D
 - 96-ball (8mm x 14mm) Rev. K
- Timing – cycle time
 - 938ps @ CL = 14 (DDR3-2133)
 - 1.071ns @ CL = 13 (DDR3-1866)
 - 1.25ns @ CL = 11 (DDR3-1600)
 - 1.5ns @ CL = 9 (DDR3-1333)
 - 1.87ns @ CL = 7 (DDR3-1066)
- Special Options
 - Premium Lifecycle Product (PLP)
- Operating temperature
 - Commercial (0°C ≤ T_C ≤ +95°C)
 - Industrial (–40°C ≤ T_C ≤ +95°C)
- Revision

Marking

512M4
256M8
128M16

DA
HX

HA
JT

-093
-107
-125
-15E
-187E

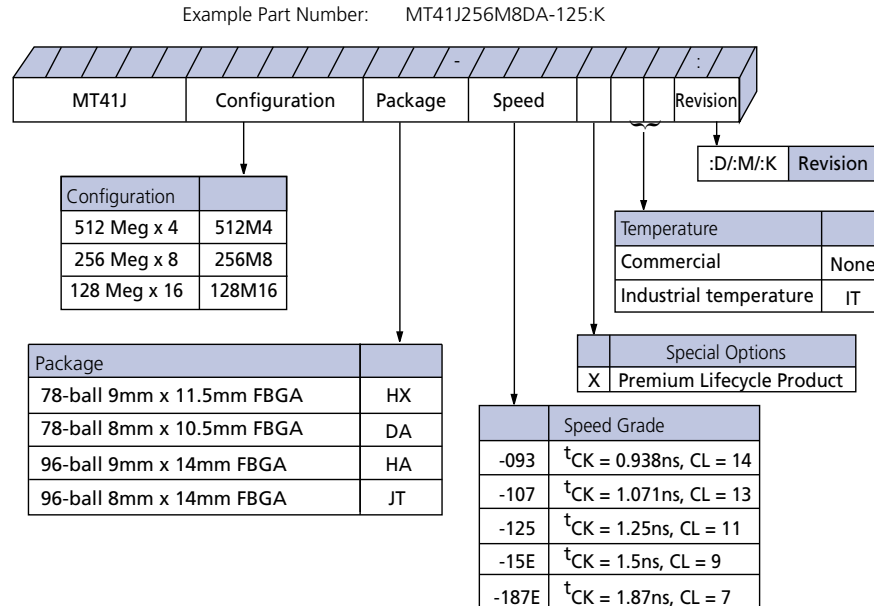
X

None
IT

:D/:M/:K

Note: 1. Not all options listed can be combined to define an offered product. Use the part catalog search on <http://www.micron.com> for available offerings.

Figure 1: DDR3 Part Numbers



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FBGA Part Marking Decoder

Due to space limitations, FBGA-packaged components have an abbreviated part marking that is different from the part number. For a quick conversion of an FBGA code, see the FBGA Part Marking Decoder on Micron's Web site: <http://www.micron.com>.



Revision History

Rev. A – 11/13

- Initial release based on the 2Gb x4, x8, x16 DDR3 SDRAM, Rev. Q 04/13 data sheet

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This data sheet contains minimum and maximum limits specified over the power supply and temperature range set forth herein.
Although considered final, these specifications are subject to change, as further product development and data characterization some-
times occur.