



BUK9635-55A

N-channel TrenchMOS logic level FET

Rev. 2 — 21 April 2011

Product data sheet

1. Product profile

1.1 General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product has been designed and qualified to the appropriate AEC standard for use in automotive critical applications.

1.2 Features and benefits

- AEC Q101 compliant
- Low conduction losses due to low on-state resistance

1.3 Applications

- Automotive and general purpose power switching

1.4 Quick reference data

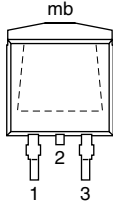
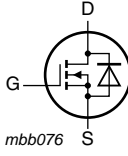
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}$	-	-	55	V
I_D	drain current	$T_{mb} = 25\text{ °C}$	-	-	34	A
P_{tot}	total power dissipation		-	-	85	W
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 25\text{ A}; T_j = 25\text{ °C}$	-	24	32	m Ω
		$V_{GS} = 5\text{ V}; I_D = 25\text{ A}; T_j = 25\text{ °C}$	-	26	35	m Ω
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 14\text{ A}; V_{sup} \leq 25\text{ V}; R_{GS} = 50\text{ }\Omega; V_{GS} = 5\text{ V}; T_{j(init)} = 25\text{ °C};$ unclamped	-	-	49	mJ

nexperia

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		
2	D	drain		
3	S	source		
mb	D	mounting base; connected to drain		

SOT404 (D2PAK)

3. Ordering information

Table 3. Ordering information

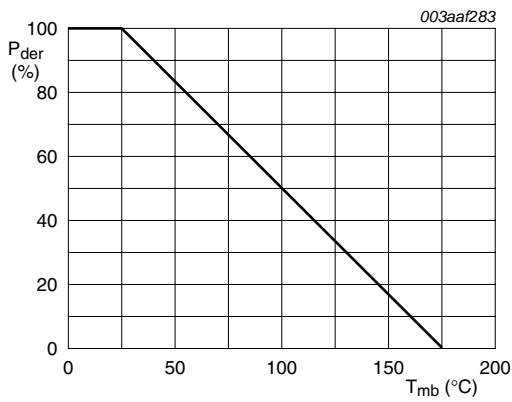
Type number	Package		
	Name	Description	Version
BUK9635-55A	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404

4. Limiting values

Table 4. Limiting values

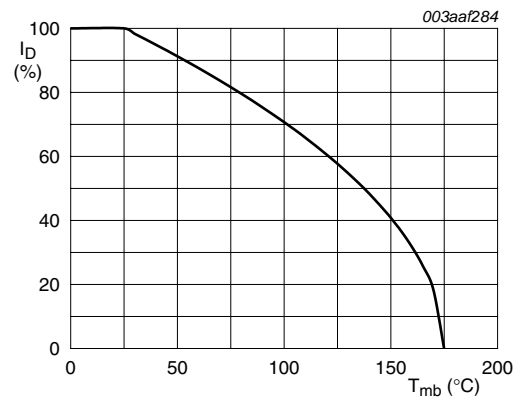
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$	-	55	V
V_{DGR}	drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$	-	55	V
V_{GS}	gate-source voltage		-10	10	V
I_D	drain current	$T_{mb} = 100\text{ °C}$	-	24	A
		$T_{mb} = 25\text{ °C}$	-	34	A
I_{DM}	peak drain current	$T_{mb} = 25\text{ °C}$; pulsed	-	133	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$	-	85	W
T_{stg}	storage temperature		-55	175	°C
T_j	junction temperature		-55	175	°C
V_{GSM}	peak gate-source voltage	pulsed; $t_p \leq 50\text{ }\mu\text{s}$	-15	15	V
Source-drain diode					
I_S	source current	$T_{mb} = 25\text{ °C}$	-	34	A
I_{SM}	peak source current	pulsed; $T_{mb} = 25\text{ °C}$	-	133	A
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 14\text{ A}$; $V_{sup} \leq 25\text{ V}$; $R_{GS} = 50\text{ }\Omega$; $V_{GS} = 5\text{ V}$; $T_{j(init)} = 25\text{ °C}$; unclamped	-	49	mJ



$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}\text{C})}} \times 100\%$$

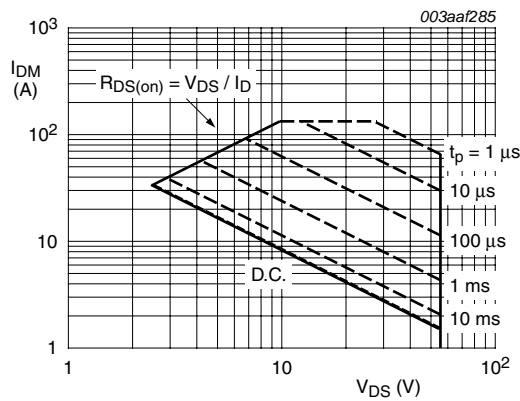
Fig 1. Normalized total power dissipation as a function of mounting base temperature



$$I_{der} = \frac{I_D}{I_{D(25^{\circ}\text{C})}} \times 100\%$$

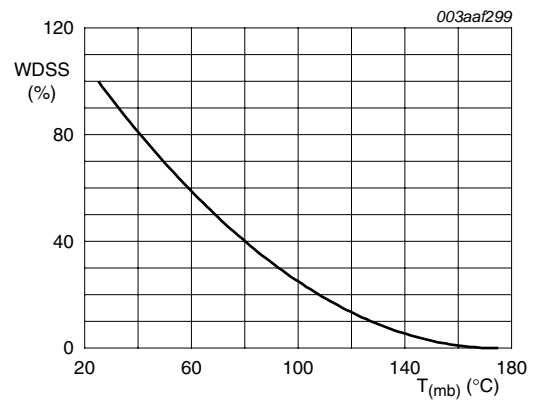
$V_{GS} \geq 5\text{ V}$

Fig 2. Normalized continuous drain current as a function of mounting base temperature



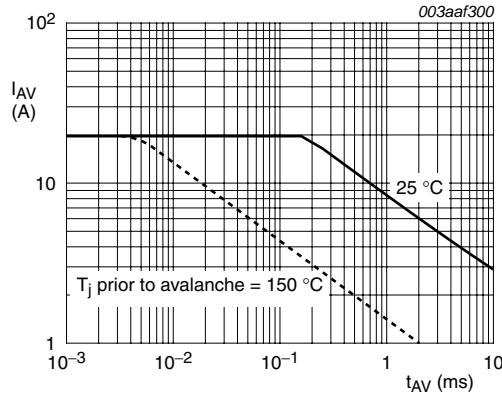
$T_{mb} = 25^{\circ}\text{C}$

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage



$I_D = 75\text{ A}$

Fig 4. Normalised drain-source non-repetitive avalanche energy as a function of mounting-base temperature



unclamped inductive load

Fig 5. Single-shot avalanche rating; avalanche current as a function of avalanche period

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base		-	-	1.8	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	minimum footprint; FR4 board	-	50	-	K/W

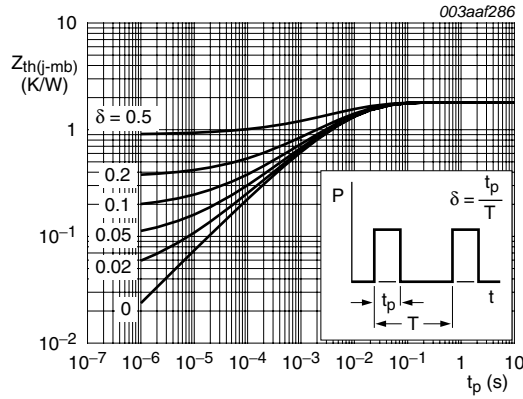


Fig 6. Transient thermal impedance from junction to mounting base as a function of pulse duration

6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ mV}; T_j = 25 \text{ }^\circ\text{C}$	55	-	-	V
		$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ mV}; T_j = -55 \text{ }^\circ\text{C}$	50	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ\text{C}$	-	-	2.3	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ\text{C}$	1	1.5	2	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ\text{C}$	0.5	-	-	V
I_{DSS}	drain leakage current	$V_{DS} = 55 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	0.05	10	μA
		$V_{DS} = 55 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 \text{ }^\circ\text{C}$	-	-	500	μA
I_{GSS}	gate leakage current	$V_{GS} = 10 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	2	100	nA
		$V_{GS} = -10 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	2	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 4.5 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$	-	26.5	38	m Ω
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$	-	24	32	m Ω
		$V_{GS} = 5 \text{ V}; I_D = 25 \text{ A}; T_j = 175 \text{ }^\circ\text{C}$	-	-	70	m Ω
		$V_{GS} = 5 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$	-	26	35	m Ω
Dynamic characteristics						
C_{iss}	input capacitance	$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}; f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ\text{C}$	-	880	1173	pF
C_{oss}	output capacitance		-	165	198	pF
C_{rss}	reverse transfer capacitance		-	111	152	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 30 \text{ V}; R_L = 1.2 \text{ }^\Omega; V_{GS} = 5 \text{ V}; R_{G(ext)} = 10 \text{ }^\Omega; T_j = 25 \text{ }^\circ\text{C}$	-	6	9	ns
t_r	rise time		-	36	55	ns
$t_{d(off)}$	turn-off delay time		-	96	134	ns
t_f	fall time		-	73	102	ns
L_D	internal drain inductance	from upper edge of drain mounting base to centre of die; $T_j = 25 \text{ }^\circ\text{C}$	-	2.5	-	nH
		from drain lead 6 mm from package to centre of die; $T_j = 25 \text{ }^\circ\text{C}$	-	4.5	-	nH
L_S	internal source inductance	from source lead to source bond pad; $T_j = 25 \text{ }^\circ\text{C}$	-	7.5	-	nH
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 25 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	0.85	1.2	V
		$I_S = 34 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	1.1	-	V
t_{rr}	reverse recovery time	$I_S = 34 \text{ A}; di_S/dt = -100 \text{ A}/\mu\text{s}; V_{GS} = -10 \text{ V}; V_{DS} = 30 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	36	-	ns
Q_r	recovered charge		-	0.07	-	μC

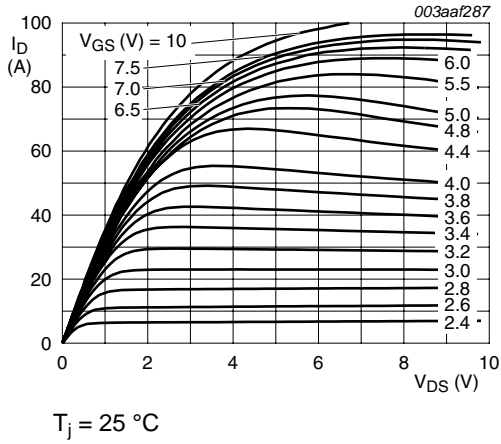


Fig 7. Output characteristics: drain current as a function of drain-source voltage; typical values

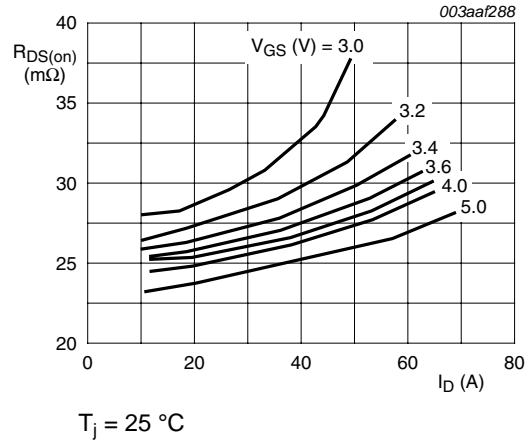


Fig 8. Drain-source on-state resistance as a function of drain current; typical values

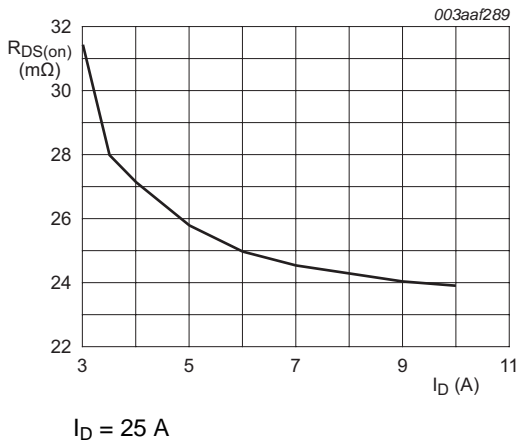


Fig 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

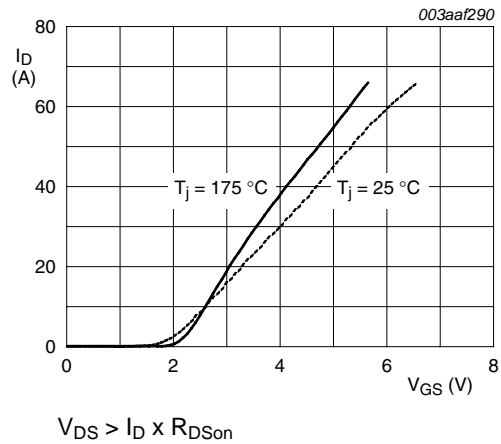


Fig 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values

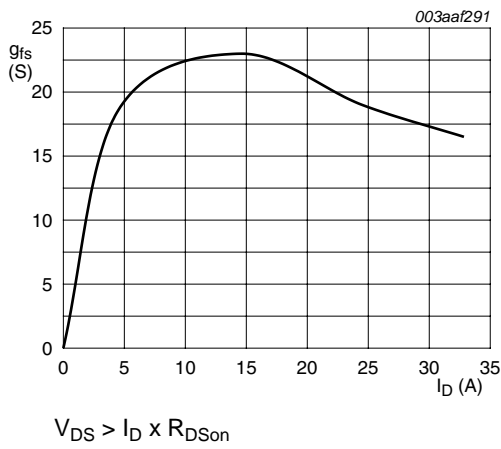
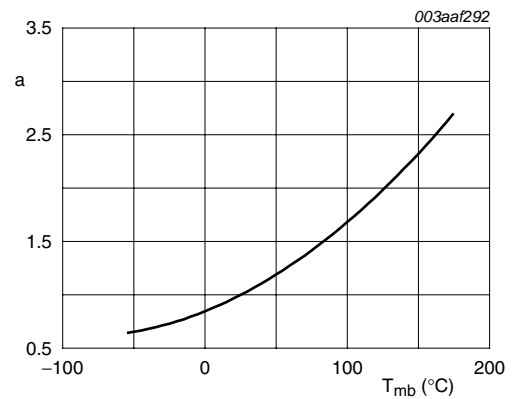


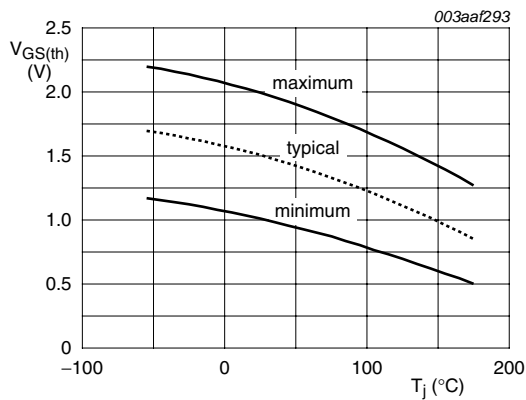
Fig 11. Forward transconductance as a function of drain current; typical values



$$a = \frac{R_{DSon}}{R_{DSon(25^\circ C)}}$$

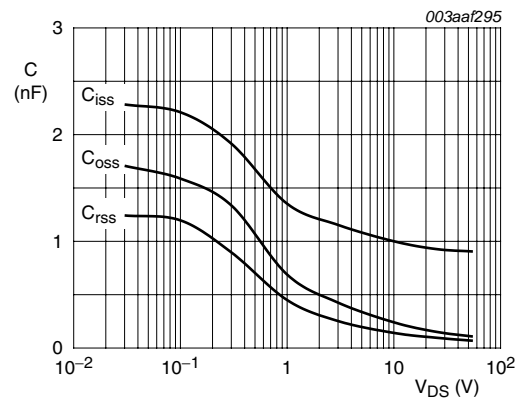
$I_D = 25 \text{ A}; V_{GS} = 5 \text{ V}$

Fig 12. Normalized drain-source on-state resistance factor as a function of junction temperature



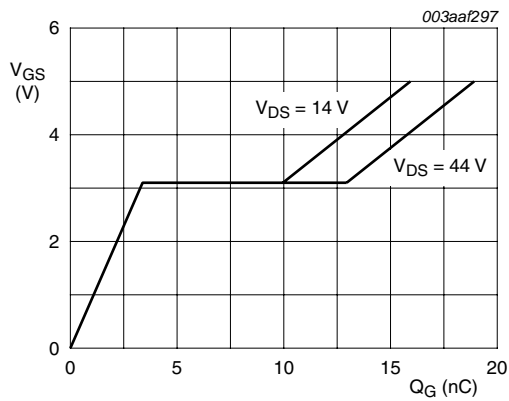
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

Fig 13. Gate-source threshold voltage as a function of junction temperature



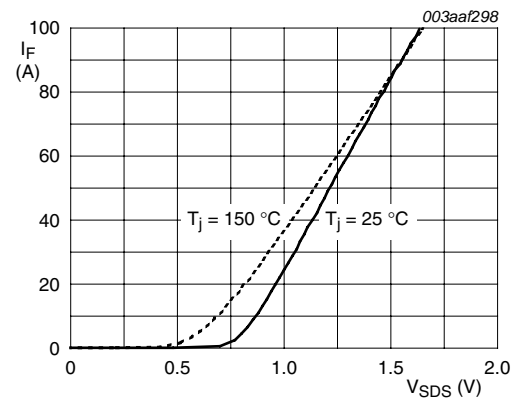
$V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$

Fig 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$T_j = 25\text{ }^\circ\text{C}$; $I_D = 25\text{ A}$

Fig 15. Gate-source voltage as a function of gate charge; typical values



$V_{GS} = 0\text{ V}$

Fig 16. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

7. Package outline

Plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)

SOT404



Fig 17. Package outline SOT404 (D2PAK)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BUK9635-55A v.2	20110421	Product data sheet	-	BUK9535_9635-55A_1
Modifications:	<ul style="list-style-type: none">• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.• Legal texts have been adapted to the new company name where appropriate.• Type number BUK9635-55A separated from data sheet BUK9535_9635-55A_1.			
BUK9535_9635-55A_1	20000201	Product specification	-	-

9. Legal information

9.1 Data sheet status

Document status [1] [2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nexperia.com>.

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