Ordering number : ENA1021

SANYO Semiconductors
DATA SHEET

CMOS IC

LC75100M — Digital Echo IC with Microphone Amplifier Circuit

Overview

The LC75100M is a digital echo IC that incorporates a microphone amplifier and is ideal for use in minicompo and other audio systems.

Functions

- Digital echo IC incorporating a microphone amplifier.

Specitications

Absolute Maximum Rating at Ta = 25°C, V_{SS} = 0V

Parameter	Symbol	Pin Name	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max	V_{DD}		10.5	V
Allowable power dissipation	Pd max		Ta≤70°C	350	mW
Operating ambient temperature	Topr			-20 to +70	°C
Storage ambient temperature	Tstg			-40 to +125	°C

Allowable Operating Ranges (Operating Conditions) at Ta = 25°C

Parameter	Symbol	Pin Name	min	typ	max	unit
Recommended supply voltage	V_{DD}	V_{DD}		9.0		V
Operating supply voltage range	V_{DD}opg	V_{DD}	8.0		10.0	
Input high-level voltage	V_{IH}		2.0		3.5	V
Input low-level voltage	V_{IL}		0		0.5	V
Input pulse width	tϕW		1.0			µs
Hold time	thold		1.0			µs
Operating frequency	fopg				500	kHz

SANYO Semiconductor Co., Ltd.
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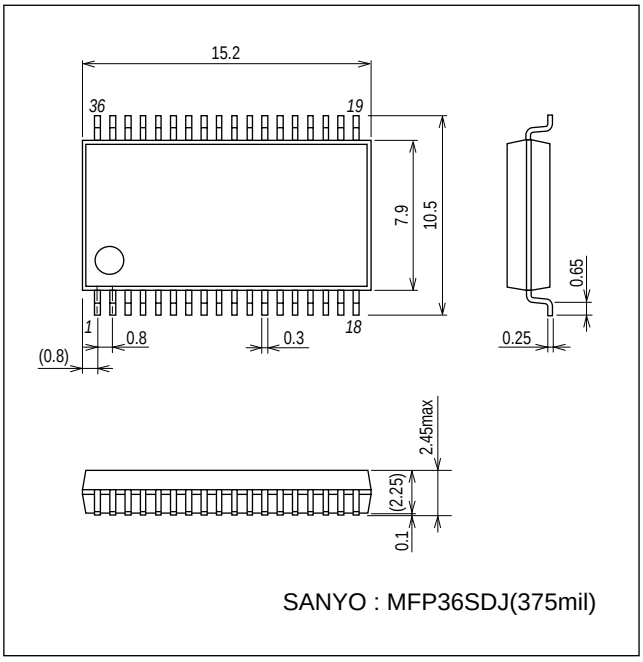
Electrical Characteristics at Ta=25°C, V_{DD}=9.0V, fin=1kHz, RL=10kΩ

Parameter	Symbol	Pin	Conditions	min	typ	max	unit
Quiescent current	$I_{DD}O$	V_{DD}			13	60	mA
Clock frequency	FCLK	OSC	OSC Ex.R=22kΩ	1.82	2.6	3.38	MHz
Mic-AMP (Input=MICIN1/MICIN2, Output=MICOUT1/MICOUT2, V_{IN}=-46dBV, VALC=VREF–1.414V, Mic-AMP NF Ex.R=6.2kΩ)							
Mic gain 1	VGM1		Mic-AMP NF Ex.R=0Ω	+50	+53	+56	dB
Mic gain 2	VGM2		Mic-AMP NF Ex.R=6.2kΩ	+33	+36	+39	dB
Maximum output voltage	VoTM		Mic Gain=+36dB, THD=1%, ALC=OFF	1.75			Vrms
Total harmonic distortion 1	THDM1		Mic Gain=+36dB, ALC=OFF, V_O=-10dBV		0.3	1.0	%
Total harmonic distortion 2	THDM2		Mic Gain=+36dB, ALC=ON, V_O=-10dBV, V_{IN}=0dBV		1.5	2.0	%
Output noise voltage	VNOM		Mic Gain=+36dB, JIS-A		-60	-55	dBV
Input impedance	ZiM			37	50	62	kΩ
ALC attack time	TaA				30		ms
ALC release time	TaR				1.0		s
Digital Echo (Input=IN1/IN2, Output=ECHOOUT, V_{IN}=-10dBV, Delay Time=100ms, Mic volume 1/2=0dB, feedback volume=-∞)							
Delay time	DT	ECHOOUT	FCLK=2.6MHz		100		ms
Output level deviation	VGE	ECHOOUT		+2.5	+5.5	+8.5	dB
Maximum output voltage	VoE	ECHOOUT	THD=10%	1.5			Vrms
Total harmonic distortion	THDE	ECHOOUT	Filter=A Filter		0.5	2.0	%
Output noise voltage	VNOE	ECHOOUT	Filter=A Filter		-65	-55	dBV
Stereo Line (Input=LCHIN/RCHIN, Output=LCHOUT/RCHOUT, V_{IN}=-10dBV, Line select=STEREO, Mic volume 1/2=ECHO volume=-∞)							
Output level deviation	VGS	LCHOUT/RCHOUT	V_{IN}=-10dBV	-2.5	-0.5	+1.5	dB
Maximum output voltage	VoS	LCHOUT/RCHOUT	THD=1%	1.5			Vrms
Total harmonic distortion	THDS	LCHOUT/RCHOUT	JIS-A, Stereo out		0.03	0.1	%
Output noise voltage	VNOS	LCHOUT/RCHOUT	JIS-A, ECHO OFF		-85	-75	dBV
Vocal removal rate	VC	LCHOUT/RCHOUT	JIS-A, V_{IN}=-10dBV	-20	-18	-16	dB

Package Dimensions

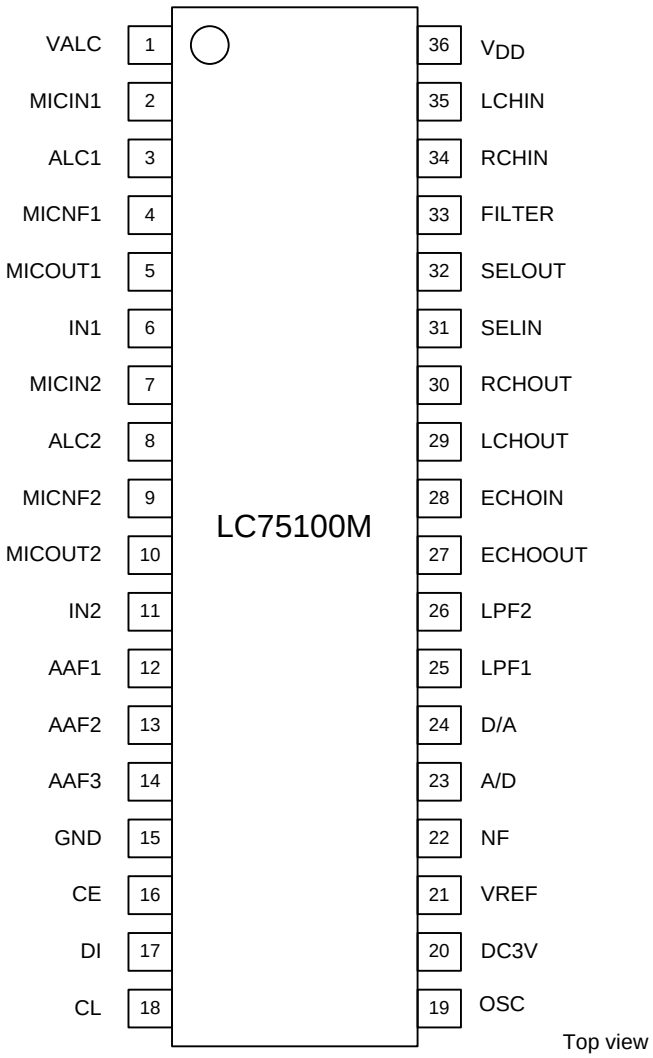
unit : mm (typ)

3263



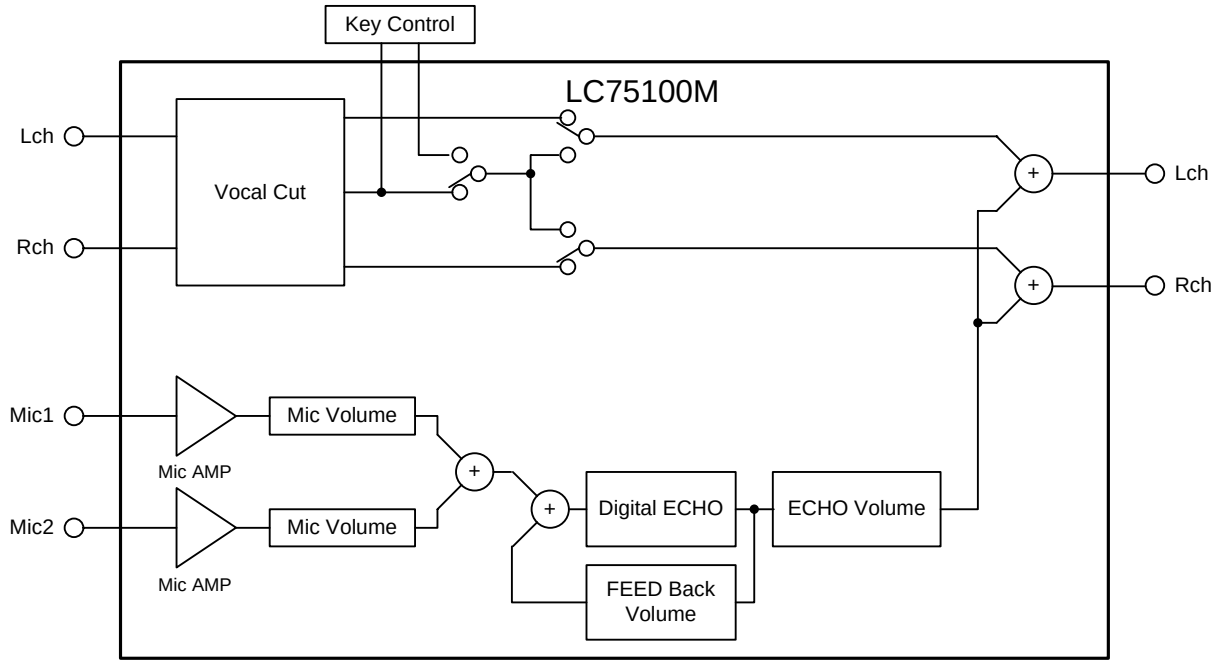
SANYO : MFP36SDJ(375mil)

Pin Assignment

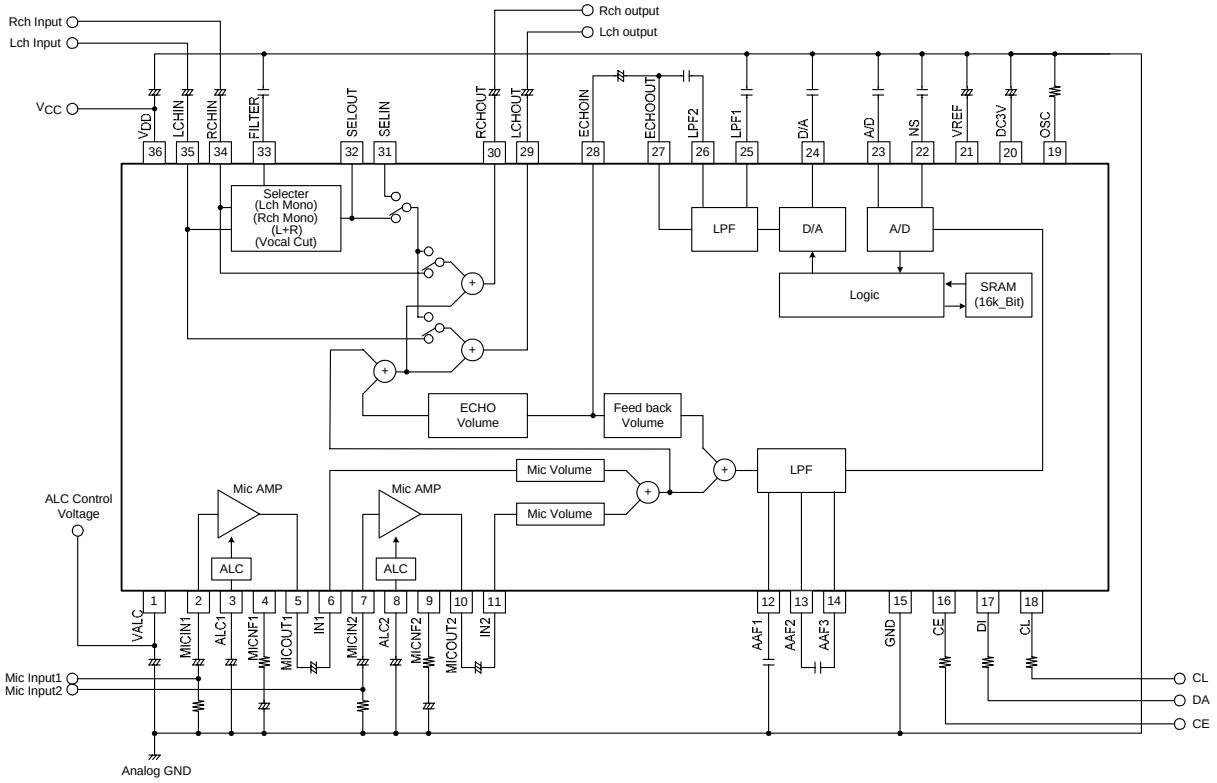


Top view

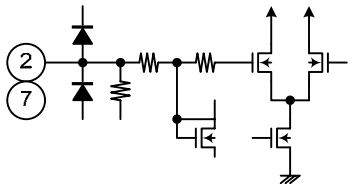
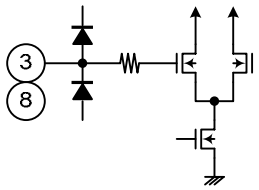
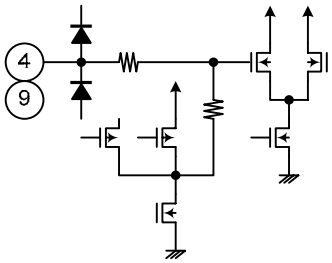
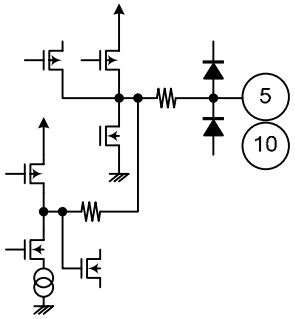
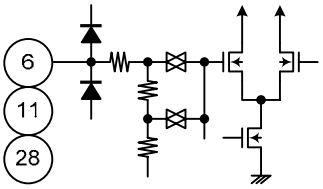
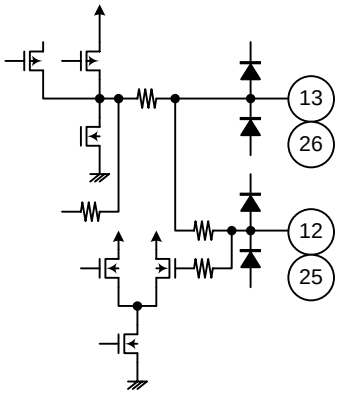
System Configuration Diagram



Block Diagram



Pin Description

Pin No.	Pin Name	Voltage	Internal Equivalent Circuit	Description
1	VALC			ALC detection voltage setting pin
2 7	MICIN1 MICIN2	1/2 V_{DD}		Mic signal input 1 Mic signal input 2
3 8	ALC1 ALC2			Auto level control pin 1 Auto level control pin 2
4 9	MICNF1 MICNF2	1/2 V_{DD}		Mic feedback signal input pin 1 Mic feedback signal input pin 2
5 10	MICOUT1 MICOUT2	1/2 V_{DD}		Mic signal output pin 1 Mic signal output pin 2
6 11 28	IN1 IN2 ECHOIN	1/2 V_{DD}		ECHO circuit signal input pin 1 ECHO circuit signal input pin 2 ECHO signal input pin
12 13 25 26	AAF1 AAF2 LPF1 LPF2	1/2 V_{DD}		AAF input pin 1 AAF input pin 2 LPF input pin 1 LPF input pin 2

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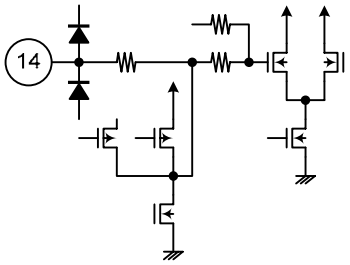
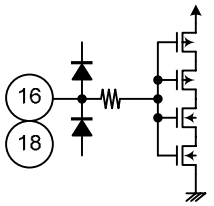
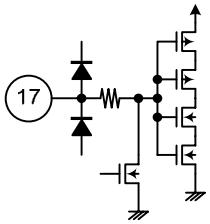
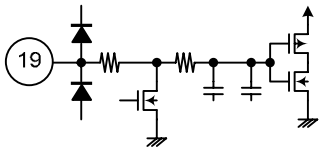
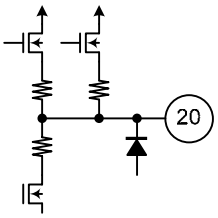
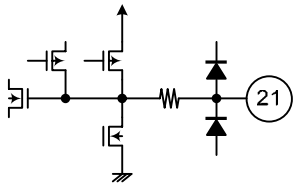
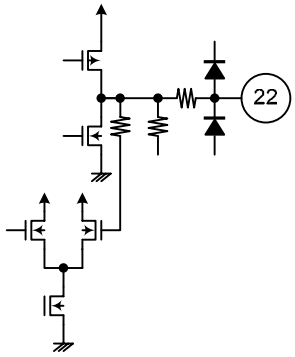
Pin No.	Pin Name	Voltage	Internal Equivalent Circuit	Description
14	AAF3	1/2 V_{DD}		AAF input pin 3
15	GND	0V		Analog GND
16 18	CE CL(SCL)	0V/3.3V		CCB CE pin CCB CL pin/I^2C bus SCL pin
17	DI(SDA)	0V/3.3V		CCB DI pin/I^2C bus SDA pin
19	OSC	0V/3.3V		Oscillator circuit adjustment pin
20	DC3V	3.3V		Power supply for logic block
21	VREF	1/2 V_{DD}		Internal reference voltage
22	NF	1/2 V_{DD}		A/D pin

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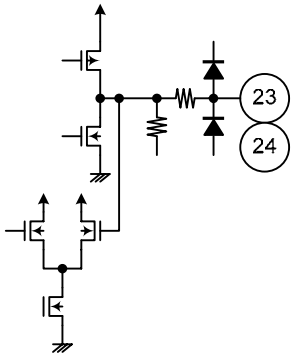
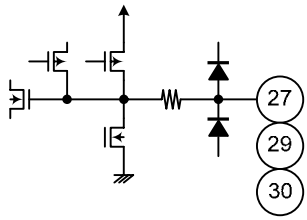
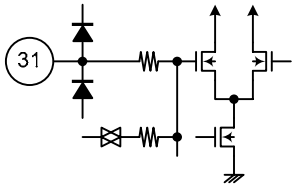
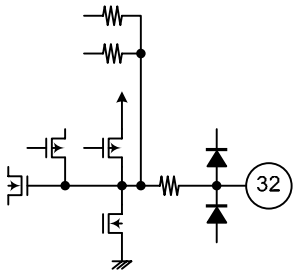
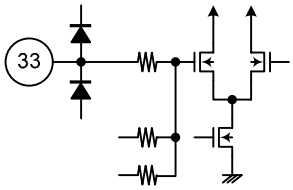
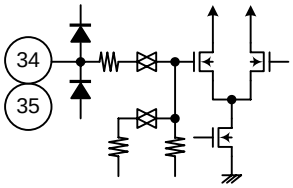
Pin No.	Pin Name	Voltage	Internal Equivalent Circuit	Description
23 24	A/D D/A	1/2 V_{DD}		A/D pin D/A pin
27 29 30	ECHOOUT LCHOUT RCHOUT	1/2 V_{DD}		ECHO signal output pin Lch output Rch output
31	SELIN	1/2 V_{DD}		Selector input pin
32	SELOUT	1/2 V_{DD}		Selector output pin
33	FILTER	1/2 V_{DD}		Filter input pin 1
34 35	RCHIN LCHIN	1/2 V_{DD}		Rch input pin Lch input pin
36	V_{DD}			Supply voltage

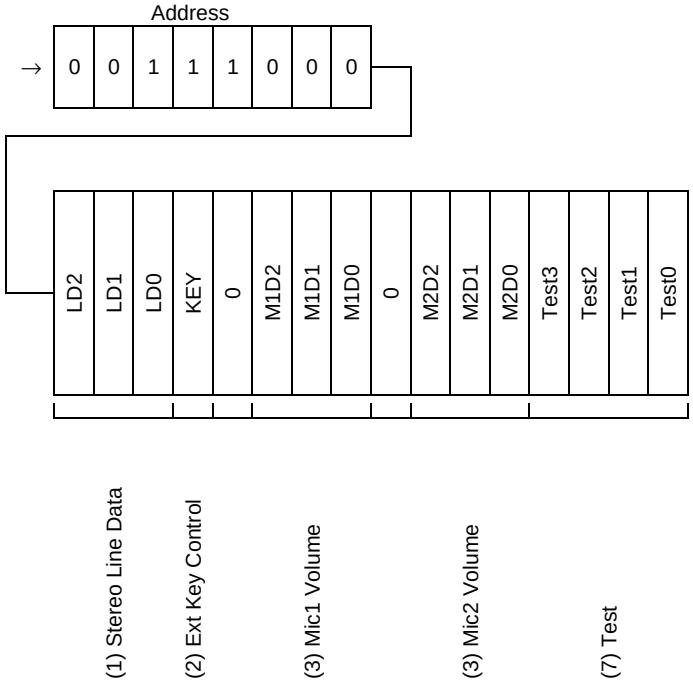
Control Data (Serial Data Input) Format

Various settings of the LC75100M can be configured with a CCB or I^2C bus. When controlling the LC75100M via an I^2C bus, set and hold the CE pin at low level.

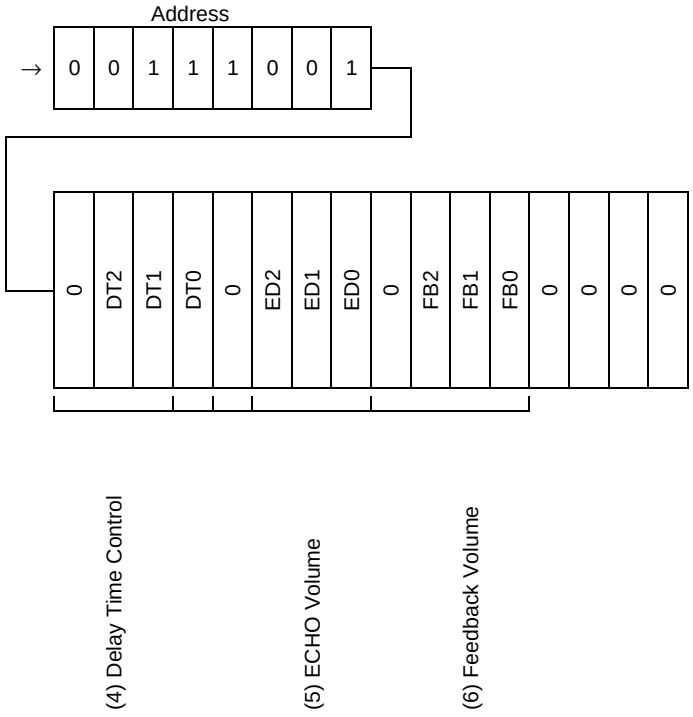
(1) CCB control

① Control register

• IN1 mode

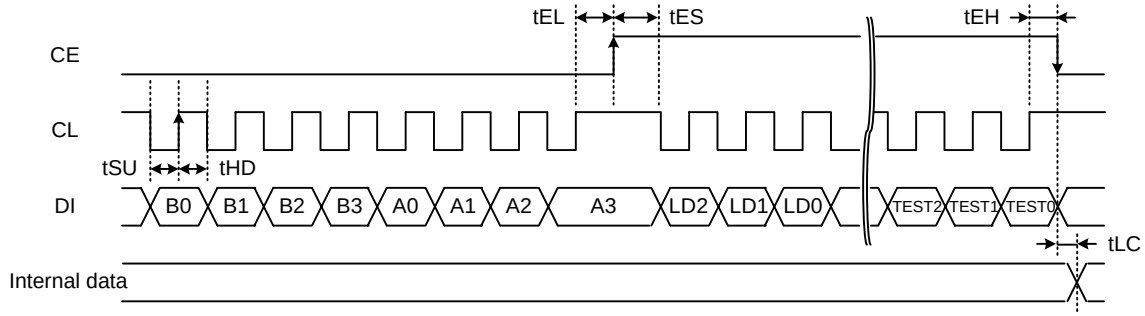


• IN2 mode

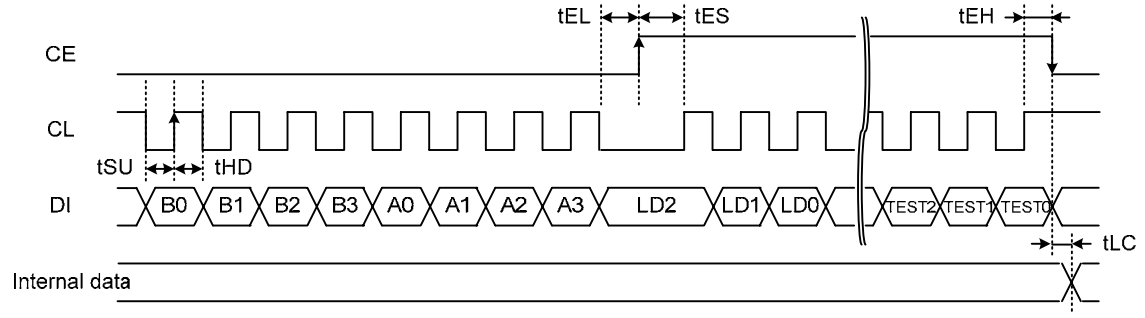


② Serial data input

• CL: Normal Hi



• CL: Normal Low

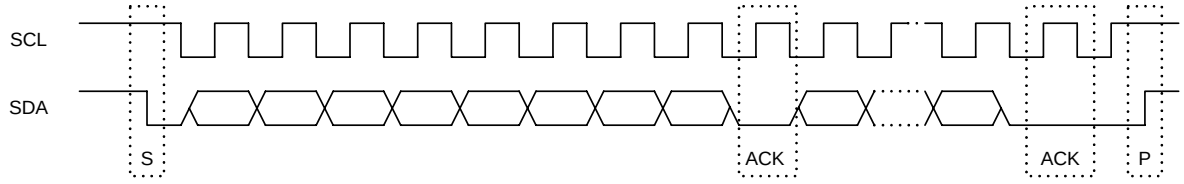


(2) I^2C bus control

I^2C bus register

The I^2C (Inter IC) bus is a bus system developed by Philips Corporation.

It controls the start and stop condition with SDA (Serial Data) and SCL (Serial Clock). The outputs of these signals are of open drain type and wired OR.



S: Start condition/P: Stop condition/ACK: Acknowledge

Data is transferred MSB first.
One unit is made up of 8 bits. ACK is returned by the slave for acknowledgement.
The slave IC reads the data on the rising edge of SCL.
The master IC changes the data on the falling edge of SCL.

① Control registers

• Slave Address

MSB							LSB
0	0	1	1	1	0	0	0

Note: The LC75100M can be used in the receive only mode if the LSB is set to 0.

• I^2C Data

Function	Sub Address		Data							
	BINARY	HEX	D7	D6	D5	D4	D3	D2	D1	D0
Stereo line select	0000 0001	01	LD2	LD1	LD0	KEY	0	MID2	MID1	MID0
Mic volume control	0000 0010	02	0	M2D2	M2D1	M2D0	TEST3	TEST2	TEST1	TEST0
Delay time control	0000 0011	03	0	DT2	DT1	DT0	0	ED2	ED1	ED0
ECHO/Feedback volume	0000 1000	04	0	FB2	FB1	FB0	0	0	0	0

*: All test bits must be set to 0.

Control Data Description (common to both CCB and I^2C bus)

No	Control Block/Data	Description	Related Data
(1)	Line Select LD2 LD1 LD0	• Determines the line output.	
(2)	External key control enable/disable key	• Determines the path that uses the external key control.	
(3)	Mic volume gain data M1D2 M1D1 M1D0 M2D2 M2D1 M2D0	• Determines the gain of mic inputs 1 and 2.	

LD2	LD1	LD0	
0	0	0	Stereo output
0	0	1	Lch Mono output
0	1	0	Rch Mono output
0	1	1	L+R/2 output
1	0	0	Vocal cut output
1	0	1	Reserve
1	1	0	Reserve
1	1	1	Reserve

KEY	External Key Control
0	Disabled
1	Enabled

M1D2 M2D2	M1D1 M2D1	M1D0 M2D0	
0	0	0	0dB
0	0	1	-2dB
0	1	0	-4dB
0	1	1	-6dB
1	0	0	-9dB
1	0	1	-12dB
1	1	0	-15dB
1	1	1	-∞

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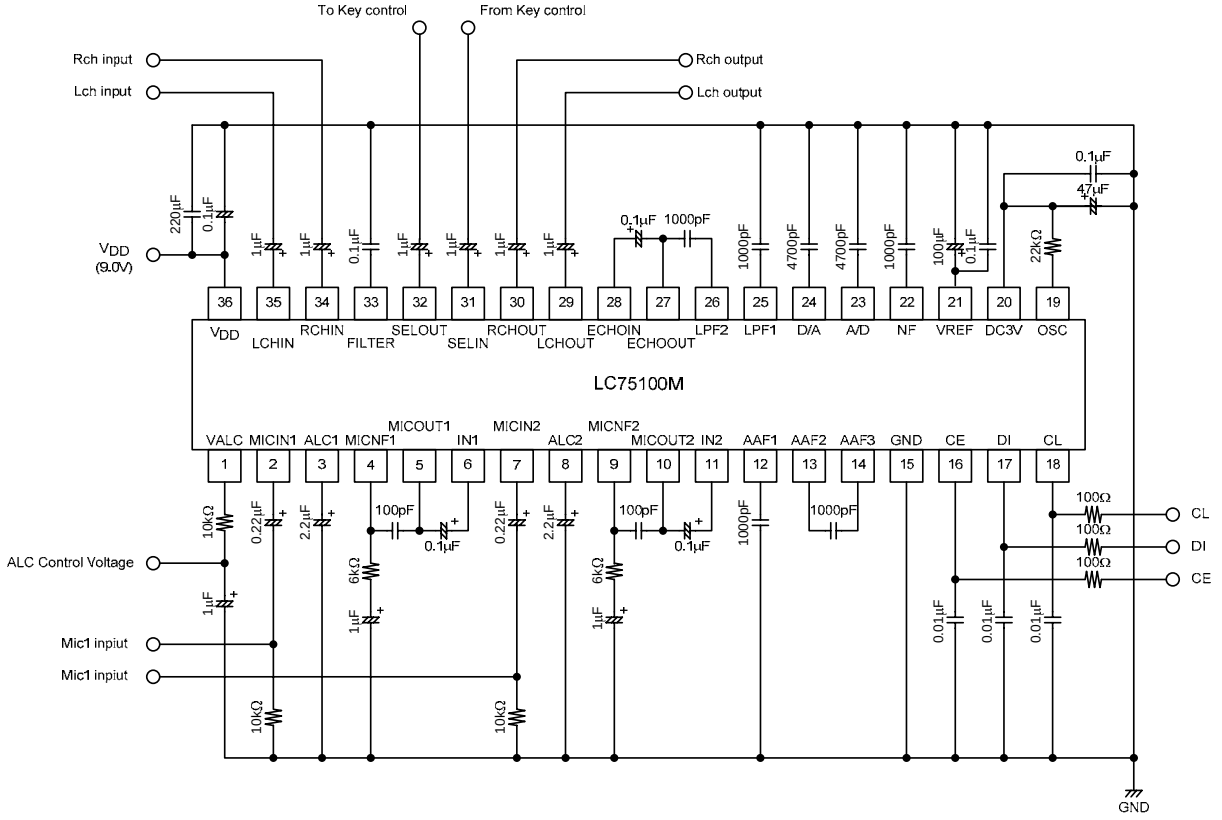
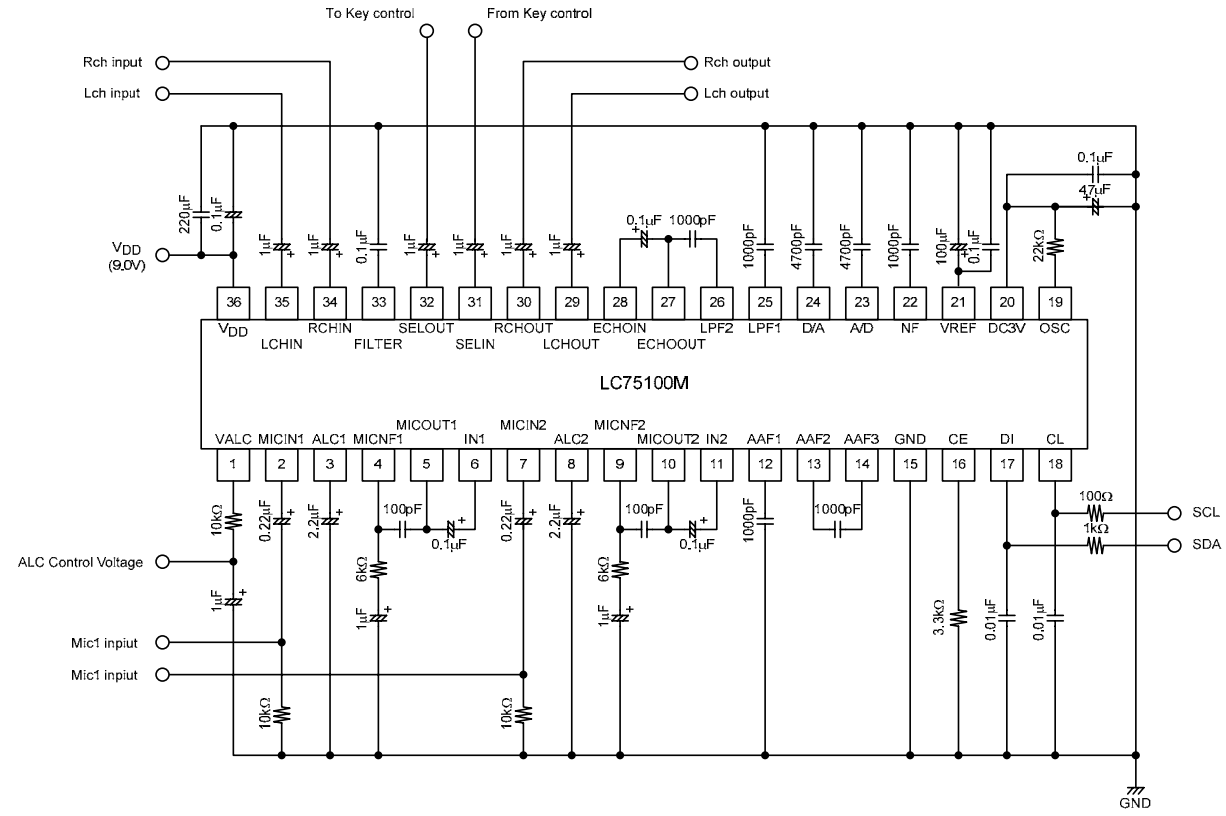
<table>
<tr><th>No</th><th>Control Block/Data</th><th>Description</th><th>Related Data</th></tr>
<tr><td>(4)</td><td>Delay time data
DT2
DT1
DT0</td><td>• Determines the echo delay time.
<table>
<tr><th>DT2</th><th>DT1</th><th>DT0</th><th></th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>OFF</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>75ms</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>100ms</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>125ms</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>150ms</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>175ms</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>200ms</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Reserved</td></tr>
</table></td><td></td></tr>
<tr><td>(5)</td><td>Echo volume gain data
ED2
ED1
ED0</td><td>• Determines the gain of the echo output.
<table>
<tr><th>ED2</th><th>ED1</th><th>ED0</th><th></th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0dB</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>-2dB</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>-4dB</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>-6dB</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>-9dB</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>-12dB</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>-15dB</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>-∞</td></tr>
</table></td><td></td></tr>
<tr><td>(6)</td><td>Feedback volume gain data
FB2
FB1
FB0</td><td>• Determines the volume of the echo feedback.
<table>
<tr><th>FB2</th><th>FB1</th><th>FB0</th><th></th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>-2dB</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>-4dB</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>-6dB</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>-8dB</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>-∞</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Reserve</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Reserve</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Reserve</td></tr>
</table></td><td></td></tr>
<tr><td>(7)</td><td>IC test data
TEST3
TEST2
TEST1
TEST0</td><td>• Used for testing the IC.
TEST3 to TEST0 must all be set to 0.</td><td></td></tr>
</table>

Recommended Circuit (Mic-Gain=-36dB)

[CCB Control]

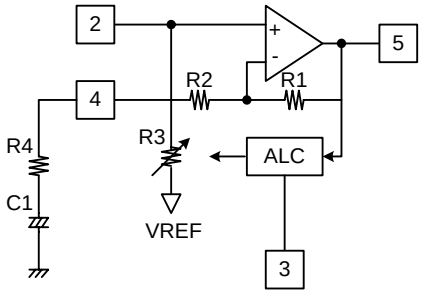


[I²C Control]



Setting the Mic Amplifier Gain

The mic amplifier gain can be adjusted by the resistors connected to pins 3 and 34. Moreover, the low frequency region can be cut off by connecting a capacitor. The mic amplifer has a built-in ALC (Auto Level Control) and the output level can be controlled by applying the reference voltage to pin 1.



(1) Setting the mic AMP gain

- R1=562.3kΩ, R2=1.0kΩ

[When Mic Gain=45dB]

R4=(R1/Mic Gain)-R2
=562.3k/177.8-1k
≈2.2kΩ

(2) Determining the fc

$$fc = \frac{1}{2\pi(R1+1k)C1}$$

(3) Setting the ALC operating voltage