DDR2 SDRAM Registered MiniDIMM

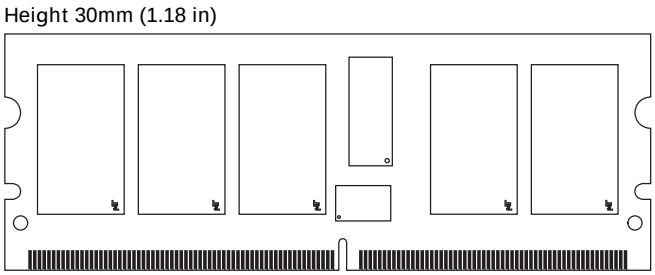
MT9HTF3272(P)K – 256MB
MT9HTF6472(P)K – 512MB
MT9HTF12872(P)K – 1GB

For component specifications, refer to Micron's Web site: www.micron.com/products/dram/ddr2

Features

- 244-pin, mini dual in-line memory module (MiniDIMM)
- Fast data transfer rates: PC2-3200, PC2-4200, or PC2-5300
- Supports ECC error detection and correction
- 256MB (32 Meg x 72), 512MB (64 Meg x 72), 1GB (128 Meg x 72)
- $V_{DD} = V_{DD}Q = +1.8V$
- $V_{DDSPD} = +1.7V$ to $+3.6V$
- JEDEC standard 1.8V I/O (SSTL_18 compatible)
- Differential data strobe (DQS, DQS#) option
- Four-bit prefetch architecture
- DLL to align DQ and DQS transitions with CK
- Multiple internal device banks for concurrent operation
- Supports duplicate output strobe (RDQS/RDQS#)
- Programmable CAS# latency (CL)
- Posted CAS# additive latency (AL)
- WRITE latency = READ latency - 1 ^{t}CK
- Programmable burst lengths: 4 or 8
- Adjustable data-output drive strength
- 64ms, 8,192-cycle refresh
- On-die termination (ODT)
- Serial presence-detect (SPD) with EEPROM
- Gold edge contacts
- Single rank

Figure 8: 244-Pin DIMM (MO-244 R/C "A")



Options	Marking
• Parity	P
• Package	
244-pin DIMM (lead-free)	Y
• Frequency/CAS latency[1]	
2.5ns @ CL = 5 (DDR2-800)[2]	-80E
2.5ns @ CL = 6 (DDR2-800)[2]	-800
3ns @ CL = 5 (DDR2-667)	-667
3.75ns @ CL = 4 (DDR2-533)	-53E
5.0ns @ CL = 3 (DDR2-400)	-40E
• PCB height	
30mm (1.18in)	

Notes: 1. CL = CAS (READ) latency; registered mode will add one clock cycle to CL.
2. Not available in 256MB density.

Table 1: Address Table

	256MB	512MB	1GB
Refresh count	8K	8K	8K
Row addressing	8K (A0–A12)	16K (A0–A13)	16K (A0–A13)
Device bank addressing	4 (BA0, BA1)	4 (BA0, BA1)	8 (BA0, BA1, BA2)
Device page size per bank	1KB	1KB	1KB
Device configuration	256Mb (32 Meg x 8)	512Mb (64 Meg x 8)	1Gb (128 Meg x 8)
Column addressing	1K (A0–A9)	1K (A0–A9)	1K (A0–A9)
Module rank addressing	1 (S0#)	1 (S0#)	1 (S0#)

Table 2: Key Timing Parameters

Speed Grade	Industry Nomenclature	Data Rate (MT/s)				^{t}RCD (ns)	^{t}RP (ns)	^{t}RC (ns)
		CL = 6	CL = 5	CL = 4	CL = 3			
-80E	PC2-6400	–	800	533	–	12.5	12.5	55
-800	PC2-6400	800	667	–	–	15	15	55
-667	PC2-5300	–	667	533	400	15	15	55
-53E	PC2-4200	–	–	533	400	15	15	55
-40E	PC2-3200	–	–	400	400	15	15	55

Table 3: Part Numbers and Timing Parameters – 256MB
Base device: MT47H32M8, 256Mb DDR2 SDRAM

Part Number[1]	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Latency (CL - ^{t}RCD - ^{t}RP)
MT9HTF3272(P)KY-667__	256MB	32 Meg x 72	5.3 GB/s	3.0ns/667 MT/s	5-5-5
MT9HTF3272(P)KY-53E__	256MB	32 Meg x 72	4.3 GB/s	3.75ns/533 MT/s	4-4-4
MT9HTF3272(P)KY-40E__	256MB	32 Meg x 72	3.2 GB/s	5.0ns/400 MT/s	3-3-3

Table 4: Part Numbers and Timing Parameters – 512MB
Base device: MT47H64M8, 512Mb DDR2 SDRAM

Part Number[1]	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Latency (CL - ^{t}RCD - ^{t}RP)
MT9HTF6472(P)KY-80E__	512MB	64 Meg x 72	6.4 GB/s	2.5ns/800 MT/s	5-5-5
MT9HTF6472(P)KY-800	512MB	64 Meg x 72	6.4 GB/s	2.5ns/800 MT/s	6-6-6
MT9HTF6472(P)KY-667__	512MB	64 Meg x 72	5.3 GB/s	3.0ns/667 MT/s	5-5-5
MT9HTF6472(P)KY-53E__	512MB	64 Meg x 72	4.3 GB/s	3.75ns/533 MT/s	4-4-4
MT9HTF6472(P)KY-40E__	512MB	64 Meg x 72	3.2 GB/s	5.0ns/400 MT/s	3-3-3

Table 5: Part Numbers and Timing Parameters – 1GB
Base device: MT47H128M8, 1Gb DDR2 SDRAM

Part Number[1]	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Latency (CL - ^{t}RCD - ^{t}RP)
MT9HTF12872(P)KY-80E__	1GB	128 Meg x 72	6.4 GB/s	2.5ns/800 MT/s	5-5-5
MT9HTF12872(P)KY-800__	1GB	128 Meg x 72	6.4 GB/s	2.5ns/800 MT/s	6-6-6
MT9HTF12872(P)KY-667__	1GB	128 Meg x 72	5.3 GB/s	3.0ns/667 MT/s	5-5-5
MT9HTF12872(P)KY-53E__	1GB	128 Meg x 72	4.3 GB/s	3.75ns/533 MT/s	4-4-4
MT9HTF12872(P)KY-40E__	1GB	128 Meg x 72	3.2 GB/s	5.0ns/400 MT/s	3-3-3

Notes:
1. All part numbers end with a two-place code (not shown), designating component and PCB revisions. Consult factory for current revision codes. Example: MT9HTF6472KY-40EC2.
2. For component data sheets, refer to Micron's web site at www.micron.com/products/dram/ddr2.

Pin Assignments and Descriptions

Table 6: Pin Assignments

244-Pin MiniDIMM Front							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	VREF	32	VSS	63	VDDQ	94	DQS5#
2	VSS	33	DQ24	64	A2	95	DQS5
3	DQ0	34	DQ25	65	VDD	96	VSS
4	DQ1	35	VSS	66	VSS	97	DQ42
5	VSS	36	DQS3#	67	VSS	98	DQ43
6	DQS0#	37	DQS3	68	PAR_IN	99	VSS
7	DQS0	38	VSS	69	VDD	100	DQ48
8	VSS	39	DQ26	70	A10/AP	101	DQ49
9	DQ2	40	DQ27	71	BA0	102	VSS
10	DQ3	41	VSS	72	VDD	103	SA2
11	VSS	42	CB0	73	WE#	104	NC (Test)
12	DQ8	43	CB1	74	VDDQ	105	VSS
13	DQ9	44	VSS	75	CAS#	106	DQS6#
14	VSS	45	DQS8#	76	VDDQ	107	DQS6
15	DQS1#	46	DQS8	77	NC	108	VSS
16	DQS1	47	VSS	78	NC	109	DQ50
17	VSS	48	CB2	79	VDDQ	110	DQ51
18	RESET#	49	CB3	80	NC	111	VSS
19	NC	50	VSS	81	VSS	112	DQ56
20	VSS	51	NC	82	DQ32	113	DQ57
21	DQ10	52	VDDQ	83	DQ33	114	VSS
22	DQ11	53	CKE0	84	VSS	115	DQS7#
23	VSS	54	VDD	85	DQS4#	116	DQS7
24	DQ16	55	NC/BA2	86	DQS4	117	VSS
25	DQ17	56	ERR_OUT	87	VSS	118	DQ58
26	VSS	57	VDDQ	88	DQ34	119	DQ59
27	DQS2#	58	A11	89	DQ35	120	VSS
28	DQS2	59	A7	90	VSS	121	SA0
29	VSS	60	VDD	91	DQ40	122	SA1
30	DQ18	61	A5	92	DQ41		
31	DQ19	62	A4	93	VSS		

244-Pin MiniDIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
123	VSS	154	DQ28	185	A3	216	NC/ RDQS#5
124	DQ4	155	DQ29	186	A1	217	VSS
125	DQ5	156	VSS	187	VDD	218	DQ46
126	VSS	157	DM3/ RDQS3	188	CK0	219	DQ47
127	DM0/ RDQS0	158	NC/ RDQS#3	189	CK0#	220	VSS
128	NC/ RDQS#0	159	VSS	190	VDD	221	DQ52
129	VSS	160	DQ30	191	A0	222	DQ53
130	DQ6	161	DQ31	192	BA1	223	VSS
131	DQ7	162	VSS	193	VDD	224	RFU
132	VSS	163	CB4	194	RAS#	225	RFU
133	DQ12	164	CB5	195	VDDQ	226	VSS
134	DQ13	165	VSS	196	S0#	227	DM6/ RDQS6
135	VSS	166	DM8/ RDQS8	197	VDDQ	228	NC/ RDQS#6
136	DM1/ RDQS1	167	NC/ RDQS#8	198	ODT0	229	VSS
137	NC/ RDQS#1	168	VSS	199	NC/A13	230	DQ54
138	VSS	169	CB6	200	VDD	231	DQ55
139	RFU	170	CB7	201	NC	232	VSS
140	RFU	171	VSS	202	VSS	233	DQ60
141	VSS	172	NC	203	DQ36	234	DQ61
142	DQ14	173	VDDQ	204	DQ37	235	VSS
143	DQ15	174	NC/CKE1	205	VSS	236	DM7/ RDQS7
144	VSS	175	VDD	206	DM4/ RDQS4	237	NC/ RDQS#7
145	DQ20	176	NC	207	NC/ RDQS#4	238	VSS
146	DQ21	177	NC	208	VSS	239	DQ62
147	VSS	178	VDDQ	209	DQ38	240	DQ63
148	DM2/ RDQS2	179	A12	210	DQ39	241	VSS
149	NC/ RDQS#2	180	A9	211	VSS	242	SDA
150	VSS	181	VDD	212	DQ44	243	SCL
151	DQ22	182	A8	213	DQ45	244	VDDSPD
152	DQ23	183	A6	214	VSS		
153	VSS	184	VDDQ	215	DM5/ RDQS5		

Notes: 1. Pin 55 is NC for 256MB and 512MB, and BA2 for 1GB.
2. Pin 199 is NC for 256MB, and A13 for 512MB and 1GB.

Table 7: Pin Descriptions

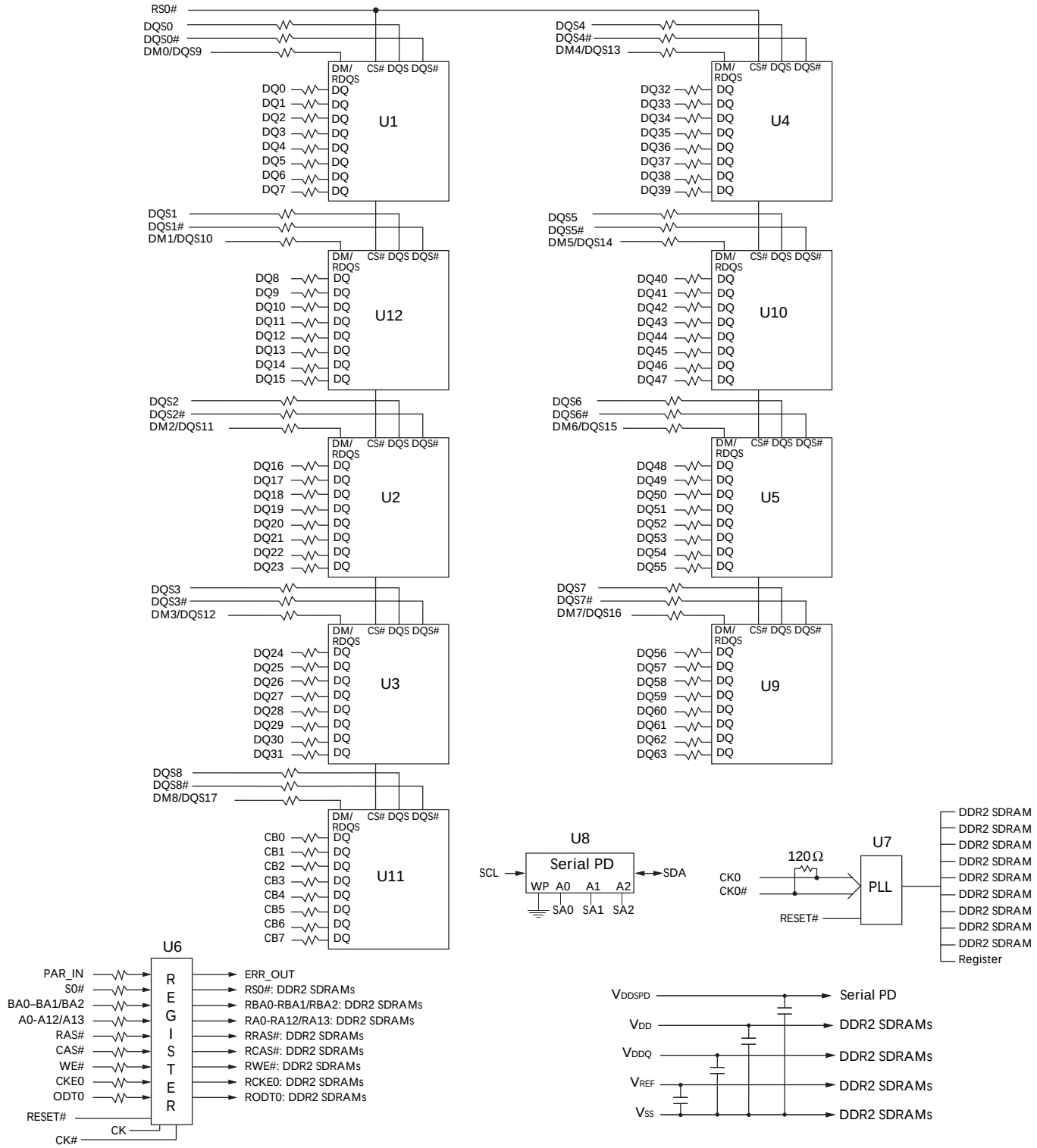
Symbol	Type	Description
ODT0	Input	**On-Die termination**: ODT (registered HIGH) enables termination resistance internal to the DDR2 SDRAM. When enabled, ODT is only applied to each of the following pins: DQ, DQS, DQS#, RDQS, RDQS#, CB, and DM. The ODT input will be ignored if disabled via the LOAD MODE (LM) command.
CK0, CK0#	Input	**Clock**: CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK#. Output data (DQs and DQS/DQS#) is referenced to the crossings of CK and CK#.
CKE0	Input	**Clock enable**: CKE (registered HIGH) activates and CKE (registered LOW) deactivates clocking circuitry on the DDR2 SDRAM. The specific circuitry that is enabled/disabled is dependent on the DDR2 SDRAM configuration and operating mode. CKE LOW provides PRECHARGE power-down and SELF REFRESH operations (all device banks idle), or ACTIVE power-down (row ACTIVE in any device bank). CKE is synchronous for power-down entry, power-down exit, output disable, and for SELF REFRESH entry. CKE is asynchronous for SELF REFRESH exit. Input buffers (excluding CK, CK#, CKE, and ODT) are disabled during power-down. Input buffers (excluding CKE) are disabled during SELF REFRESH. CKE is an SSTL_18 input but will detect a LVCMOS LOW level once V_{DD} is applied during first power-up. After Vref has become stable during the power on and initialization sequence, it must be maintained for proper operation of the CKE receiver. For proper SELF-REFRESH operation V_{REF} must be maintained to this input.
S0#	Input	**Chip select**: S# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when S# is registered HIGH. S# provides for external rank selection on systems with multiple ranks. S# is considered part of the command code.
RAS#, CAS#, WE#	Input	**Command inputs**: RAS#, CAS#, and WE# (along with S#) define the command being entered.
BA0, BA1 (256MB, 512MB) BA0–BA2 (1GB)	Input	**Bank address inputs**: BA0–BA1/BA2 define to which device bank an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA0–BA1/BA2 define which mode register including MR, EMR, EMR(2), and EMR(3) is loaded during the LM command.
A0–A12 (256MB) A0–A13 (512MB, 1GB)	Input	**Address inputs**: Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for Read/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one device bank (A10 LOW, device bank selected by BA0–BA1/BA2) or all device banks (A10 HIGH). The address inputs also provide the op-code during a LM command.
PAR_IN	Input	Parity bit for the address and control bus.
SCL	Input	**Serial clock for presence-detect**: SCL is used to synchronize the presence-detect data transfer to and from the module.
SA0–SA2	Input	**Presence-Detect address inputs**: These pins are used to configure the presence-detect device.
RESET#	Input	Asynchronously forces all registered outputs LOW when RESET# is LOW. This signal can be used during power up to ensure that CKE is LOW and DQs are High-Z.
DQ0–DQ63	I/O	**Data Input/output**: Bidirectional data bus.
DQS0–DQS8, RDQS0#–RDQS8#	I/O	**Data strobe:** Output with read data, input with write data for source synchronous operation. Edge-aligned with read data, center aligned with write data. DQS# is only used when differential data strobe mode is enabled via the LM command. DQS9#–DQS17# are only used when RDQS# is enabled via the LM command.
DM0–DM8	I/O	**Input data mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. Although DM pins are input-only, the DM loading is designed to match that of DQ and DQS pins. If RDQS is enabled, DQS9#–DQS17# are used only during the READ command. If RDQS is disabled, DQS0–DQS17 become DM0–DM8 and DQS9#–DQS17# are not used.
CB0–CB7	I/O	Check bits.

Table 7: Pin Descriptions (Continued)

Symbol	Type	Description
SDA	I/O	**Serial presence-detect data**: SDA is a bidirectional pin used to transfer addresses and data into and out of the presence-detect portion of the module.
ERR_OUT	Output	Parity error found on the address and control bus.
VDD	Supply	Power supply: 1.8V ±0.1V.
VDDQ	Supply	DQ power supply: 1.8V ±0.1V.
VREF	Supply	SSTL_18 reference voltage.
VSS	Supply	Ground.
VDDSPD	Supply	**Serial EEPROM positive power supply**: +1.7V to +3.6V.

Functional Block Diagram

Figure 9: Functional Block Diagram



Notes: 1. Unless otherwise noted, resistor values are 22Ω.

General Description

The MT9HTF3272(P)K, MT9HTF6472(P)K, and MT9HTF12872(P)K DDR2 SDRAM modules are high-speed, CMOS, dynamic random-access 256MB, 512MB, and 1GB memory modules organized in x72 configuration. DDR2 SDRAM modules use internally configured quad-bank (256Mb, 512Mb) or eight-bank (1Gb) DDR2 SDRAM devices.

DDR2 SDRAM modules use double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a 4*n*-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR2 SDRAM module effectively consists of a single 4*n*-bit-wide, one-clock-cycle data transfer at the internal DRAM core and four corresponding *n*-bit-wide, one-half-clock-cycle data transfers at the I/O pins.

A bidirectional data strobe (DQS, DQS#) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the DDR2 SDRAM device during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs.

DDR2 SDRAM modules operate from a differential clock (CK and CK#); the crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK. Commands (address and control signals) are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

PLL and Register Operation

DDR2 SDRAM modules operate in registered mode, where the command/address input signals are latched in the registers on the rising clock edge and sent to the DDR2 SDRAM devices on the following rising clock edge (data access is delayed by one clock cycle). A phase-lock loop (PLL) on the module receives and redrives the differential clock signals (CK, CK#) to the DDR2 SDRAM devices. The registers and PLL minimize system and clock loading. Registered mode will add one clock cycle to CL.

Serial Presence-Detect Operation

DDR2 SDRAM modules incorporate serial presence-detect (SPD). The SPD function is implemented using a 2,048-bit EEPROM. This nonvolatile storage device contains 256 bytes. The first 128 bytes can be programmed by Micron to identify the module type and various SDRAM organizations and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device occur via a standard I^2C bus using the DIMM's SCL (clock) and SDA (data) signals, together with SA (2:0), which provide eight unique DIMM/EEPROM addresses. Write protect (WP) is tied to ground on the module, permanently disabling hardware write protect.

Electrical Specifications

Stresses greater than those listed in Table 8 may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 8: Absolute Maximum DC Ratings

Symbol	Parameter		Min	Max	Units
V_{DD}	V_{DD} supply voltage relative to V_{SS}		–1.0	+2.3	V
V_{DDQ}	V_{DDQ} supply voltage relative to V_{SS}		–0.5	+2.3	V
V_{DDL}	V_{DDL} supply voltage relative to V_{SS}		–0.5	+2.3	V
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}		–0.5	+2.3	V
T_{STG}	Storage temperature		–55	+100	°C
T_{CASE}	DDR2 SDRAM device operating temperature		0	+85	°C
T_{OPR}	Operating temperature		0	+55	°C
I_I	Input leakage current; Any input 0V ≤ V_{IN} ≤ V_{DD}; V_{REF} input 0V ≤ V_{IN} ≤0.95V; (All other pins not under test = 0V)	Command/Address, RAS#, CAS#, WE# S#, CKE, ODT, DM	–5	+5	µA
		CK, CK#	–10	+10	
I_{OZ}	Output leakage current; 0V ≤ V_{OUT} ≤ V_{DDQ}; DQs and ODT are disabled	DQ, DQS, DQS#	–5	+5	µA
I_{VREF}	V_{REF} leakage current; V_{REF} = Valid V_{REF} level		–18	+18	µA

Capacitance

At DDR2 data rates, Micron encourages designers to simulate the performance of the module to achieve optimum values. When inductance and delay parameters associated with trace lengths are used in simulations, they are significantly more accurate and realistic than a gross estimation of module capacitance. Simulations can then render a considerably more accurate result. JEDEC modules are now designed by using simulations to close timing budgets.

Table 9: IDD Specifications and Conditions – 256MB
Values shown for DDR2 SDRAM components only

Parameter/Condition		Symbol	-667	-53E	-40E	Units
Operating one bank active-precharge current; tCK = tCK (IDD), tRC = tRC (IDD), tRAS = tRAS MIN (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		IDD0	810	720	675	mA
Operating one bank active-read-precharge current; IOUT = 0mA; BL = 4, CL = CL (IDD), AL = 0; tCK = tCK (IDD), tRC = tRC (IDD), tRAS = tRAS MIN (IDD), tRCD = tRCD (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data pattern is same as IDD4W		IDD1	900	810	765	mA
Precharge power-down current; All device banks idle; tCK = tCK (IDD); CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating		IDD2P	45	45	45	mA
Precharge quiet standby current; All device banks idle; tCK = tCK (IDD); CKE is HIGH, S# is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are floating		IDD2Q	360	315	225	mA
Precharge standby current; All device banks idle; tCK = tCK (IDD); CKE is HIGH, S# is HIGH; Other control and address bus inputs are switching; Data bus inputs are switching		IDD2N	360	315	270	mA
Active power-down current; All device banks open; tCK = tCK (IDD); CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating	Fast PDN Exit MR[12] = 0	IDD3P	270	225	180	mA
	Slow PDN Exit MR[12] = 1		54	54	54	mA
Active standby current; All device banks open; tCK = tCK (IDD), tRAS = tRAS MAX (IDD), tRP = tRP (IDD); CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching		IDD3N	450	360	270	mA
Operating burst write current; All device banks open, continuous burst writes; BL = 4, CL = CL (IDD), AL = 0; tCK = tCK (IDD), tRAS = tRAS MAX (IDD), tRP = tRP (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		IDD4W	1,710	1,440	1,125	mA
Operating burst read current; All device banks open, continuous burst reads, IOUT = 0mA; BL = 4, CL = CL (IDD), AL = 0; tCK = tCK (IDD), tRAS = tRAS MAX (IDD), tRP = tRP (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		IDD4R	1,620	1,350	1,035	mA
Burst refresh current; tCK = tCK (IDD); REFRESH command at every tRFC (IDD) interval; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching		IDD5	1,620	1,530	1,485	mA
Self refresh current; CK and CK# at 0V; CKE ≤ 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are floating		IDD6	45	45	45	mA
Operating bank interleave read current; All device banks interleaving reads, IOUT= 0mA; BL = 4, CL = CL (IDD), AL = tRCD (IDD) -1 × tCK (IDD); tCK = tCK (IDD), tRC = tRC (IDD), tRRD = tRRD (IDD), tRCD = tRCD (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are stable during deselects; Data bus inputs are switching; See IDD7 Conditions for detail		IDD7	2250	2,160	2,070	mA

Table 10: IDD Specifications and Conditions – 512MB
Values shown for DDR2 SDRAM components only

Parameter/Condition		Symbol	-80E/-800	-667	-53E	-40E	Units
Operating one bank active-precharge current; tCK = tCK (IDD), tRC = tRC (IDD), tRAS = tRAS MIN (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		IDD0	900	810	720	720	mA
Operating one bank active-read-precharge current; IOUT = 0mA; BL = 4, CL = CL (IDD), AL = 0; tCK = tCK (IDD), tRC = tRC (IDD), tRAS = tRAS MIN (IDD), tRCD = tRCD (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data pattern is same as IDD4W		IDD1	1,035	945	855	810	mA
Precharge power-down current; All device banks idle; tCK = tCK (IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are floating		IDD2P	63	63	63	63	mA
Precharge quiet standby current; All device banks idle; tCK = tCK (IDD); CKE is HIGH, S# is HIGH; Other control and address bus inputs are stable; Data bus inputs are floating		IDD2Q	450	405	360	315	mA
Precharge standby current; All device banks idle; tCK = tCK (IDD); CKE is HIGH, S# is HIGH; Other control and address bus inputs are switching; Data bus inputs are switching		IDD2N	495	450	405	360	mA
Active power-down current; All device banks open; tCK = tCK (IDD); CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating	Fast PDN Exit MR[12] = 0	IDD3P	360	315	270	225	mA
	Slow PDN Exit MR[12] = 1		108	108	108	108	mA
Active standby current; All device banks open; tCK = tCK (IDD), tRAS = tRAS MAX (IDD), tRP = tRP (IDD); CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching		IDD3N	630	585	495	405	mA
Operating burst write current; All device banks open, continuous burst writes; BL = 4, CL = CL (IDD), AL = 0; tCK = tCK (IDD), tRAS = tRAS MAX (IDD), tRP = tRP (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		IDD4W	1,755	1,530	1,260	1,035	mA
Operating burst read current; All device banks open, Continuous burst reads, IOUT = 0mA; BL = 4, CL = CL (IDD), AL = 0; tCK = tCK (IDD), tRAS = tRAS MAX (IDD), tRP = tRP (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		IDD4R	1,845	1,620	1,305	1,035	mA
Burst refresh current; tCK = tCK (IDD); REFRESH command at every tRFC (IDD) interval; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching		IDD5	2,070	1,620	1,530	1,485	mA
Self refresh current; CK and CK# at 0V; CKE ≤ 0.2V; Other control and address bus inputs are floating; Data bus inputs are floating		IDD6	63	63	63	63	mA
Operating bank interleave read current; All device banks interleaving reads, IOUT = 0mA; BL = 4, CL = CL (IDD), AL = tRCD (IDD) - 1 × tCK (IDD); tCK = tCK (IDD), tRC = tRC (IDD), tRRD = tRRD (IDD), tRCD = tRCD (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are stable during deselects; Data bus inputs are switching; See IDD7 Conditions for detail		IDD7	2,700	2,160	2,025	1,980	mA

Table 11: IDD Specifications and Conditions – 1GB
Values shown for DDR2 SDRAM components only

Parameter/Condition		Symbol	-80E/-800	-667	-53E	-40E	Units
Operating one bank active-precharge current; tCK = tCK (IDD), tRC = tRC (IDD), tRAS = tRAS MIN (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		IDD0	810	765	630	630	mA
Operating one bank active-read-precharge current; IOUT = 0mA; BL = 4, CL = CL (IDD), AL = 0; tCK = tCK (IDD), tRC = tRC (IDD), tRAS = tRAS MIN (IDD), tRCD = tRCD (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data pattern is same as IDD4W		IDD1	990	900	855	810	mA
Precharge power-down current; All device banks idle; tCK = tCK (IDD); CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating		IDD2P	63	63	63	63	mA
Precharge quiet standby current; All device banks idle; tCK = tCK (IDD); CKE is HIGH, S# is HIGH; Other control and address bus inputs are stable; Data bus inputs are floating		IDD2Q	450	360	360	315	mA
Precharge standby current; All device banks idle; tCK = tCK (IDD); CKE is HIGH, S# is HIGH; Other control and address bus inputs are switching; Data bus inputs are switching		IDD2N	450	360	360	315	mA
Active power-down current; All device banks open; tCK = tCK (IDD); CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating	Fast PDN Exit MR[12] = 0	IDD3P	360	270	270	270	mA
	Slow PDN Exit MR[12] = 1		90	90	90	90	mA
Active standby current; All device banks open; tCK = tCK (IDD), tRAS = tRAS MAX (IDD), tRP = tRP (IDD); CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching		IDD3N	540	495	405	360	mA
Operating burst write current; All device banks open, continuous burst writes; BL = 4, CL = CL (IDD), AL = 0; tCK = tCK (IDD), tRAS = tRAS MAX (IDD), tRP = tRP (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		IDD4W	1,440	1,215	1,125	945	mA
Operating burst read current; All device banks open, continuous burst reads, IOUT = 0mA; BL = 4, CL = CL (IDD), AL = 0; tCK = tCK (IDD), tRAS = tRAS MAX (IDD), tRP = tRP (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		IDD4R	1,440	1,215	1,125	945	mA
Burst refresh current; tCK = tCK (IDD); REFRESH command at every tRFC (IDD) interval; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching		IDD5	2,115	1,935	1,890	1,845	mA
Self refresh current; CK and CK# at 0V; CKE ≤ 0.2V; Other control and address bus inputs are floating; Data bus inputs are floating		IDD6	63	63	63	63	mA
Operating bank interleave read current; All device banks interleaving reads, IOUT = 0mA; BL = 4, CL = CL (IDD), AL = tRCD (IDD) - 1 × tCK (IDD); tCK = tCK (IDD), tRC = tRC (IDD), tRRD = tRRD (IDD), tRCD = tRCD (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are stable during deselects; Data bus inputs are switching; See IDD7 Conditions for detail		IDD7	3,015	2,520	2,430	2,340	mA

AC Operating Specifications

Recommended AC operating conditions are given in the DDR2 component data sheets, available at www.micron.com/products/dram/ddr2. Module speed grades correlate with component speed grades as shown in Figure 12:

Table 12: Module and Component Speed Grade Table

Module Speed Grade	Component Speed Grade
-80E	-25E
-800	-25
-667	-3
-53E	-37E
-40E	-5E

Register and PLL Specifications

Table 13: Register (SSTUB3287A or Equivalent)

Parameter	Symbol	Pins	Condition	Min	Max	Units
DC high-level input voltage	$V_{IH(DC)}$	Address, Control, Command	SSTL_18	$V_{REF(DC)}$ +125	V_{DDQ} + 250	mV
DC low-level input voltage	$V_{IL(DC)}$	Address, Control, Command	SSTL_18	0	$V_{REF(DC)}$ - 125	mV
AC high-level input voltage	$V_{IH(AC)}$	Address, Control, Command	SSTL_18	$V_{REF(DC)}$ + 250	V_{DD}	mV
AC low-level input voltage	$V_{IL(AC)}$	Address, Control, Command	SSTL_18	0	$V_{REF(DC)}$ - 250	mV
Output high voltage	V_{OH}	Parity output	LVCMOS	1.2	–	mV
Output low voltage	V_{OL}	Parity output	LVCMOS	–	0.5	mV
Input current	I_I	All pins	V_I = V_{DDQ} or V_{SSQ}	–5	5	µA
Static standby	I_{DD}	All pins	RESET# = V_{SSQ} (I/O = 0)	–	100	µA
Static operating	I_{DD}	All pins	RESET# = V_{SSQ}; V_I = $V_{IH(AC)}$ or $V_{IL(DC)}$ I/O = 0	–	80mA	µA
Dynamic operating – clock tree	I_{DDD}	N/A	RESET# = V_{DD}, V_I = $V_{IH(AC)}$ or $V_{IL(AC)}$, I0 = 0; CK and CK# switching 50% duty cycle	–	Varies by manufacturer	µA
Dynamic operating (per each input)	I_{DDD}	N/A	RESET# = V_{DD}, V_I = $V_{IH(AC)}$ or $V_{IL(AC)}$, I0 = 0; CK and CK# switching 50% duty cycle; One data input switching at $^tCK/2$, 50% duty cycle	–	Varies by manufacturer	µA
Input capacitance (per device, per pin)	C_I	All inputs except RESET#	V_I = V_{REF} ±250mV; V_{DDQ} = 1.8V	2.5	3.5	pF
Input capacitance (per device, per pin)		RESET#	V_I = V_{DDQ} or V_{SSQ}	–	Varies by manufacturer	pF

PLL

Table 14: PLL (CU877 device or Equivilent JESD82-8.01)

Parameter	Symbol	Pins	Condition	Min	Max	Units
DC high-level input voltage	V_{IH}	RESET#	LVCMOS	0.65 × V_{DD}	–	mV
DC low-level input voltage	V_{IL}	RESET#	LVCMOS	–	0.35 × V_{DD}	mV
Input voltage (limits)	V_{IN}	RESET#, CK, CK#		–0.3	$V_{DD}Q$ + 0.3	mV
DC high-level input voltage	V_{IH}	CK, CK#	Differential input	0.65 × V_{DD}	–	mV
DC low-level input voltage	V_{IL}	CK, CK#	Differential input	–	0.35 × V_{DD}	mV
Input differential-pair cross voltage	V_{IX}	CK, CK#	Differential input	($V_{DD}Q$/2) - 0.15	($V_{DD}Q$/2) + 0.15	V
Input differential voltage	$V_{ID(DC)}$	CK, CK#	Differential input	0.3	$V_{DD}Q$ + 0.4	V
Input differential voltage	$V_{ID(AC)}$	CK, CK#	Differential input	0.6	$V_{DD}Q$ + 0.4	V
Input current	I_I	RESET#	V_I = $V_{DD}Q$ or $V_{SS}Q$	–10	10	µA
		CK, CK#	V_I = $V_{DD}Q$ or $V_{SS}Q$	–250	250	µA
Output disabled current	I_{ODL}		RESET# = $V_{SS}Q$; V_I = $V_{IH(AC)}$ or $V_{IL(DC)}$	100	–	µA
Static supply current	I_{DDLD}		CK = CK# = LOW	–	500	µA
Dynamic supply	I_{DD}	N/A	CK, CK# = 270 MHz, all outputs open (not connected to PCB)	–	300	mA
Input capacitance	C_{IN}	Each input	V_I = $V_{DD}Q$ or $V_{SS}Q$	2	3	pF

Table 15: PLL Clock Driver Timing Requirements and Switching Characteristics
Note: 1

Parameter	Symbol	0°C ≤ T_{OPR} ≤ +55°C, V_{DD} = +1.8V ±0.1V		Units
		Min	Max	
Stabilization time	^tL	–	15	µs
Input clock slew rate	^tLS_I	1.0	4	V/ns
SSC modulation frequency		30	33	KHz
SSC clock input frequency deviation		0.0	–0.50	%
PLL loop bandwidth (-3dB from unity gain)		2.0	–	MHz

Notes:
1. PLL timing and switching specifications are critical for proper operation of the DDR2 DIMM. This is a subset of parameters for the specific PLL used. Detailed PLL information is available in JEDEC Standard JESD82.
2. The output slew rate is determined from the IBIS model:

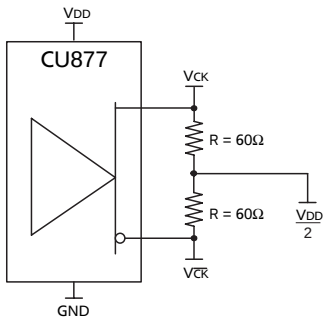


Table 16: Serial Presence-Detect EEPROM DC Operating Conditions

All voltages referenced to V_{SS}; V_{DDSPD} = +1.7V to +3.6V

Parameter/Condition	Symbol	Min	Max	Units
Supply voltage	V_{DDSPD}	1.7	3.6	V
Input high voltage: Logic 1; All inputs	V_{IH}	V_{DDSPD} × 0.7	V_{DDSPD} + 0.5	V
Input low voltage: Logic 0; All inputs	V_{IL}	–0.6	V_{DDSPD} × 0.3	V
Output low voltage: I_{OUT} = 3mA	V_{OL}	–	0.4	V
Input leakage current: V_{IN} = GND to V_{DDSPD}	I_{LI}	0.10	3	µA
Output leakage current: V_{OUT} = GND to V_{DDSPD}	I_{LO}	0.05	3	µA
Standby current:	I_{SB}	1.6	4	µA
Power Supply Current, READ: SCL clock frequency = 100 KHz	I_{CC_R}	0.4	1	mA
Power Supply Current, WRITE: SCL clock frequency = 100 KHz	I_{CC_W}	2	3	mA

Table 17: Serial Presence-Detect EEPROM AC Operating Conditions

All voltages referenced to V_{SS}; V_{DDSPD} = +1.7V to +3.6V

Parameter/Condition	Symbol	Min	Max	Units	Notes
SCL LOW to SDA data-out valid	^tAA	0.2	0.9	µs	1
Time the bus must be free before a new transition can start	^tBUF	1.3		µs	
Data-out hold time	^tDH	200		ns	
SDA and SCL fall time	^tF		300	ns	2
Data-in hold time	$^tHD:DAT$	0		µs	
Start condition hold time	$^tHD:STA$	0.6		µs	
Clock HIGH period	^tHIGH	0.6		µs	
Noise suppression time constant at SCL, SDA inputs	^tI		50	ns	
Clock LOW period	^tLOW	1.3		µs	
SDA and SCL rise time	^tR		0.3	µs	2
SCL clock frequency	^fSCL		400	KHz	
Data-in setup time	$^tSU:DAT$	100		ns	
Start condition setup time	$^tSU:STA$	0.6		µs	3
Stop condition setup time	$^tSU:STO$	0.6		µs	
WRITE cycle time	^tWRC		10	ms	4

Notes:
1. To avoid spurious start and stop conditions, a minimum delay is placed between SCL = 1 and the falling or rising edge of SDA.
2. This parameter is sampled.
3. For a restart condition, or following a WRITE cycle.
4. The SPD EEPROM WRITE cycle time (^tWRC) is the time from a valid stop condition of a write sequence to the end of the EEPROM internal ERASE/PROGRAM cycle. During the WRITE cycle, the EEPROM bus interface circuit is disabled, SDA remains HIGH due to pull-up resistor, and the EEPROM does not respond to its slave address.

Table 18: Serial Presence-Detect Matrix

"1"/"0": Serial Data, "driven to HIGH"/"driven to LOW"; table notes located on page 17

Byte	Description	Entry (Version)	MT9HTF3272K/ MT9HTF3272(P)K	MT9HTF6472K/ MT9HTF6472(P)K	MT9HTF12872K/ MT9HTF12872K(P)K
0	Number of SPD bytes used by Micron	128	80	80	80
1	Total number of bytes in SPD device	256	08	08	08
2	Fundamental memory type	DDR2 SDRAM	08	08	08
3	Number of row addresses on assembly	13, 14	0D	0E	0E
4	Number of column addresses on assembly	10	0A	0A	0A
5	DIMM height and module ranks	30mm, single rank	60	60	60
6	Module data width	72	48	48	48
7	Module data width (continued)	0	00	00	00
8	Module voltage interface levels	SSTL 1.8V	05	05	05
9	SDRAM cycle time, ^{t}CK (CL = maximum value, see byte 18)	-80E/-800 -667 -53E -40E	– 30 3D 50	25 30 3D 50	25 30 3D 50
10	SDRAM access from Clock, ^{t}AC (CL = maximum value, see byte 18)	-80E/-800 -667 -53E -40E	– 45 50 60	40 45 50 60	40 45 50 60
11	Module configuration type	ECC ECC and parity	02 06	02 06	02 06
12	Refresh rate/type	7.81µs/SELF	82	82	82
13	SDRAM device width (primary SDRAM)	8	08	08	08
14	Error-checking SDRAM data width	8	08	08	08
15	Minimum clock delay, back-to-back random column access	1 clock	00	00	00
16	Burst lengths supported	4, 8	0C	0C	0C
17	Number of banks on SDRAM device	4 or 8	04	04	08
18	CAS latencies supported	-80E (5, 4) -800 (6, 5) -667 (5, 4, 3) -53E/-40E (4, 3)	– – 38 18	30 60 38 18	60 60 38 18
19	Module thickness		01	01	01
20	DDR2 DIMM type	Registered MiniDIMM	10	10	10
21	SDRAM module attributes		04	04	04
22	SDRAM device attributes: weak driver (01) and 50Ω ODT (03)	-80E/-800/-667 -53E/-40E	–/03 01	03 01	03 01
23	SDRAM cycle time, ^{t}CK, MAX CL - 1	-80E/-667 -800 -53E/-40E	–/3D – 50	3D 30 50	3D 30 50

Table 18: Serial Presence-Detect Matrix

"1"/"0": Serial Data, "driven to HIGH"/"driven to LOW"; table notes located on page 17

Byte	Description	Entry (Version)	MT9HTF3272K/ MT9HTF3272(P)K	MT9HTF6472K/ MT9HTF6472(P)K	MT9HTF12872K/ MT9HTF12872K(P)K
24	SDRAM access from CK, ^{t}AC, MAX CL - 1	-80E/-800 -667 -53E -40E	– 45 50 60	40 45 50 60	40 45 50 60
25	SDRAM cycle time, ^{t}CK, MAX CL - 2	-80E/-800 -667 -53E/-40E(N/A)	– 50 00	00 50 00	00 50 00
26	SDRAM access from CK, ^{t}AC, MAX CL - 2	-80E/-800 -667 -53E/-40E(N/A)	– 45 00	00 45 00	00 45 00
27	Minimum row precharge time, ^{t}RP	-80E -800/-667/-53E/ -40E	– –/3C	32 3C	32 3C
28	Minimum row active-to-row active, ^{t}RRD		1E	1E	1E
29	Minimum RAS#-to-CAS# delay, ^{t}RCD	-80E -800/-667/-53E/ -40E	– –/3C	32 3C	32 3C
30	Minimum RAS# pulse width, ^{t}RAS	-80E/-800/ -667/-53E -40E	2D 2D 28	2D 2D 28	2D 2D 28
31	Module rank density	256MB, 512MB 1GB	40	80	01
32	Address and command setup time, $^{t}IS_{b}$	-80E/-800 -667 -53E -40E	– 20 25 35	17 20 25 35	17 20 25 35
33	Address and command hold time, $^{t}IH_{b}$	-80E/-800 -667 -53E -40E	– 27 37 47	25 27 37 47	25 27 37 47
34	Data/ Data mask input setup time, $^{t}DS_{b}$	-80E/-800 -667/-53E -40E	– 10 15	5 10 15	5 10 15
35	Data/ Data mask input hold time, $^{t}DH_{b}$	-80E/-800 -667 -53E -40E	– 17 22 27	12 17 22 27	12 35 22 27
36	Write recovery time, ^{t}WR		3C	3C	3C
37	WRITE-to-READ command delay, ^{t}WTR	-80E -800/-40E -667/-53E	– 28 1E	1E 28 1E	28 28 1E
38	READ-to-PRECHARGE command delay, ^{t}RTP		1E	1E	1E
39	Memory analysis probe		00	00	00
40	Extension for bytes 41 and 42	-80E -800 -667/-53E/-40E	– – 00	30 00 00	06 06 06

Table 18: Serial Presence-Detect Matrix

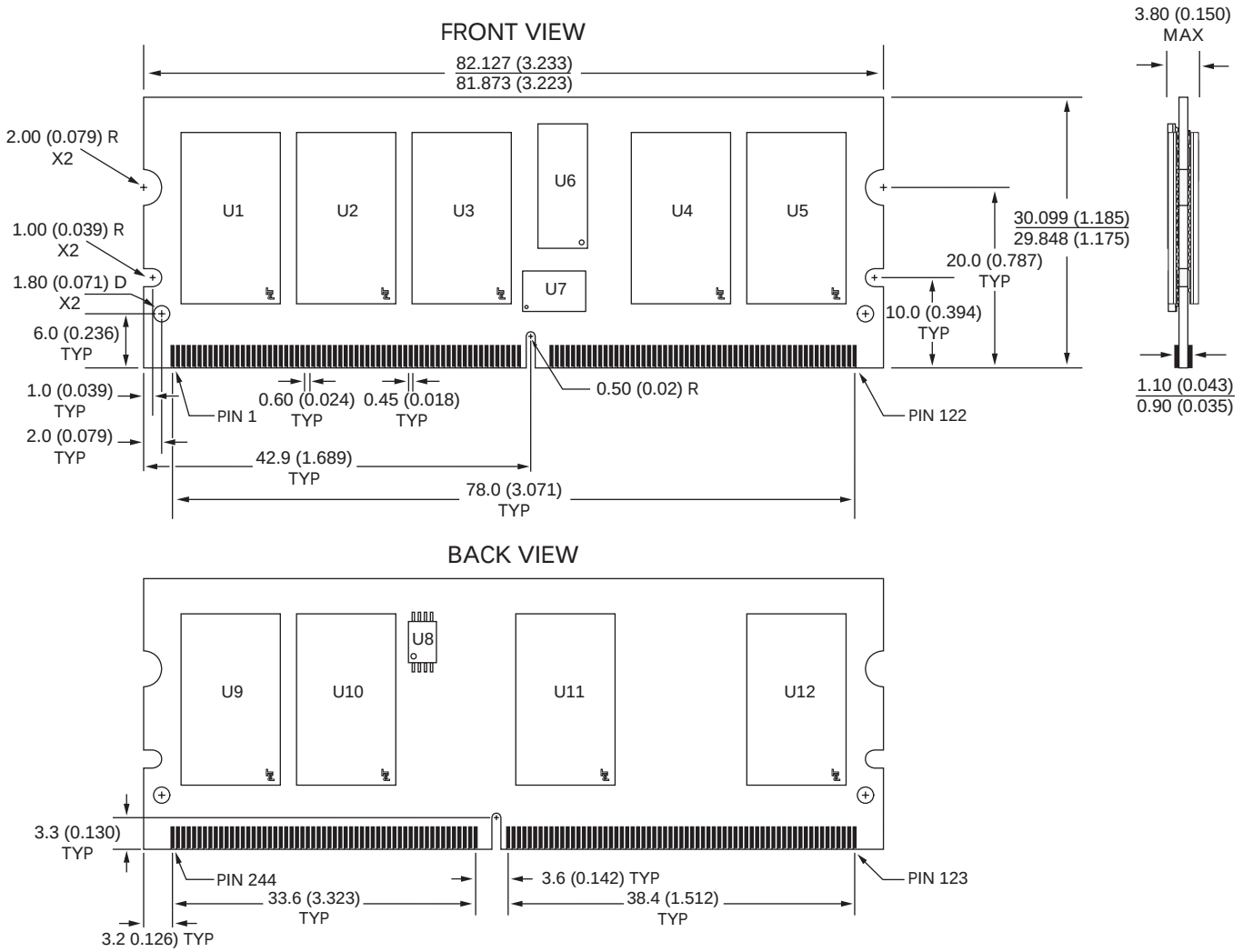
"1"/"0": Serial Data, "driven to HIGH"/"driven to LOW"; table notes located on page 17

Byte	Description	Entry (Version)	MT9HTF3272K/ MT9HTF3272(P)K	MT9HTF6472K/ MT9HTF6472(P)K	MT9HTF12872K/ MT9HTF12872K(P)K
41	MIN active auto refresh time, ^{t}RC (see note 1)	-80E -800/-667/-53E -40E	39 3C 37	39 3C 37	3C 3C 37
42	Minimum AUTO REFRESH to ACTIVE/AUTO REFRESH command period, ^{t}RFC		4B	69	7F
43	SDRAM device MAX cycle time, ^{t}CK (MAX)		80	80	80
44	SDRAM device MAX DQS–DQ skew time, ^{t}DQSQ	-80E/-800 -667 -53E -40E	– 18 1E 23	14 18 1E 23	14 18 1E 23
45	SDRAM device MAX read data hold skew factor, ^{t}QHS	-80E/-800 -667 -53E -40E	– 22 28 2D	1E 22 28 2D	1E 22 28 2D
46	PLL relock time		0F	0F	0F
47–61	Optional features, not supported		00	00	00
62	SPD revision	Release 1.2	12	12	12
63	Checksum for bytes 0–62 ECC/ECC and parity	-80E -800 -667 -53E -40E	– – 1F/23 CA/CE 31/35	C6 DA 7E/82 29/2D 90/94	7B 7B 1F/23 CA/CE 31/35
64	Manufacturer's JEDEC ID code	MICRON	2C	2C	2C
65–71	Manufacturer's JEDEC ID code	(Continued)	FF	FF	FF
72	Manufacturing location	01–12	01–0C	01–0C	01–0C
73–90	Module part number (ASCII)		Variable data	Variable data	Variable data
91	PCB identification code	1–9	01–09	01–09	01–09
92	Identification code (continued)	0	00	00	00
93	Year of manufacture in BCD		Variable data	Variable data	Variable data
94	Week of manufacture in BCD		Variable data	Variable data	Variable data
95–98	Module serial number		Variable data	Variable data	Variable data
99–127	Manufacturer-specific data (RSVD)		00	00	00
128–255	Customer reserved		FF	FF	FF

Notes: 1. The ^{t}RC SPD values shown are JEDEC DDR2 device specification values. The actual Micron DDR2 device specification is ^{t}RC = 55nsfor all speed grades.

Module Dimensions

Figure 10: 244-pin DIMM DDR2 Module Dimensions



Notes:
1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.
2. The dimensional diagram is for reference only. Refer to the MO document for complete design dimensions.

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