NB3M8T3910G

2.5V/3.3V 3:1:10 Configurable Differential Clock Fanout Buffer with LVCMOS Reference Output

ON Semiconductor®

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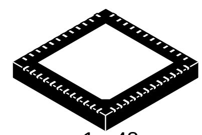
Description

The NB3M8T3910G is a 3:1:10 Clock fanout buffer operating on a 2.5 V/3.3 V Core V_{DD} and a flexible 2.5 V / 3.3 V V_{DDO} supply ($V_{DDO} \le V_{DD}$).

A 3:1 MUX selects between Crystal oscillator inputs, or either of two differential Clock inputs capable of accepting LVPECL, LVDS, HCSL, or SSTL levels. The MUX select lines, SEL0 and SEL1, accept LVCMOS or LVTTL levels and select input per Table 3. The Crystal input is disabled when a Clock input is selected.

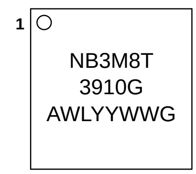
Differential Outputs consist of two banks of five differential outputs with each bank independently mode configurable as LVPECL, LVDS or HCSL. Each bank of differential output pairs is configured with a pair of SMODEAx/Bx select lines using LVCMOS or LVTTL levels per Table 6. Clock input levels and outputs states are determined per Table 5.

The Single−Ended LVCMOS Output, REFOUT, is synchronously enabled by the OE_SE control line per Table 4 using LVCMOS / LVTTL levels. For Clock frequencies above 250 MHz, the REFOUT line should be disabled.



QFN48
G SUFFIX
CASE 485AJ

MARKING DIAGRAM



A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
G	= Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information on page 19 of this data sheet.

Features

- Crystal, Single−Ended or Differential Input Reference Clocks
- Differential Input Pair can Accept: LVPECL, LVDS, HCSL, SSTL
- Two Output Banks: Each has Five Differential Outputs Configurable as LVPECL, LVDS, or HCSL by SMODEAx/Bx Pins
- One Single−Ended LVCMOS Output with Synchronous OE Control
- LVCMOS/LVTTL Interface Levels for all Control Inputs
- Clock Frequency: Up to 1400 MHz, Typical
- Output Skew: 50 ps (Max)
- Additive RMS Jitter <0.03 ps (156.25 MHz, Typical)
- Input to Output Propagation Delay (900 ps Typical)
- Operating Supply Modes V_{DD}/V_{DDO}: 2.5 V/2.5 V, 3.3 V/3.3 V or 3.3 V/2.5 V
- Industrial Temperature Range −40°C to 85°C
- This is a Pb−Free Device

Applications

- Clock Distribution
- Telecom
- Networking
- Backplane
- High End Computing
- Wireless and Wired Infrastructure

End Products

- Servers
- Ethernet Switch/Routers
- ATE
- Test and Measurement

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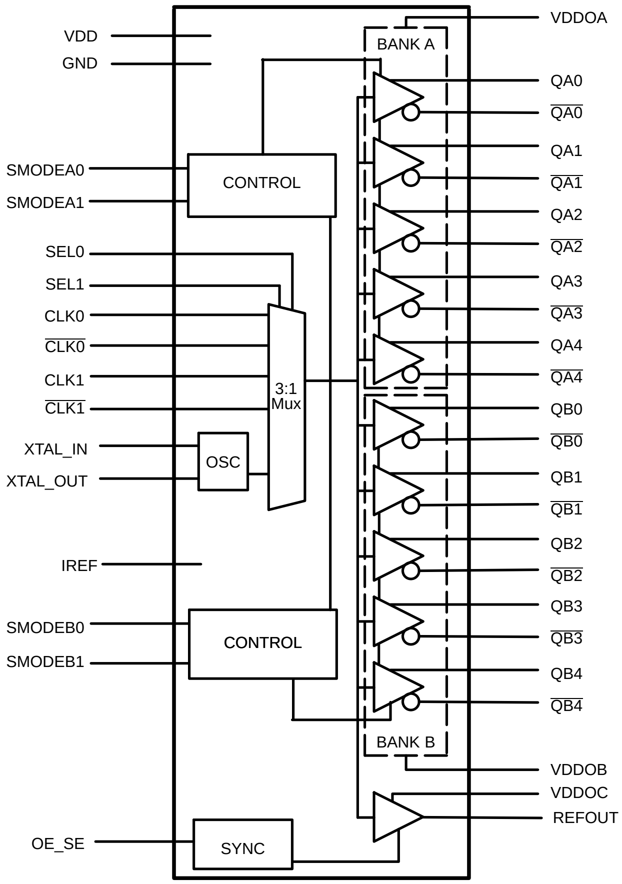


Figure 1. Simplified Logic Diagram

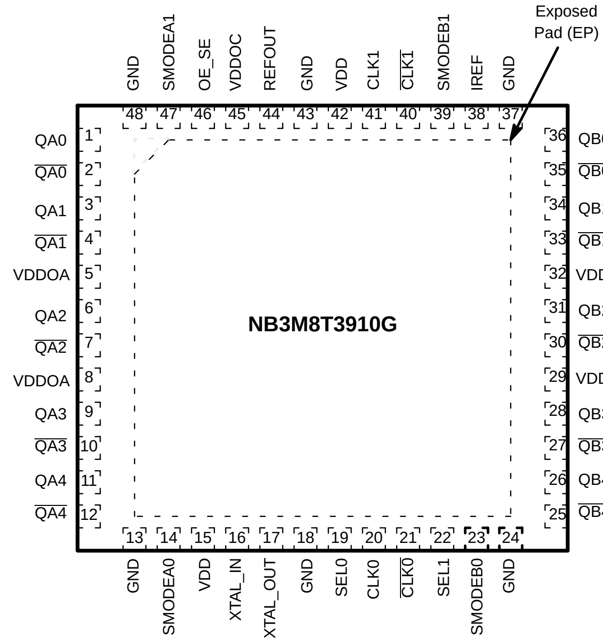


Figure 2. QFN−48 Pinout Configuration (Top View)

Table 1. PIN DESCRIPTION

Number	Name	Type	Default (Internal Resistors)	Description
1, 2	QA0, $\overline{QA0}$	Output		Bank A differential output pair Q0. Configurable as LVPECL / LVDS / HCSL
3, 4	QA1, $\overline{QA1}$	Output		Bank A differential output pair Q1. Configurable as LVPECL / LVDS / HCSL
5, 8	VDDOA	Power		VDDOA Positive Supply pin for Bank A outputs. VDDOA pins must all be externally connected to a power supply to guarantee proper operation. Bypass with 0.01 μF cap to GND
29, 32	VDDOB	Power		VDDOB Positive Supply pin for Bank B outputs. VDDOB pins must all be externally connected to a power supply to guarantee proper operation. Bypass with 0.01 μF cap to GND
45	VDDOC	Power		VDDOC Positive Supply pin for REFOUT output. VDDOC pin must be externally connected to a power supply to guarantee proper operation. Bypass with 0.01 μF cap to GND
6,7	QA2, $\overline{QA2}$	Output		Bank A differential output pair Q2. Configurable as LVPECL / LVDS / HCSL.
9,10	QA3, $\overline{QA3}$	Output		Bank A differential output pair Q3. Configurable as LVPECL / LVDS / HCSL
11,12	QA4, $\overline{QA4}$	Output		Bank A differential output pair Q4. Configurable as LVPECL / LVDS / HCSL
13, 18, 24, 37, 43, 48	GND	Power		Ground Supply. All GND pins must be externally connected to power supply to guarantee proper operation.
14, 47	SMODEA0 / SMODEA1	Input	Pulldown	Output driver selectors for BANK A. See Table 6 for function. LVCMOS/LVTTL levels.

Table 1. PIN DESCRIPTION

Number	Name	Type	Default (Internal Resistors)	Description
15, 42	VDD	Power		VDD Positive Supply pin for core logic. VDD pins must all be externally connected to a power supply to guarantee proper operation. Bypass with 0.01 μF cap to GND.
16, 17	XTAL_IN, XTAL_OUT	Input		Crystal input / output. XTAL_IN can also be driven by X0, TCX0 or other external single−ended clock.
19, 22	SEL0 SEL1	Input	Pulldown	Input clock selectors. See Table 3 for function. LVCMOS/LVTTL interface levels.
20	CLK0	Input	Pulldown	Non−inverting clock input 0. LVPECL, LVDS, SSTL, HCSL levels.
21	$\overline{\text{CLK0}}$	Input	Pullup / Pulldown	Inverting differential clock input 0. LVPECL, LVDS, SSTL, HCSL, LVCMOS levels. Internal bias to $V_{DD} \div 2$.
23, 39	SMODEB0 / SMODEB1	Input	Pulldown	Output driver selects for BANK B. See Table 6 for function. LVCMOS/LVTTL levels.
25,26	$\overline{\text{QB4}}$, QB4	Output		Bank B differential output pair Q4. Configurable as LVPECL / LVDS / HCSL
27,28	$\overline{\text{QB3}}$, QB3	Output		Bank B differential output pair Q3. Configurable as LVPECL / LVDS / HCSL.
30,31	$\overline{\text{QB2}}$, QB2	Output		Bank B differential output pair Q2. Configurable as LVPECL / LVDS / HCSL.
33,34	$\overline{\text{QB1}}$, QB1	Output		Bank B differential output pair Q1. Configurable as LVPECL / LVDS / HCSL.
35,36	$\overline{\text{QB0}}$, QB0	Output		Bank B differential output pair Q0. Configurable as LVPECL / LVDS / HCSL.
38	IREF	Output		Connect a fixed 475 Ω precision resistor from this pin to ground to provide the output reference current. Required for HCSL, not used for LVPECL or LVDS.
40	$\overline{\text{CLK1}}$	Input	Pullup / Pulldown	Inverting differential clock input 1. LVPECL, LVDS, SSTL, HCSL levels internal bias to $V_{DD}/2$. Internal bias to $V_{DD} \div 2$.
41	CLK1	Input	Pulldown	Non−inverting differential clock input 1. LVPECL, LVDS, SSTL, HCSL, LVCMOS levels.
44	REFOUT	Output		Reference output, LVCMOS.
46	OE_SE	Input	Pulldown	Synchronous Enable Control for REFOUT. LVCMOS/LVTTL levels.
EP	EXPOSED PAD	Thermal		The Exposed Pad (EP) on the QFN−48 package bottom is thermally connected to the die for improved heat transfer out of package. The exposed pad must be attached to a heat−sinking conduit. The pad is electrically connected to the die, and must be electrically connected to GND.

Table 2. PIN CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Unit
CIN	Input Capacitance		4		pF
RPU/RPD	Input Pullup/Pulldown Resistor		50		kΩ

FUNCTION TABLES

Table 3. SELx INPUT SELECT TABLE

SEL[1:0] Inputs	Selected Input
00	CLK0/$\overline{CLK0}$
01	CLK1/$\overline{CLK1}$
10	XTAL
11	XTAL

Table 4. OE_SE OUTPUT CONTROL TABLE FOR REFOUT

OE_SE Input Level	REFOUT Status
Low	High Impedance
High	Enabled

Table 5. DIFF CLK INPUT / OUTPUT TABLE (Diff or S.E. stimulus)

Input State	Output State
CLKx = LOW, $\overline{CLKx}$ = HIGH	Qx = LOW, $\overline{Qx}$ = HIGH
CLKx = HIGH, $\overline{CLKx}$ = LOW	Qx = HIGH, $\overline{Qx}$ = LOW
CLKx = Open; $\overline{CLKx}$ = Open	Qx = LOW, $\overline{Qx}$ = HIGH
CLKx = LOW; $\overline{CLKx}$ = LOW	Qx = LOW, $\overline{Qx}$ = HIGH
CLKx = HIGH; $\overline{CLKx}$ = HIGH	Qx = LOW, $\overline{Qx}$ = HIGH

Table 6. OUTPUT MODE CONFIGURATION TABLE

SMODEA/B[1:0] Inputs	Output Mode
00	LVPECL output.
01	LVDS output.
10	HCSL output.
11	High Impedance.

Table 7. ATTRIBUTES

Characteristic		Value
ESD Protection	Human Body Model Machine Model	>2 kV 200 V
Moisture Sensitivity (Note 1)	QFN48	Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in
Transistor Count		1318 Devices
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

1. For additional information, see Application Note AND8003/D.

Table 8. MAXIMUM RATINGS (Note 2)

Symbol	Parameter	Condition	Rating	Unit
V_{DD}	Positive Power Supply	GND = 0 V	4.6	V
V_I	XTAL_IN Input Voltage CLKx/$\overline{CLKx}$; SELx; SMODExx; OS_SE		$0 \le V_I \le V_{DD}$ $-0.5 \le V_I \le V_{DDO} + 0.5$	V V
V_o	Output Voltage	HCSL; LVCMOS	$-0.5 \le V_O \le V_{DDO} + 0.5$	V
I_o	LVPECL Output Current	Continuous Current Surge Current	50 100	mA
I_o	LVDS Output Current	Continuous Current Surge Current	10 15	mA
V_{OHCSL}	Output Voltage (HCSL)		−0.5 to V_{DDO} + 0.5	V
T_A	Operating Temperature Range, Industrial		−40 to 85	°C
T_{stg}	Storage Temperature Range		−65 to +150	°C
θ_{JA}	Thermal Resistance (Junction−to−Ambient)	0 lfpm 500 lfpm	30.5 24.9	°C/W
θ_{JC}	Thermal Resistance (Junction−to−Case)	(Note 2)	12 − 17	°C/W
T_{sol}	Soldering Temperature		+260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. JEDEC standard multilayer board − 2S2P (2 signal, 2 power).

DC ELECTRICAL CHARACTERISTICS

Table 9. DC ELECTRICAL CHARACTERISTICS POWER SUPPLY DC CHARACTERISTICS, GND = 0.0 V; T_A = −40°C to 85°C

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{DD}	Core Supply Voltage		2.375		3.465	V
V_{DDOx}	Output Supply Voltage		2.375		3.465	V
I_{DD}	Core Supply Current	LVPECL Outputs LVDS Outputs HCSL Outputs		85 155 90	120 185 120	mA
I_{DDO}	Output Supply Current	All LVPECL Outputs Unloaded ALL LVDS Outputs Loaded All HCSL Output Unloaded		50 60 45	70 80 60	mA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

Table 10. LVCMOS/LVTTL DC, V_{DD}/V_{DDO} = 2.5 V/2.5 V, 3.3 V/3.3 V or 3.3 V/2.5 V ±5%; GND = 0.0 V; T_A = −40°C to 85°C

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IH}	Input High Voltage (SEL0/1, SMODEA0/1, SMODEB0/1 OE_SE)	V_{DD} = 3.3 V V_{DD} = 2.5 V	2 1.7		V_{DD} + 0.3 V_{DD} + 0.3	V
V_{IL}	Input Low Voltage (SEL0/1, SMODEA0/1, SMODEB0/1 OE_SE)	V_{DD} = 3.3 V V_{DD} = 2.5 V	−0.3 −0.3		0.8 0.7	V
I_{IH}	Input High Current (SEL0/1, SMODEA0/1, SMODEB0/1 OE_SE)	V_{DD} = V_{IN} = 3.465 V			150	μA
I_{IL}	Input Low Current (SEL0/1, SMODEA0/1, SMODEB0/1 OE_SE)	V_{DD} = 3.465V, V_{IN} = 0 V	−150			μA
V_{OH}	Output High Voltage (Note 3) REFOUT	V_{DDO} = 3.3 V ±5% V_{DDO} = 2.5 V ±5%	2.3 1.5			V
V_{OL}	Output LOW Voltage (Note 3) REFOUT	V_{DDO} = 3.3 V ±5% V_{DDO} = 2.5 V ±5%			0.5 0.4	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

3. Outputs terminated with 50 Ω to V_{DDO}/2. See Parameter Measurement Information.

Table 11. DIFFERENTIAL INPUT DC CHARACTERISTICS, V_{DD}/V_{DDO} = 2.5 V/2.5 V, 3.3 V/3.3 V or 3.3 V/2.5 V ±5%; GND = 0.0 V; T_A = −40°C to 85°C

Symbol	Parameter		Test Conditions	Min	Typ	Max	Unit
I_{IH}	Input High Current	CLK0, CLK1, $\overline{CLK0}$, $\overline{CLK1}$	$V_{DD} = V_{IN}$ = 3.465 V			150	µA
I_{IL}	Input Low Current	CLK0, CLK1 $\overline{CLK0}$, $\overline{CLK1}$	V_{DD} = 3.465 V, V_{IN} = 0 V	−150			µA
V_{ID}	Input Voltage Swing (Note 4)			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; (Notes 4 and 5)			GND + 0.5		V_{DD} − 0.85	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

4. V_{IL} should not be less than −0.3 V.
5. Common mode input voltage is defined as V_{IH}.

Table 12. LVPECL DC OUTPUT CHARACTERISTICS, V_{DD}/V_{DDO} = 2.5 V/2.5 V, 3.3 V/3.3 V or 3.3 V/2.5 V ±5%; GND = 0.0 V; T_A = −40°C to 85°C (Note 6)

Symbol	Parameter	Min	Typ	Max	Unit
V_{OH}	Output High voltage	V_{DDO} − 1.4		V_{DDO} − 0.9	V
V_{OL}	Output Low voltage	V_{DDO} − 2.1		V_{DDO} − 1.7	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

6. Output pairs are terminated with 50 Ω to V_{DDO} − 2 V.

Table 13. LVDS DC OUTPUT CHARACTERISTICS, V_{DD}/V_{DDO} = 2.5 V/2.5 V, 3.3 V/3.3 V or 3.3 V/2.5 V ±5%; GND = 0.0 V; T_A = −40°C to 85°C. (Note 7)

Symbol	Parameter	Min	Typ	Max	Unit
V_{OH}	Output High Voltage		1.433		V
V_{OL}	Output Low Voltage		1.064		V
V_{OD}	Differential Output Voltage	250			mV
ΔV_{OD}	V_{OD} Magnitude Change			25	mV
V_{OS}	Offset Voltage	1.125	1.25	1.375	V
ΔV_{OS}	V_{OS} Magnitude Change			25	mV
R_O	Output Impedance	85		140	Ω

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

7. Output pairs are terminated with 100 Ω line to line at receiver.

Table 14. HCSL DC OUTPUT CHARACTERISTICS, V_{DD}/V_{DDO} = 2.5 V/2.5 V, 3.3 V/3.3 V or 3.3 V/2.5 V ±5%; GND = 0.0 V; T_A = −40°C to 85°C. (Note 8)

Symbol	Parameter	Min	Typ	Max	Unit
V_{OH}	HCSL Output HIGH Voltage	520		920	mV
V_{OL}	HCSL Output LOW Voltage	0		150	mV

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

8. Output pairs are terminated with 50 Ω to GND.

Table 15. CRYSTAL CHARACTERISTICS

Parameter	Test Conditions	Min	Typ	Max	Unit
Mode of Oscillation			Fundamental		
Frequency		10		50	MHz
Equivalent Series Resistance (ESR)				70	Ω
Shunt Capacitance				7	pF
Load Capacitance		10		18	pF
Crystal Drive Level				100	μW

AC ELECTRICAL CHARACTERISTICS

Table 16. AC ELECTRICAL CHARACTERISTICS, V_{DD}/V_{DDO} = 2.5 V/2.5 V, 3.3 V/3.3 V or 3.3 V/2.5 V ±5%; GND = 0.0 V; T_A = −40°C to 85°C (Note 9)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
f_{OSC}	Input Frequency	External Crystal Input	10		50	MHz
f_{OUT}	Output Frequency	Diff CLKx/$\overline{CLKx}$ Inputs OUTPUTS: LVPECL OUTPUTS: LVDS OUTPUTS: HCSL OUTPUTS: REFOUT		 1400 1200 250 250		MHz
		Single−ended Inputs XTAL_IN, CLKx, or $\overline{CLKx}$		 250		
$t_{JITTER}Φ$	Buffer Additive RMS Phase Jitter (Integrated 12 kHz − 20 MHz)	Diff CLKx/$\overline{CLKx}$ Inputs		0.03		ps
		Single ended XTAL_IN		0.03		
t_{PD}	Propagation Delay;	CLKx/$\overline{CLKx}$ to any Qx/$\overline{Qx}$ Output Mode LVPECL Output Mode LVDS Output Mode HCSL Output REFOUT, C_L = 10 pF	 700 850 950 1600	 900 1100 1300 2000	 1200 1400 1650 2600	ps
$t_{sk(o)}$	Output−to−Output Skew	Any Two Clock Outputs with the Same Buffer Type and Same Load		25	50	ps
$t_{sk(pp)}$	Part−to−Part Skew;	 Output Mode LVPECL Output Mode LVDS Output Mode HCSL		 45 30 30		ps
T_{OD}	Valid to High Z Delay, Output Disable	$CLK_x/\overline{CLK_x}$			200	ns
T_{OE}	High Z to Valid Delay, Output Enable	$CLK_x/\overline{CLK_x}$			200	ns
V_{RB}	Ringback Voltage Margin (Notes 10, 11)	HCSL Output	−100		100	mV
V_{MAX}	Voltage High (Notes 12, 13)	HCSL Output	520		920	mV
V_{MIN}	Voltage Low (Notes 12, 14)	HCSL Output	−150		150	mV
V_{CROSS}	Absolute Crossing Voltage (Notes 12, 15, 16)	HCSL Output	160		460	mV
$ΔV_{CROSS}$	Total Variation of VCROSS over all edges; (Notes 12, 15 and 17)	HCSL Output			140	mV

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

9. OUTPUT MODE LVPECL: Output pairs are terminated with 50 Ω to V_{DDO} − 2 V.
   OUTPUT MODE LVDS: Output pairs are terminated with 100 Ω line to line at receiver.
   OUTPUT MODE HCSL: Output pairs are terminated with 50 Ω to GND
   REFOUT Output terminated with 50 Ω to $V_{DDO}/2$.
10. Measurement taken from differential waveform.
11. T_{STABLE} is the time the differential clock must maintain a minimum ± 150 mV differential voltage after rising/falling edges before it is allowed to drop back into the VRB ±100 mV differential range.
12. Measurement taken from single−ended waveform.
13. Defined as the maximum instantaneous voltage including overshoot. See Parameter Measurement Information Section.
14. Defined as the minimum instantaneous voltage including undershoot. See Parameter Measurement Information Section.
15. Measured at crossing point where the instantaneous voltage value of the rising edge of Q_x equals the falling edge of $\overline{Qx}$.
16. Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.
17. Defined as the total variation of all crossing voltages of rising Q_x and falling nQ_x, This is the maximum allowed variance in V_{cross} for any particular system.
18. Measured from −150 mV to +150 mV on the differential waveform (Q_x minus nQ_x). The signal must be monotonic through the measurement region for rise and fall time. The 300 mV measurement window is centered on the differential zero crossing.

Table 16. AC ELECTRICAL CHARACTERISTICS, V_{DD}/V_{DDO} = 2.5 V/2.5 V, 3.3 V/3.3 V or 3.3 V/2.5 V ±5%; GND = 0.0 V; T_A = −40°C to 85°C (Note 9)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Δt_R / Δt_F	Rise/Fall Edge Rate (Notes 12, and 18)	HCSL Outputs; Measured between 150 mV to +150 mV	0.6		4.0	V/ns
t_R / t_F	Output Rise/Fall Time	HCSL Outputs 20% to 80% at 50 MHz V_{DDO} = 3.3 V V_{DDO} = 2.5 V	250 250		550 750	ps
t_R / t_F	Output Rise/ Fall Time	LVDS Outputs (20% to 80% at 50 MHz) V_{DDO} = 3.3 V V_{DDO} = 2.5 V	150 150		500 550	ps
t_R / t_F	Output Rise/ Fall Time	LVPECL Outputs (20% to 80% at 50 MHz) V_{DDO} = 3.3 V V_{DDO} = 2.5 V	125 125		325 375	ps
t_R / t_F	Output Rise/ Fall Time	REFOUT (20% to 80% at 50 MHz) C_L = 10 pF		550		ps
odc	Output Duty Cycle	f ≤ 350 MHz LVPECL f ≤ 250 MHz HCSL f ≤ 350 MHz LVDS	48 48 47		52 52 53	%
		f = 50 MHz REFOUT C_L = 10 pF	45		55	%
V_{PP}	Output Swing Single−Ended	LVPECL Outputs LVDS Outputs HCSL Outputs	400 250 520		1000	mV
MUX_ISOLATION	MUX Isolation	156.25 MHz	55			dB

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

9. OUTPUT MODE LVPECL: Output pairs are terminated with 50 Ω to V_{DDO} − 2 V.
OUTPUT MODE LVDS: Output pairs are terminated with 100 Ω line to line at receiver.
OUTPUT MODE HCSL: Output pairs are terminated with 50 Ω to GND
REFOUT Output terminated with 50 Ω to V_{DDO}/2.
10. Measurement taken from differential waveform.
11. T_{STABLE} is the time the differential clock must maintain a minimum ± 150 mV differential voltage after rising/falling edges before it is allowed to drop back into the VRB ±100 mV differential range.
12. Measurement taken from single−ended waveform.
13. Defined as the maximum instantaneous voltage including overshoot. See Parameter Measurement Information Section.
14. Defined as the minimum instantaneous voltage including undershoot. See Parameter Measurement Information Section.
15. Measured at crossing point where the instantaneous voltage value of the rising edge of Q_x equals the falling edge of $\overline{Qx}$.
16. Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.
17. Defined as the total variation of all crossing voltages of rising Q_x and falling nQ_x, This is the maximum allowed variance in V_{cross} for any particular system.
18. Measured from −150 mV to +150 mV on the differential waveform (Q_x minus nQ_x). The signal must be monotonic through the measurement region for rise and fall time. The 300 mV measurement window is centered on the differential zero crossing.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{DD} = 3.3 V, V_{DDO} = 3.3 V, T_A = +25°C

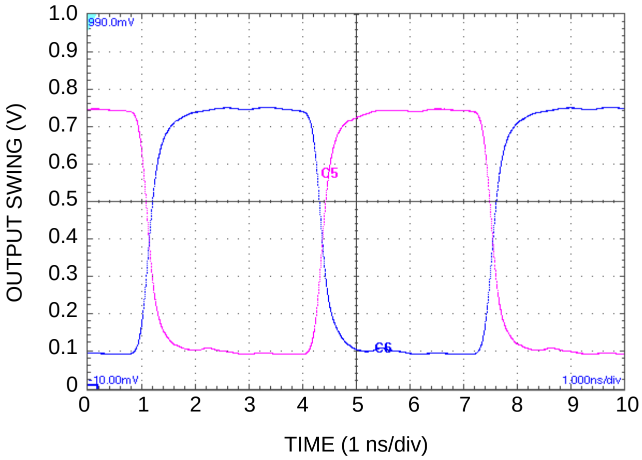


Figure 3. LVPECL Output Swing @ 156.25 MHz

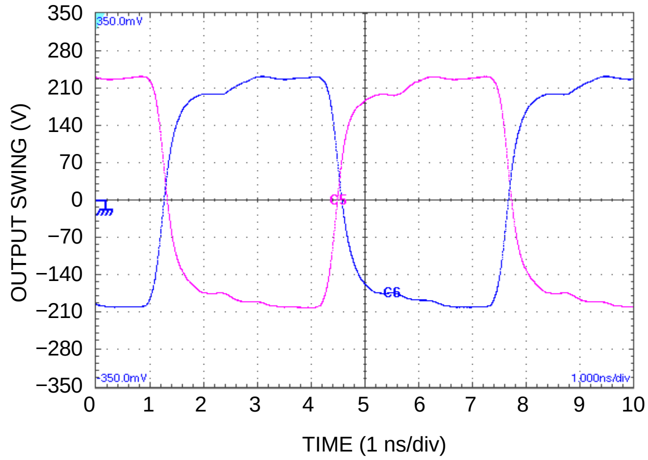


Figure 4. LVDS Output Swing @ 156.25 MHz

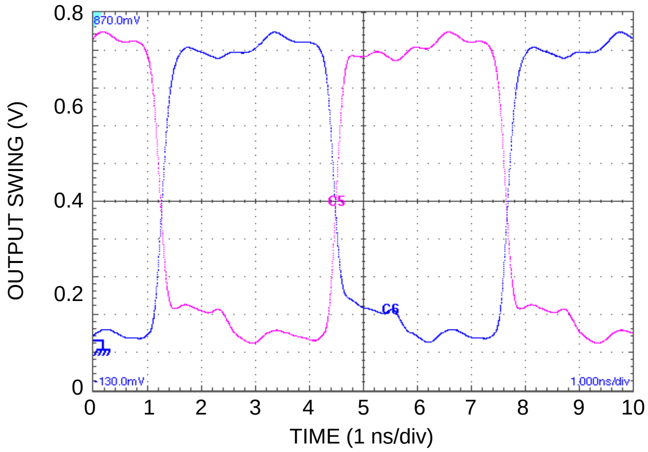


Figure 5. HCSL Output Swing @ 156.25 MHz

TYPICAL PERFORMANCE CHARACTERISTICS

V_{DD} = 3.3 V, V_{DDO} = 3.3 V, T_A = +25°C

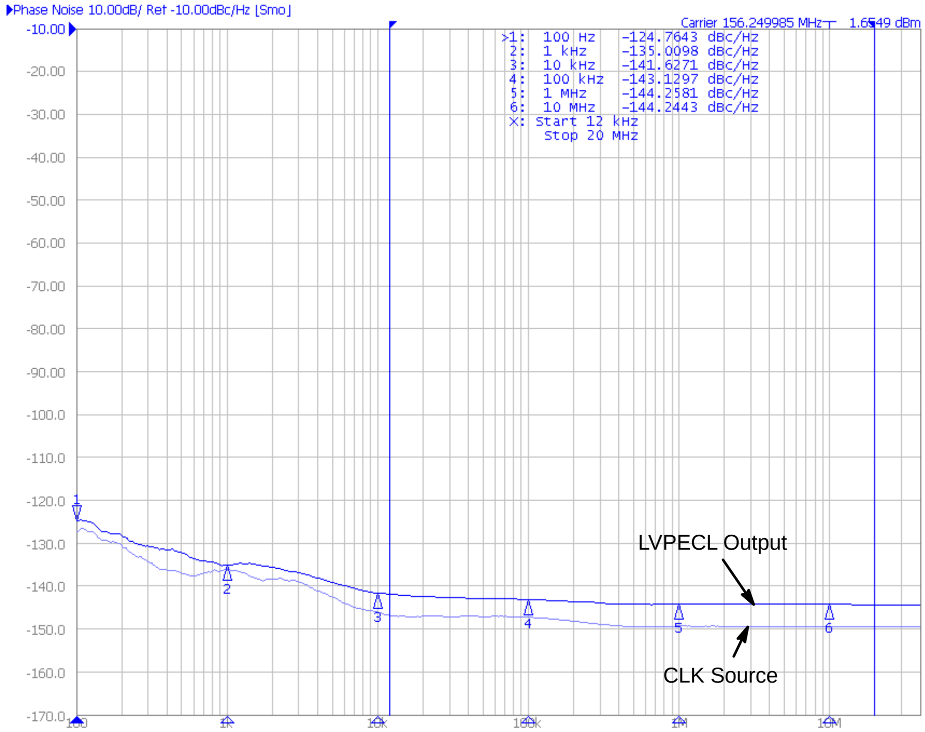


Figure 6. LVPECL Phase Noise @ 156.25 MHz

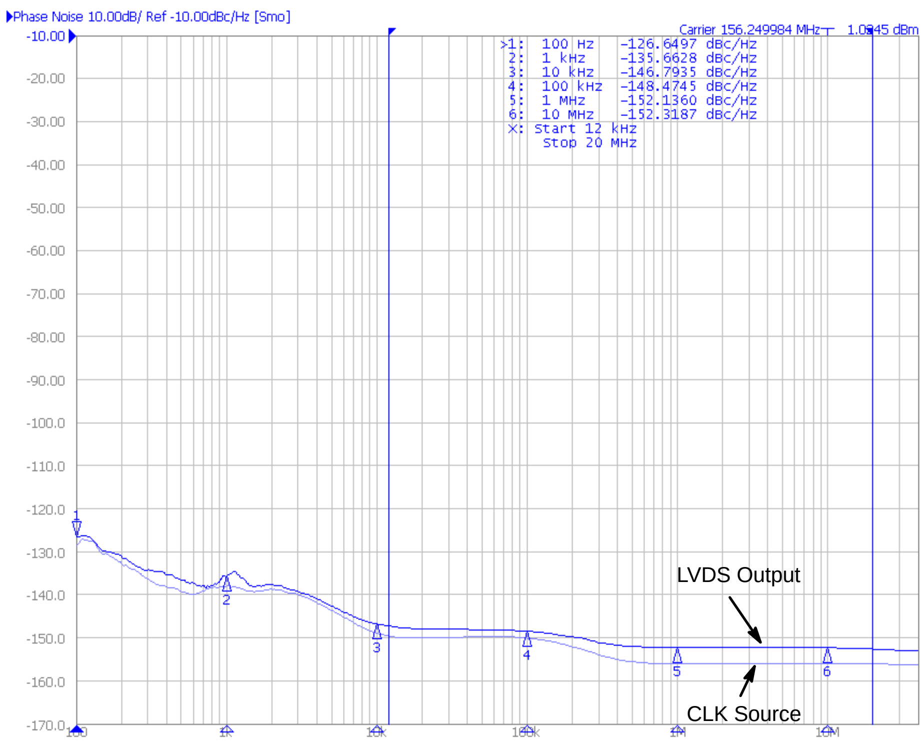


Figure 7. LVDS Phase Noise @ 156.25 MHz

TYPICAL PERFORMANCE CHARACTERISTICS

V_{DD} = 3.3 V, V_{DDO} = 3.3 V, T_A = +25°C

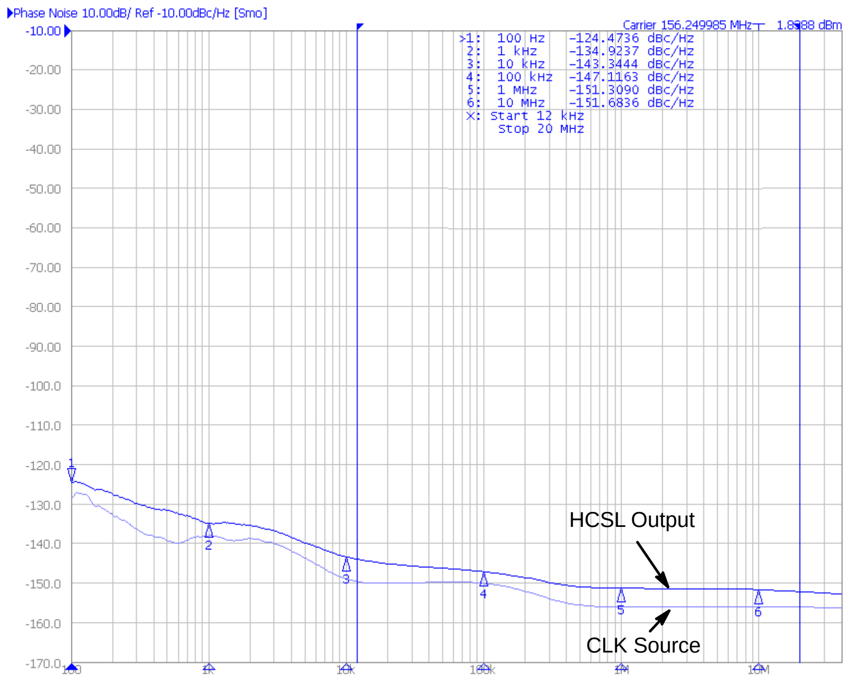


Figure 8. HCSL Phase Noise @ 156.25 MHz

PARAMETER MEASUREMENT INFORMATION

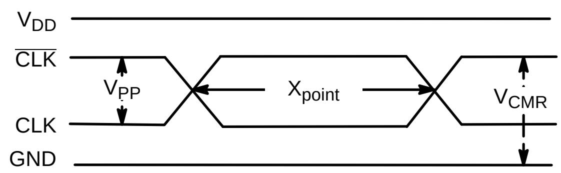


Figure 9. Differential Input Level

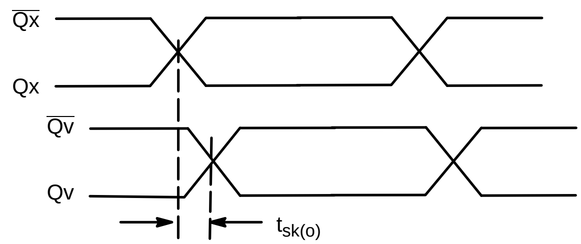


Figure 10. Within Device Output Skew x=Bank A or Bank B

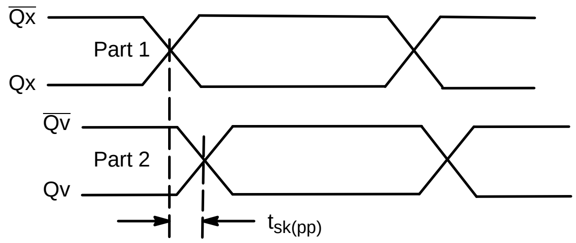


Figure 11. Device to Device Output Skew x = Bank A or Bank B

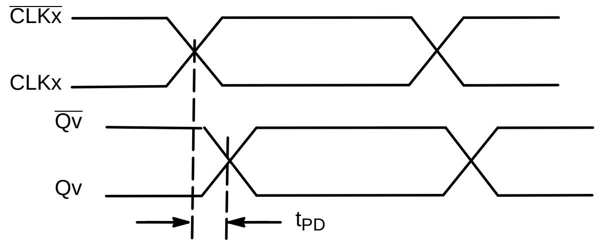


Figure 12. Propagation Delay

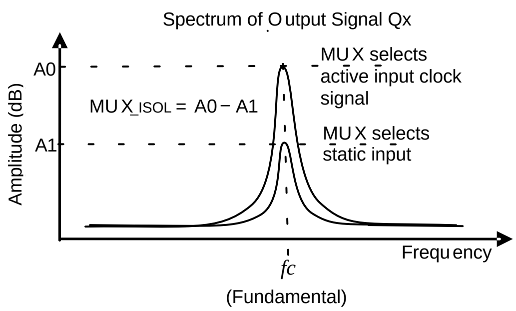


Figure 13. MUX Isolation

PARAMETER MEASUREMENT INFORMATION

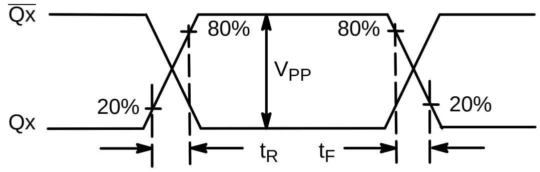


Figure 14. Output Rise/Fall Time

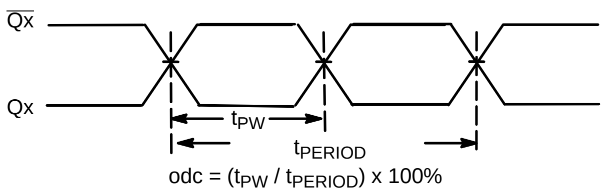


Figure 15. Output Duty Cycle / Pulse Width / Period

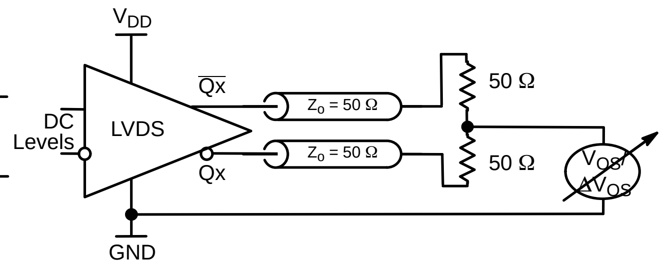


Figure 16. LVDS Offset Voltage Setup

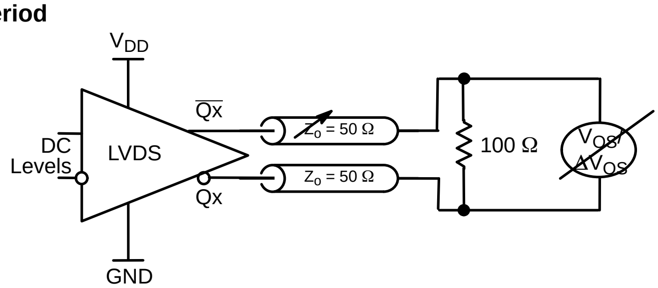


Figure 17. LVDS Differential Output Voltage Setup

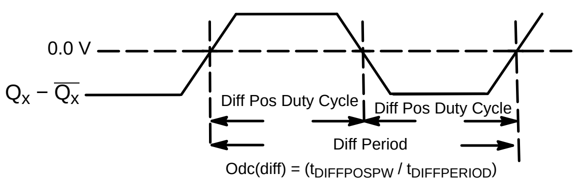


Figure 18. Differential Measurement Points for Duty Cycle / Pulse Width / Period

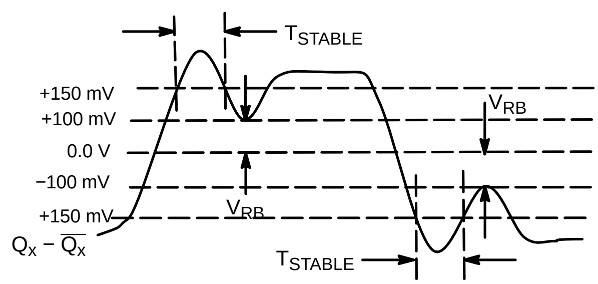


Figure 19. HCSL Differential Measurement Points for Ringback

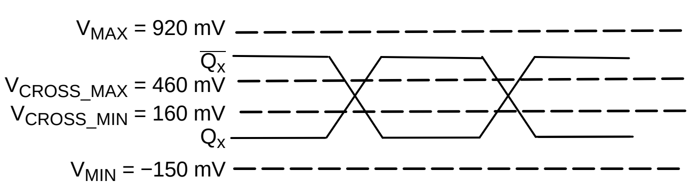


Figure 20. Single−Ended Measurement Points for HCSL Absolute Crossing Voltage

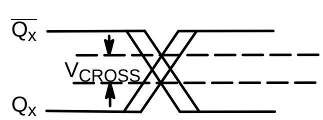


Figure 21. Single−Ended Measurement Points for HCSL ΔV_{CROSS}

APPLICATION INFORMATION

Recommendations for Unused Input and Output Pins

Inputs:

CLK/$\overline{\text{CLK}}$ Inputs

For applications not requiring the use of the differential input, both CLK and $\overline{\text{CLK}}$ can be left floating. Though not required, but for additional protection, a 1 kΩ resistor can be tied from CLK to ground.

Crystal Inputs

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1 kΩ resistor can be tied from XTAL_IN to ground.

LVCMOS Control Pins

All control pins have internal pulldowns; additional resistance is not required but can be added for additional protection. A 1 kΩ resistor can be used.

Outputs:

LVCMOS Outputs

The unused LVCMOS output can be left floating and recommend that there is no trace attached.

Differential Outputs

All unused differential outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

LVPECL Outputs

All unused LVPECL output pairs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

LVDS Outputs

All unused LVDS output pairs can be either left floating or terminated with 100 Ω across. If they are left floating, we recommend that there is no trace attached.

Differential Input with Single−Ended Interconnect

Refer to Figure 22 to interconnect a single ended signal to a Differential Pair of inputs. The reference bias voltage VREF = $V_{DD}/2$ is generated by the resistor divider of R1 and R2. Bypass capacitor (C1) can filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. Adjust R1 and R2 to common mode voltage of the signal input swing to preserve duty cycle.

This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination by R3 and R4 will attenuate the signal amplitude in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance. For most 50 Ω applications, R3 and R4 can be 100 Ω. The differential input can handle full rail LVCMOS signaling, but it is recommended that the amplitude be reduced. The datasheet specifies differential amplitude which needs to be doubled for a single ended equivalent stimulus. V_{ILmin} cannot be less than −0.3 V and V_{IH} max cannot be more than V_{DD} + 0.3 V. The datasheet specifications are characterized and guaranteed by using a differential signal.

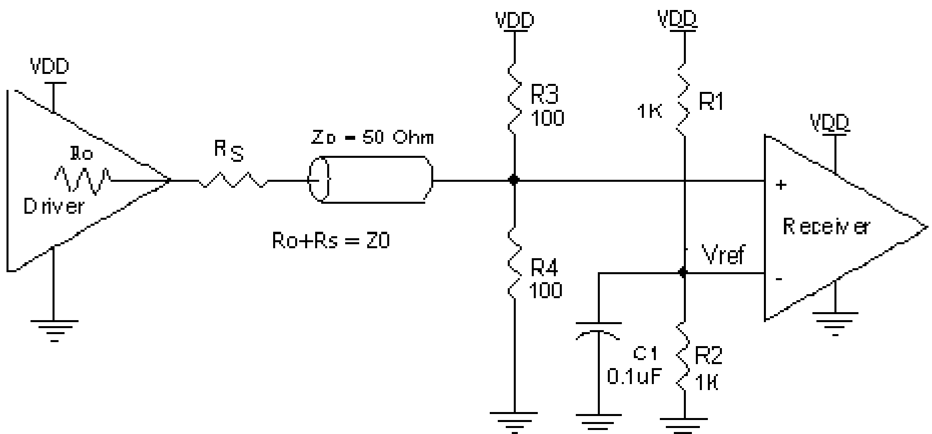


Figure 22. Differential Input with Single−Ended Interconnect

Crystal Input Interface

The device has been characterized with 18 pF parallel resonant crystals. The capacitor values, C1 and C2, shown in Figure 23 below were determined using an 18 pF parallel resonant crystal and were chosen to minimize the ppm error. The C1 and C2 load caps are in parallel and must be reduced by any input and stray capacitance. Typical value would be 36 pF minus all input and stray capacitance, or about 25 to 30 pF. The optimum C1 and C2 values can be slightly adjusted for different board layouts.

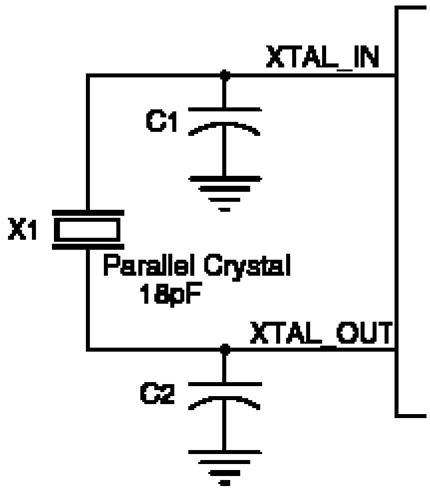


Figure 23. Crystal Input Interface

CLOCK Overdriving the XTAL Interface

The XTAL_IN input can accept a single−ended LVCMOS signal through an AC coupling capacitor. A general LVCMOS interface diagram is shown in Figure 24 and a general LVPECL interface in Figure 25. The XTAL_OUT pin must be left floating. The maximum amplitude of the input signal should not exceed 2 V and the input edge rate can be as slow as 10 ns. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50 Ω applications, R1 and R2 can be 100 Ω. This can also be accomplished by removing R1 and making R2 50 Ω. By overdriving the crystal oscillator, the device will be functional, but note, the device performance is guaranteed by using a quartz crystal.

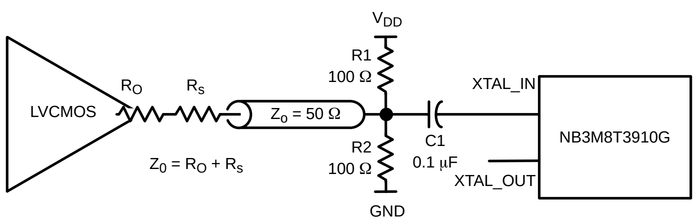


Figure 24. General Diagram for LVCMOS Driver to XTAL Input Interface

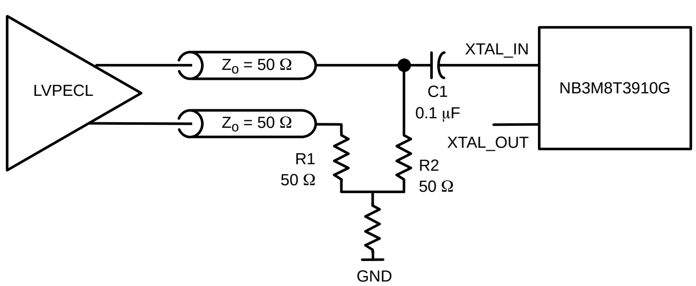


Figure 25. General Diagram for LVPECL Driver to XTAL Input Interface

HCSL RECOMMENDED TERMINATION

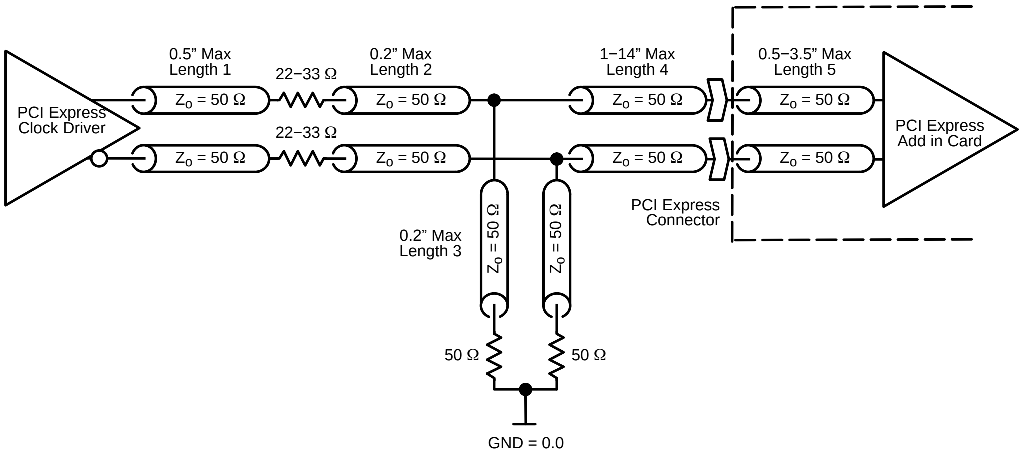


Figure 26. HCSL Recommended Interconnect and Termination Board to Board

Figure 26 is the recommended termination for applications which require the receiver and driver to be on a separate PCB. All traces should be 50 Ω impedance.

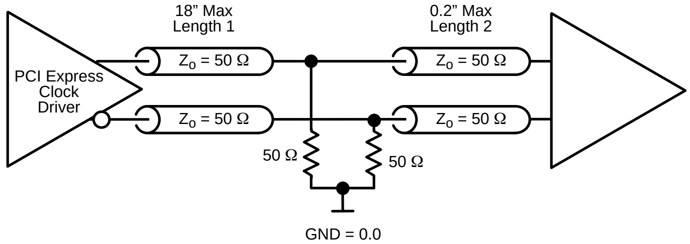


Figure 27. Recommended Termination Interconnect and Termination within a Board

Figure 27 is the recommended termination for applications which require a point to point connection and contain the driver and receiver on the same PCB. All traces should all be 50 Ω impedance.

LVDS Driver Termination

A general LVDS interface is shown in Figure 28. Standard termination for LVDS type output structure requires both a 100 Ω parallel resistor at the receiver and a 100 Ω differential transmission line environment. In order to avoid any transmission line reflection issues, the 100 Ω resistor must be placed as close to the receiver as possible. The standard termination schematic as shown in Figure 28 can be used with either type of output structure. In addition, since these outputs are LVDS compatible, the amplitude and common mode input range of the input receivers should be verified for compatibility with the output.

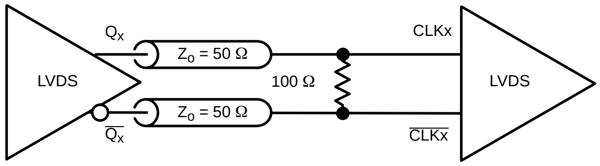


Figure 28. Typical LVDS Driver Termination

Termination for 3.3 V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines. The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50 Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. Figures 29 and 30 show two different layouts which are recommended only as guidelines. Consult AND8020/D for further termination information

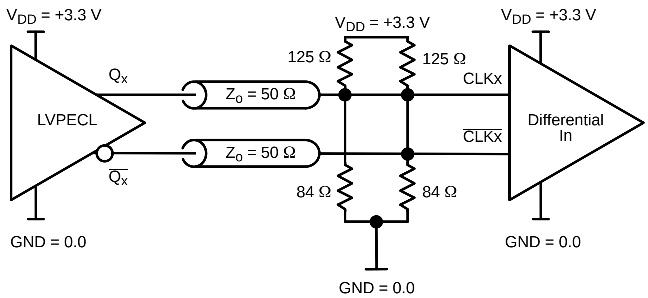


Figure 29. CLK / $\overline{\text{CLK}}$ Input Driven by 3.3 V LVPECL Driver (Thevenin Parallel Termination)

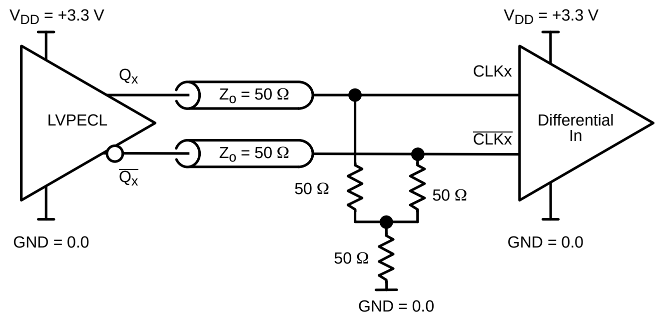


Figure 30. CLK / $\overline{\text{CLK}}$ Input Driven by 3.3 V LVPECL Driver (“Y” Parallel Termination)

Termination for 2.5 V LVPECL Outputs

Figures 31 and 32 show examples of termination for 2.5 V LVPECL driver. These terminations are equivalent to terminating 50 Ω to $V_{DD} - 2$ V. For V_{DDO} = 2.5 V, the V_{DDO} − 2 V is very close to ground level. The R3 in Figure 32 can be eliminated and the termination is shown in Figure 33. Consult AND8020 for further termination information

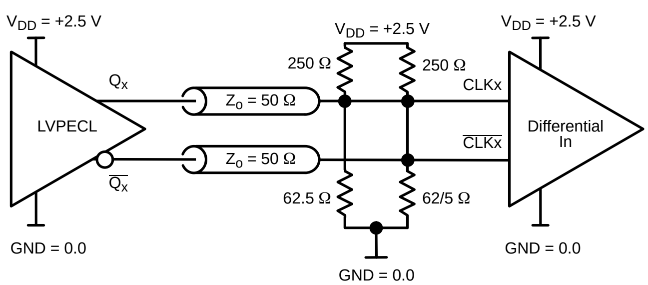


Figure 31. CLK / $\overline{\text{CLK}}$ Input Driven by 2.5 V LVPECL Driver (Thevenin Parallel Termination)

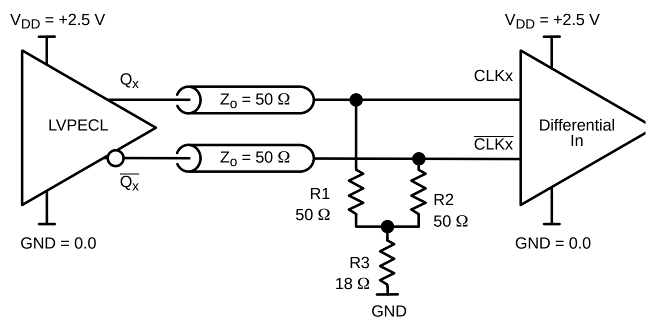


Figure 32. CLK / $\overline{\text{CLK}}$ Input Driven by 2.5 V LVPECL Driver (“Y” Parallel Termination)

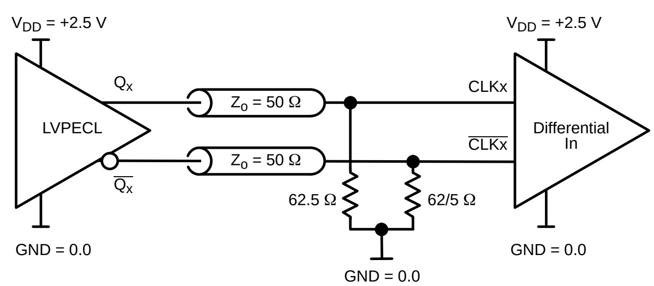


Figure 33. CLK / $\overline{\text{CLK}}$ Input Driven by 2.5 V LVPECL Driver (Modified “Y” Parallel Termination)

QFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in Figure 34. The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts. While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as thermal conduits. The number of vias may be application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13 mils (0.30 to 0.33 mm) with 1 oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only.

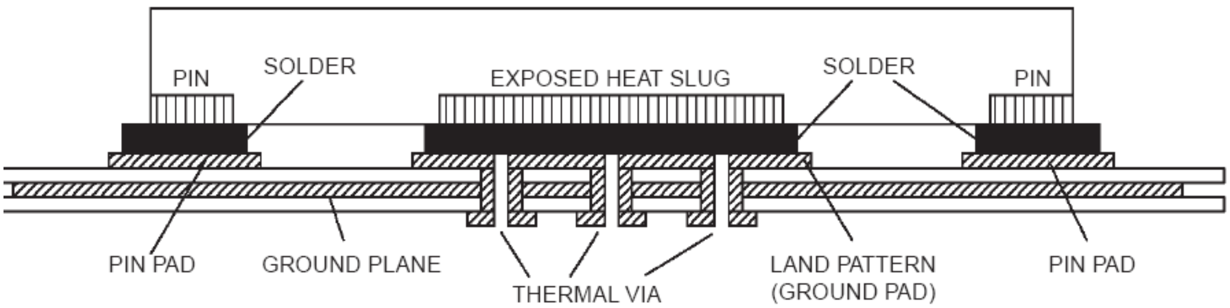


Figure 34. P.C. Assembly for Exposed Pad Thermal Release Path − Side View (drawing not to scale)

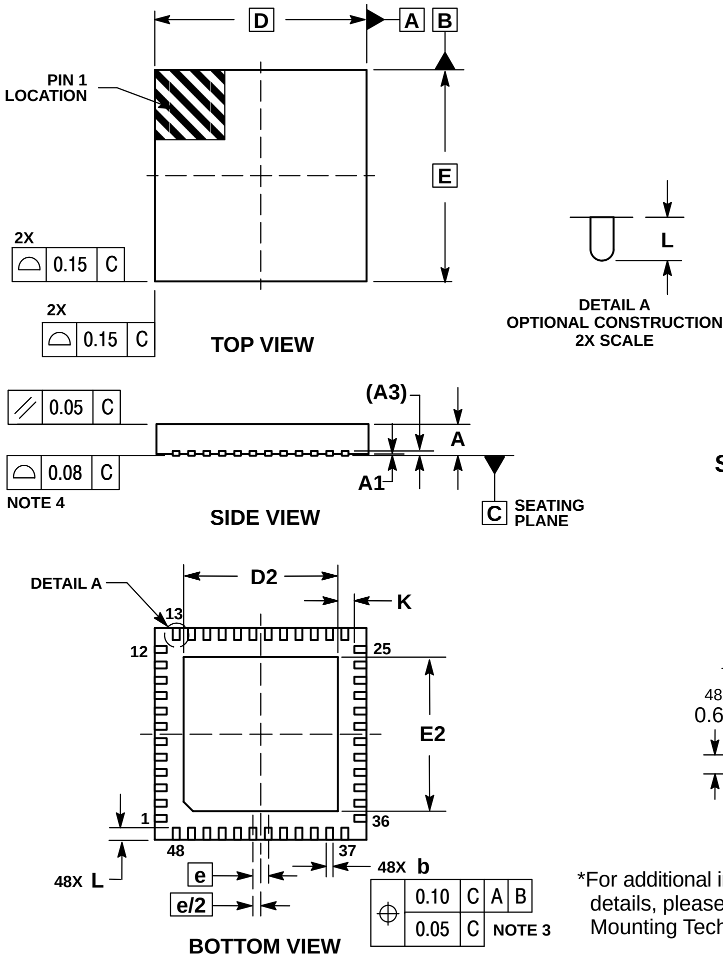
ORDERING INFORMATION

Device	Package	Shipping†
NB3M8T3910GMNR2G	QFN48 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

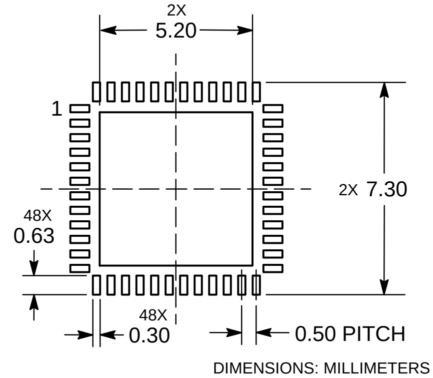
QFN48 7x7, 0.5P
CASE 485AJ
ISSUE O



NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO THE PLATED TERMINAL AND IS MEASURED ABETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	7.00 BSC	
D2	5.00	5.20
E	7.00 BSC	
E2	5.00	5.20
e	0.50 BSC	
K	0.20	−−−
L	0.30	0.50

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
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19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
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