# 3.3 V/5 V ECL Differential Receiver/Driver

# MC10EP16, MC100EP16

**ON Semiconductor®**

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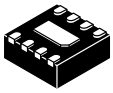
**SOIC−8 NB**
**D SUFFIX**
**CASE 751−07**


**TSSOP−8**
**DT SUFFIX**
**CASE 948R−02**



**DFN8**
**MN SUFFIX**
**CASE 506AA**

### Description

The EP16 is a world−class differential receiver/driver. The device is functionally equivalent to the EL16 and LVEL16 devices with higher performance capabilities. With output transition times significantly faster than the EL16 and LVEL16, the EP16 is ideally suited for interfacing with high frequency sources.

The $V_{BB}$ pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to $V_{BB}$ as a switching reference voltage. $V_{BB}$ may also rebias AC coupled inputs. When used, decouple $V_{BB}$ and $V_{CC}$ via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, $V_{BB}$ should be left open.

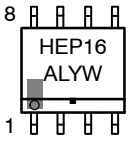
Under open input conditions (pulled to $V_{EE}$) internal input clamps will force the Q output LOW.

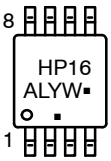
The 100 Series contains temperature compensation.

### Features

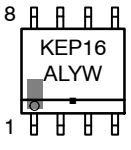
- 220 ps Typical Propagation Delay
- Maximum Frequency = > 4 GHz Typical
- PECL Mode Operating Range:
  $V_{CC}$ = 3.0 V to 5.5 V with $V_{EE}$ = 0 V
- NECL Mode Operating Range:
  $V_{CC}$ = 0 V with $V_{EE}$ = −3.0 V to −5.5 V
- Open Input Default State
- Safety Clamp on Inputs
- Q Output Will Default LOW with Inputs Open or at $V_{EE}$
- $V_{BB}$ Output
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant

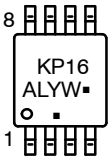
### MARKING DIAGRAMS*



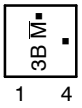




**SOIC−8 NB**




**TSSOP−8**




**DFN8**

H = MC10
K = MC100
3B = MC100
$\overline{M}$ = Date Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*For additional marking information, refer to Application Note AND8002/D.

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 8 of this data sheet.

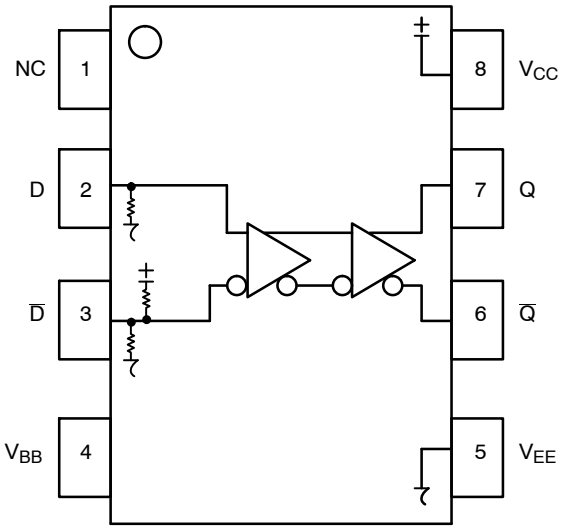



**Figure 1. 8−Lead Pinout (Top View) and Logic Diagram**

**Table 1. PIN DESCRIPTION**

| PIN | FUNCTION |
|---|---|
| D*, $\overline{D}$** | ECL Data Inputs |
| Q, $\overline{Q}$ | ECL Data Outputs |
| $V_{BB}$ | Reference Voltage Output |
| $V_{CC}$ | Positive Supply |
| $V_{EE}$ | Negative Supply |
| NC | No Connect |
| EP | (DFN8 only) Thermal exposed pad must be connected to a sufficient thermal conduit. Electrically connect to the most negative supply (GND) or leave unconnected, floating open. |

* Pins will default LOW when left open.
** Pins will default to $V_{CC}/2$ when left open.

**Table 2. ATTRIBUTES**

| Characteristics | Value |
|---|---|
| Internal Input Pulldown Resistor | 75 kΩ |
| Internal Input Pullup Resistor | 37.5 kΩ |
| ESD Protection<br>Human Body Model<br>Machine Model<br>Charged Device Model | <br>> 4 kV<br>> 200 V<br>> 2 kV |
| Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1) | Pb-Free Pkg |
| SOIC−8 NB<br>TSSOP−8<br>DFN8 | Level 1<br>Level 3<br>Level 1 |
| Flammability Rating<br>Oxygen Index: 28 to 34 | <br>UL 94 V−0 @ 0.125 in |
| Transistor Count | 167 Devices |
| Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test | |

1. For additional information, see Application Note AND8003/D.

**Table 3. MAXIMUM RATINGS**

| Symbol | Parameter | Condition 1 | Condition 2 | Rating | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | PECL Mode Power Supply | $V_{EE}$ = 0 V | | 6 | V |
| $V_{EE}$ | NECL Mode Power Supply | $V_{CC}$ = 0 V | | −6 | V |
| $V_I$ | PECL Mode Input Voltage<br>NECL Mode Input Voltage | $V_{EE}$ = 0 V<br>$V_{CC}$ = 0 V | $V_I \le V_{CC}$<br>$V_I \ge V_{EE}$ | 6<br>−6 | V |
| $I_{out}$ | Output Current | Continuous<br>Surge | | 50<br>100 | mA |
| $I_{BB}$ | $V_{BB}$ Sink/Source | | | ±0.5 | mA |
| $T_A$ | Operating Temperature Range | | | −40 to +85 | °C |
| $T_{stg}$ | Storage Temperature Range | | | −65 to +150 | °C |
| $\theta_{JA}$ | Thermal Resistance (Junction-to-Ambient) | 0 lfpm<br>500 lfpm | SOIC−8 NB<br>SOIC−8 NB | 190<br>130 | °C/W |
| $\theta_{JC}$ | Thermal Resistance (Junction-to-Case) | Standard Board | SOIC−8 NB | 41 to 44 | °C/W |
| $\theta_{JA}$ | Thermal Resistance (Junction-to-Ambient) | 0 lfpm<br>500 lfpm | TSSOP−8<br>TSSOP−8 | 185<br>140 | °C/W |
| $\theta_{JC}$ | Thermal Resistance (Junction-to-Case) | Standard Board | TSSOP−8 | 41 to 44 | °C/W |
| $\theta_{JA}$ | Thermal Resistance (Junction-to-Ambient) | 0 lfpm<br>500 lfpm | DFN8<br>DFN8 | 129<br>84 | °C/W |
| $\theta_{JC}$ | Thermal Resistance (Junction-to-Case) | (Note 2) | DFN8 | 35 to 40 | °C/W |
| $T_{sol}$ | Wave Solder (Pb-Free) | | | 265 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. JEDEC standard multilayer board − 2S2P (2 signal, 2 power)

**Table 4. 10EP DC CHARACTERISTICS, PECL** ($V_{CC}$ = 3.3 V, $V_{EE}$ = 0 V (Note 1))

| Symbol | Characteristic | −40°C | | | 25°C | | | 85°C | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $I_{EE}$ | Power Supply Current | 20 | 24 | 31 | 20 | 24 | 31 | 20 | 24 | 32 | mA |
| $V_{OH}$ | Output HIGH Voltage (Note 2) | 2165 | 2290 | 2415 | 2230 | 2355 | 2480 | 2290 | 2415 | 2540 | mV |
| $V_{OL}$ | Output LOW Voltage (Note 2) | 1365 | 1490 | 1615 | 1430 | 1555 | 1680 | 1490 | 1615 | 1740 | mV |
| $V_{IH}$ | Input HIGH Voltage (Single-Ended) | 2090 | | 2415 | 2155 | | 2480 | 2215 | | 2540 | mV |
| $V_{IL}$ | Input LOW Voltage (Single-Ended) | 1365 | | 1690 | 1430 | | 1755 | 1490 | | 1815 | mV |
| $V_{BB}$ | Output Voltage Reference | 1790 | 1890 | 1990 | 1855 | 1955 | 2055 | 1915 | 2015 | 2115 | mV |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 3) | 2.0 | | 3.3 | 2.0 | | 3.3 | 2.0 | | 3.3 | V |
| $I_{IH}$ | Input HIGH Current | | | 150 | | | 150 | | | 150 | μA |
| $I_{IL}$ | Input LOW Current<br>D<br>$\overline{D}$ | <br>0.5<br>−150 | | | <br>0.5<br>−150 | | | <br>0.5<br>−150 | | | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

1. Input and output parameters vary 1:1 with $V_{CC}$. $V_{EE}$ can vary +0.3 V to −2.2 V.
2. All loading with 50 Ω to $V_{CC}$ − 2.0 V.
3. $V_{IHCMR}$ min varies 1:1 with $V_{EE}$, $V_{IHCMR}$ max varies 1:1 with $V_{CC}$. The $V_{IHCMR}$ range is referenced to the most positive side of the differential input signal.

**Table 5. 10EP DC CHARACTERISTICS, PECL** ($V_{CC}$ = 5.0 V, $V_{EE}$ = 0 V (Note 1))

| Symbol | Characteristic | −40°C | | | 25°C | | | 85°C | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $I_{EE}$ | Power Supply Current | 20 | 24 | 31 | 20 | 24 | 31 | 20 | 24 | 32 | mA |
| $V_{OH}$ | Output HIGH Voltage (Note 2) | 3865 | 3990 | 4115 | 3930 | 4055 | 4180 | 3990 | 4115 | 4240 | mV |
| $V_{OL}$ | Output LOW Voltage (Note 2) | 3065 | 3190 | 3315 | 3130 | 3255 | 3380 | 3190 | 3315 | 3440 | mV |
| $V_{IH}$ | Input HIGH Voltage (Single-Ended) | 3790 | | 4115 | 3855 | | 4180 | 3915 | | 4240 | mV |
| $V_{IL}$ | Input LOW Voltage (Single-Ended) | 3065 | | 3390 | 3130 | | 3455 | 3190 | | 3515 | mV |
| $V_{BB}$ | Output Voltage Reference | 3490 | 3590 | 3690 | 3555 | 3655 | 3755 | 3615 | 3715 | 3815 | mV |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 3) | 2.0 | | 5.0 | 2.0 | | 5.0 | 2.0 | | 5.0 | V |
| $I_{IH}$ | Input HIGH Current | | | 150 | | | 150 | | | 150 | μA |
| $I_{IL}$ | Input LOW Current<br>D<br>$\overline{D}$ | <br>0.5<br>−150 | | | <br>0.5<br>−150 | | | <br>0.5<br>−150 | | | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

1. Input and output parameters vary 1:1 with $V_{CC}$. $V_{EE}$ can vary +2.0 V to −0.5 V.
2. All loading with 50 Ω to $V_{CC}$ − 2.0 V.
3. $V_{IHCMR}$ min varies 1:1 with $V_{EE}$, $V_{IHCMR}$ max varies 1:1 with $V_{CC}$. The $V_{IHCMR}$ range is referenced to the most positive side of the differential input signal.

**Table 6. 10EP DC CHARACTERISTICS, NECL** ($V_{CC}$ = 0 V; $V_{EE}$ = −5.5 V to −3.0 V (Note 1))

| Symbol | Characteristic | −40°C | | | 25°C | | | 85°C | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $I_{EE}$ | Power Supply Current | 20 | 24 | 31 | 20 | 24 | 31 | 20 | 24 | 32 | mA |
| VOH | Output HIGH Voltage (Note 2) | −1135 | −1010 | −885 | −1070 | −945 | −820 | −1010 | −885 | −760 | mV |
| $V_{OL}$ | Output LOW Voltage (Note 2) | −1935 | −1810 | −1685 | −1870 | −1745 | −1620 | −1810 | −1685 | −1560 | mV |
| $V_{IH}$ | Input HIGH Voltage (Single-Ended) | −1210 | | −885 | −1145 | | −820 | −1085 | | −760 | mV |
| $V_{IL}$ | Input LOW Voltage (Single-Ended) | −1935 | | −1610 | −1870 | | −1545 | −1810 | | −1485 | mV |
| $V_{BB}$ | Output Voltage Reference | −1510 | −1410 | −1310 | −1445 | −1345 | −1245 | −1385 | −1285 | −1185 | mV |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 3) | $V_{EE}$ + 2.0 | | 0.0 | $V_{EE}$ + 2.0 | | 0.0 | $V_{EE}$ + 2.0 | | 0.0 | V |
| $I_{IH}$ | Input HIGH Current | | | 150 | | | 150 | | | 150 | μA |
| $I_{IL}$ | Input LOW Current<br>D<br>$\overline{D}$ | <br>0.5<br>−150 | | | <br>0.5<br>−150 | | | <br>0.5<br>−150 | | | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

1. Input and output parameters vary 1:1 with $V_{CC}$.
2. All loading with 50 Ω to $V_{CC}$ − 2.0 V.
3. $V_{IHCMR}$ min varies 1:1 with $V_{EE}$, $V_{IHCMR}$ max varies 1:1 with $V_{CC}$. The $V_{IHCMR}$ range is referenced to the most positive side of the differential input signal.

**Table 7. 100EP DC CHARACTERISTICS, PECL** ($V_{CC}$ = 3.3 V, $V_{EE}$ = 0 V (Note 1))

| Symbol | Characteristic | −40°C | | | 25°C | | | 85°C | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $I_{EE}$ | Power Supply Current | 17 | 25 | 36 | 17 | 25 | 36 | 22 | 26 | 38 | mA |
| $V_{OH}$ | Output HIGH Voltage (Note 2) | 2155 | 2280 | 2405 | 2155 | 2280 | 2405 | 2155 | 2280 | 2405 | mV |
| $V_{OL}$ | Output LOW Voltage (Note 2) | 1355 | 1480 | 1605 | 1355 | 1480 | 1605 | 1355 | 1480 | 1605 | mV |
| $V_{IH}$ | Input HIGH Voltage (Single-Ended) | 2075 | | 2420 | 2075 | | 2420 | 2075 | | 2420 | mV |
| $V_{IL}$ | Input LOW Voltage (Single-Ended) | 1355 | | 1675 | 1355 | | 1675 | 1355 | | 1675 | mV |
| $V_{BB}$ | Output Voltage Reference | 1775 | 1875 | 1975 | 1775 | 1875 | 1975 | 1775 | 1875 | 1975 | mV |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 3) | 2.0 | | 3.3 | 2.0 | | 3.3 | 2.0 | | 3.3 | V |
| $I_{IH}$ | Input HIGH Current | | | 150 | | | 150 | | | 150 | μA |
| $I_{IL}$ | Input LOW Current<br>D<br>$\overline{D}$ | <br>0.5<br>−150 | | | <br>0.5<br>−150 | | | <br>0.5<br>−150 | | | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

1. Input and output parameters vary 1:1 with $V_{CC}$. $V_{EE}$ can vary +0.3 V to −2.2 V.
2. All loading with 50 Ω to $V_{CC}$ − 2.0 V.
3. $V_{IHCMR}$ min varies 1:1 with $V_{EE}$, $V_{IHCMR}$ max varies 1:1 with $V_{CC}$. The $V_{IHCMR}$ range is referenced to the most positive side of the differential input signal.

**Table 8. 100EP DC CHARACTERISTICS, PECL** ($V_{CC}$ = 5.0 V, $V_{EE}$ = 0 V (Note 1))

| Symbol | Characteristic | −40°C | | | 25°C | | | 85°C | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $I_{EE}$ | Power Supply Current | 17 | 25 | 36 | 17 | 25 | 36 | 22 | 26 | 38 | mA |
| $V_{OH}$ | Output HIGH Voltage (Note 2) | 3855 | 3980 | 4105 | 3855 | 3980 | 4105 | 3855 | 3980 | 4105 | mV |
| $V_{OL}$ | Output LOW Voltage (Note 2) | 3055 | 3180 | 3305 | 3055 | 3180 | 3305 | 3055 | 3180 | 3305 | mV |
| $V_{IH}$ | Input HIGH Voltage (Single-Ended) | 3775 | | 4120 | 3775 | | 4120 | 3775 | | 4120 | mV |
| $V_{IL}$ | Input LOW Voltage (Single-Ended) | 3055 | | 3375 | 3055 | | 3375 | 3055 | | 3375 | mV |
| $V_{BB}$ | Output Voltage Reference | 3475 | 3575 | 3675 | 3475 | 3575 | 3675 | 3475 | 3575 | 3675 | mV |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note3) | 2.0 | | 5.0 | 2.0 | | 5.0 | 2.0 | | 5.0 | V |
| $I_{IH}$ | Input HIGH Current | | | 150 | | | 150 | | | 150 | μA |
| $I_{IL}$ | Input LOW Current<br>D<br>$\overline{D}$ | <br>0.5<br>−150 | | | <br>0.5<br>−150 | | | <br>0.5<br>−150 | | | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

1. Input and output parameters vary 1:1 with $V_{CC}$. $V_{EE}$ can vary +2.0 V to −0.5 V.
2. All loading with 50 Ω to $V_{CC}$ − 2.0 V.
3. $V_{IHCMR}$ min varies 1:1 with $V_{EE}$, $V_{IHCMR}$ max varies 1:1 with $V_{CC}$. The $V_{IHCMR}$ range is referenced to the most positive side of the differential input signal.

**Table 9. 100EP DC CHARACTERISTICS, NECL** ($V_{CC}$ = 0 V; $V_{EE}$ = −5.5 V to −3.0 V (Note 1))

| Symbol | Characteristic | −40°C | | | 25°C | | | 85°C | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $I_{EE}$ | Power Supply Current | 17 | 25 | 36 | 17 | 25 | 36 | 22 | 26 | 38 | mA |
| $V_{OH}$ | Output HIGH Voltage (Note 2) | −1145 | −1020 | −895 | −1145 | −1020 | −895 | −1145 | −1020 | −895 | mV |
| $V_{OL}$ | Output LOW Voltage (Note 2) | −1945 | −1820 | −1695 | −1945 | −1820 | −1695 | −1945 | −1820 | −1695 | mV |
| $V_{IH}$ | Input HIGH Voltage (Single-Ended) | −1225 | | −880 | −1225 | | −880 | −1225 | | −880 | mV |
| $V_{IL}$ | Input LOW Voltage (Single-Ended) | −1945 | | −1625 | −1945 | | −1625 | −1945 | | −1625 | mV |
| $V_{BB}$ | Output Voltage Reference | −1525 | −1425 | −1325 | −1525 | −1425 | −1325 | −1525 | −1425 | −1325 | mV |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 3) | $V_{EE}$ + 2.0 | | 0.0 | $V_{EE}$ + 2.0 | | 0.0 | $V_{EE}$ + 2.0 | | 0.0 | V |
| $I_{IH}$ | Input HIGH Current | | | 150 | | | 150 | | | 150 | μA |
| $I_{IL}$ | Input LOW Current<br>D<br>$\overline{D}$ | <br>0.5<br>−150 | | | <br>0.5<br>−150 | | | <br>0.5<br>−150 | | | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

1. Input and output parameters vary 1:1 with $V_{CC}$.
2. All loading with 50 Ω to $V_{CC}$ −2.0 V.
3. $V_{IHCMR}$ min varies 1:1 with $V_{EE}$, $V_{IHCMR}$ max varies 1:1 with $V_{CC}$. The $V_{IHCMR}$ range is referenced to the most positive side of the differential input signal.

**Table 10. AC CHARACTERISTICS** ($V_{CC}$ = 0 V; $V_{EE}$ = −3.0 V to −5.5 V or $V_{CC}$ = 3.0 V to 5.5 V; $V_{EE}$ = 0 V (Note 1))

| Symbol | Characteristic | −40°C | | | 25°C | | | 85°C | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $f_{max}$ | Maximum Frequency (Figure 2) | | > 4 | | | > 4 | | | > 4 | | GHz |
| $t_{PLH}$, $t_{PHL}$ | Propagation Delay to Output Differential | 150 | 220 | 280 | 150 | 220 | 280 | 160 | 240 | 300 | ps |
| $t_{SKEW}$ | Duty Cycle Skew (Note 2) | | 5.0 | 20 | | 5.0 | 20 | | 5.0 | 20 | ps |
| $t_{JITTER}$ | Cycle-to-Cycle Jitter (Figure 2) | | 0.2 | < 1 | | 0.2 | < 1 | | 0.2 | < 1 | ps |
| $V_{PP}$ | Input Voltage Swing (Differential Configuration) | 150 | 800 | 1200 | 150 | 800 | 1200 | 150 | 800 | 1200 | mV |
| $t_r$<br>$t_f$ | Output Rise/Fall Times<br>Q, $\overline{Q}$ (20%−80%) | 70 | 120 | 170 | 80 | 130 | 180 | 100 | 150 | 200 | ps |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

1. Measured using a 750 mV source, 50% duty cycle clock source. All loading with 50 Ω to $V_{CC}$ − 2.0 V.
2. Skew is measured between outputs under identical transitions. Duty cycle skew is defined only for differential operation when the delays are measured from the cross point of the inputs to the cross point of the outputs.

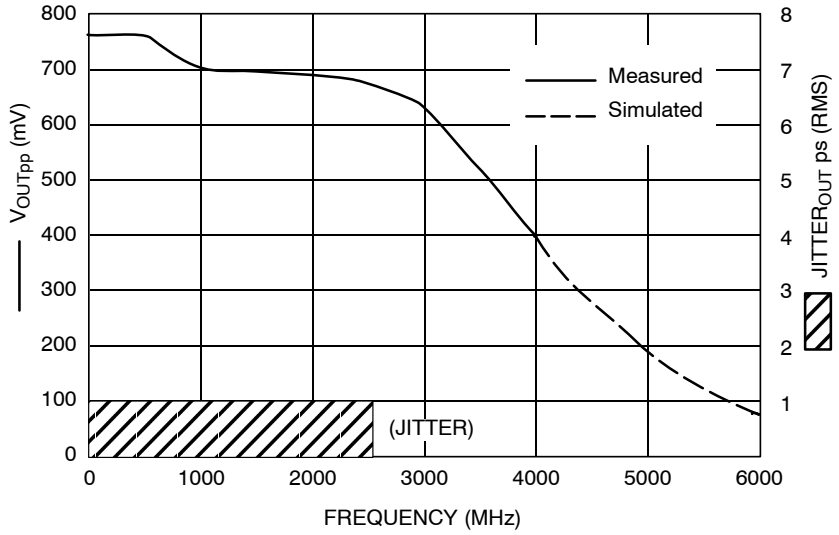



**Figure 2. $F_{max}$/Jitter**

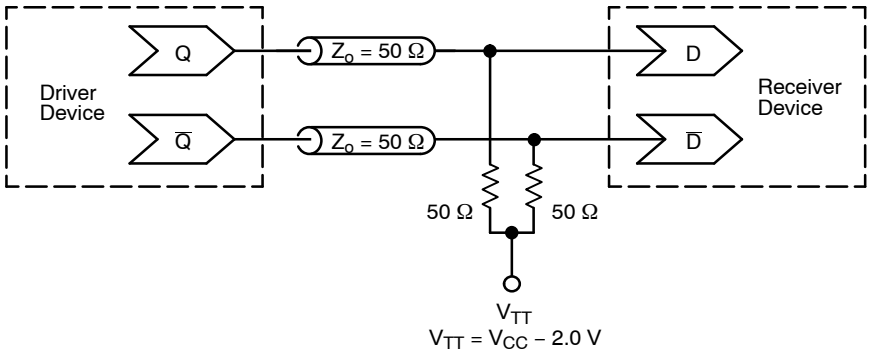



**Figure 3. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020/D – Termination of ECL Logic Devices.)**

## ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| MC10EP16DG | SOIC−8 NB (Pb-Free) | 98 Units / Tube |
| MC10EP16DTG | TSSOP−8 (Pb-Free) | 100 Units / Tube |
| MC10EP16DTR2G | TSSOP−8 (Pb-Free) | 2500 / Tape & Reel |
| MC100EP16DG | SOIC−8 NB (Pb-Free) | 98 Units / Tube |
| MC100EP16DTG | TSSOP−8 (Pb-Free) | 100 Units / Tube |
| MC100EP16DTR2G | TSSOP−8 (Pb-Free) | 2500 / Tape & Reel |
| MC100EP16MNR4G | DFN8 (Pb-Free) | 1000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

### Resource Reference of Application Notes

**AN1405/D** – ECL Clock Distribution Techniques

**AN1406/D** – Designing with PECL (ECL at +5.0 V)

**AN1503/D** – ECLinPS™ I/O SPiCE Modeling Kit

**AN1504/D** – Metastability and the ECLinPS Family

**AN1568/D** – Interfacing Between LVDS and ECL

**AN1672/D** – The ECL Translator Guide

**AND8001/D** – Odd Number Counters Design

**AND8002/D** – Marking and Date Codes

**AND8020/D** – Termination of ECL Logic Devices

**AND8066/D** – Interfacing with ECLinPS

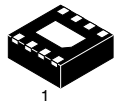
**AND8090/D** – AC Characteristics of ECL Devices

# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS

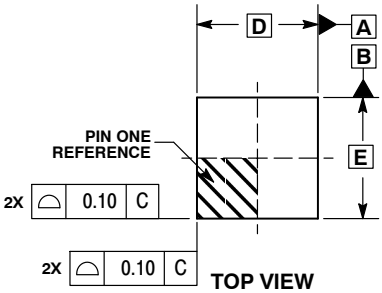
ON Semiconductor®

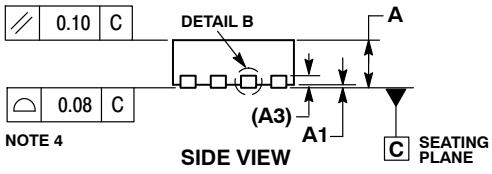
**DFN8 2x2, 0.5P**
CASE 506AA−01
ISSUE E

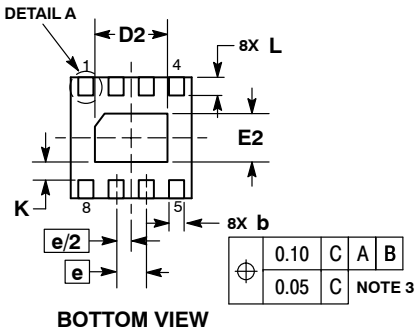
DATE 22 JAN 2010

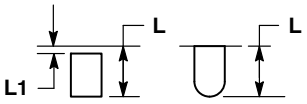


SCALE 4:1

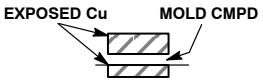



**DETAIL A**
OPTIONAL
CONSTRUCTIONS

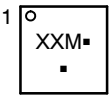



**DETAIL B**
OPTIONAL
CONSTRUCTION

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994 .
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 0.80 | 1.00 |
| A1 | 0.00 | 0.05 |
| A3 | 0.20 REF | |
| b | 0.20 | 0.30 |
| D | 2.00 BSC | |
| D2 | 1.10 | 1.30 |
| E | 2.00 BSC | |
| E2 | 0.70 | 0.90 |
| e | 0.50 BSC | |
| K | 0.30 REF | |
| L | 0.25 | 0.35 |
| L1 | −−− | 0.10 |

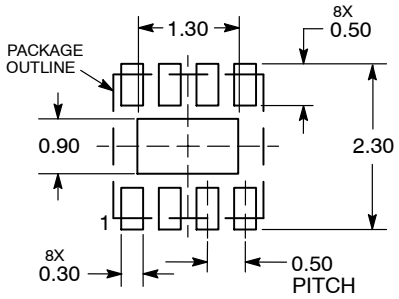
### GENERIC MARKING DIAGRAM*




XX = Specific Device Code
M = Date Code
▪ = Pb−Free Device

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

### RECOMMENDED SOLDERING FOOTPRINT*




DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

| | | |
|---|---|---|
| DOCUMENT NUMBER: | 98AON18658D | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red. |
| DESCRIPTION: | DFN8, 2.0X2.0, 0.5MM PITCH | PAGE 1 OF 1 |

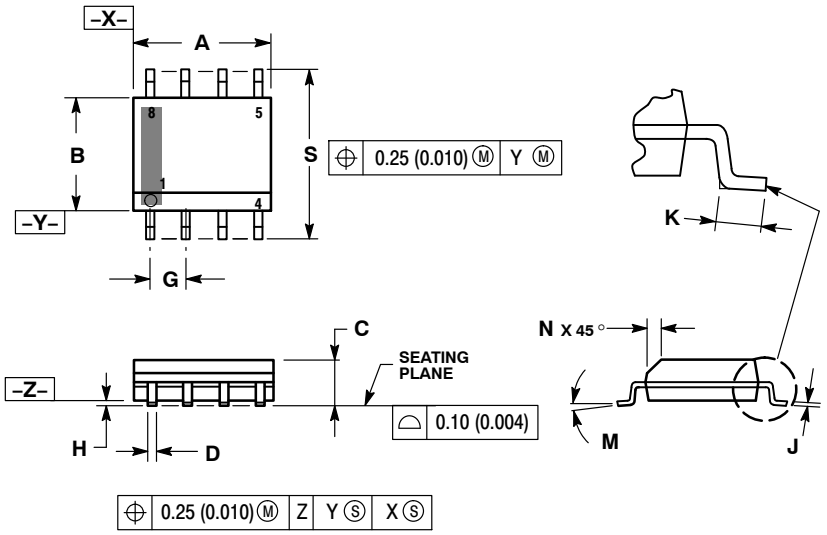
# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS

ON Semiconductor®

SCALE 1:1

**SOIC−8 NB**
CASE 751−07
ISSUE AK

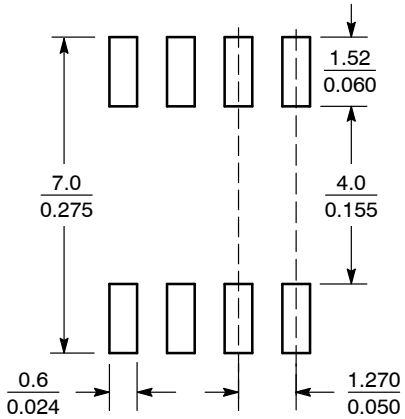
DATE 16 FEB 2011




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 4.80 | 5.00 | 0.189 | 0.197 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.053 | 0.069 |
| D | 0.33 | 0.51 | 0.013 | 0.020 |
| G | 1.27 BSC | | 0.050 BSC | |
| H | 0.10 | 0.25 | 0.004 | 0.010 |
| J | 0.19 | 0.25 | 0.007 | 0.010 |
| K | 0.40 | 1.27 | 0.016 | 0.050 |
| M | 0° | 8° | 0° | 8° |
| N | 0.25 | 0.50 | 0.010 | 0.020 |
| S | 5.80 | 6.20 | 0.228 | 0.244 |

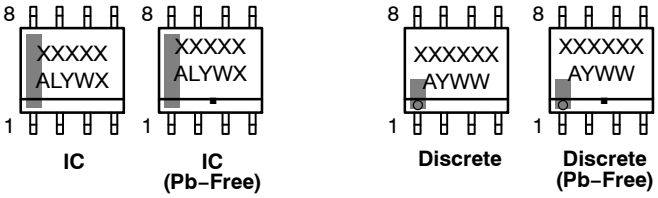
### SOLDERING FOOTPRINT*




SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

### GENERIC MARKING DIAGRAM*




XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

**STYLES ON PAGE 2**

| | | |
|---|---|---|
| **DOCUMENT NUMBER:** | **98ASB42564B** | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| **DESCRIPTION:** | **SOIC−8 NB** | **PAGE 1 OF 2** |

**SOIC−8 NB**
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

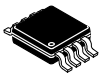
| | | | |
|---|---|---|---|
| **DOCUMENT NUMBER:** | **98ASB42564B** | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. | |
| **DESCRIPTION:** | **SOIC−8 NB** | | **PAGE 2 OF 2** |

# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS

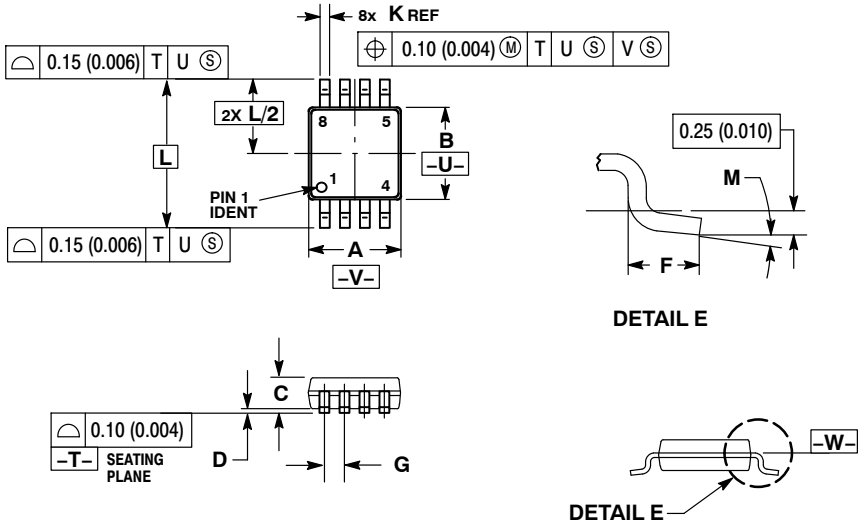
ON Semiconductor®

**TSSOP 8**
**CASE 948R–02**
**ISSUE A**

**DATE 04/07/2000**



**SCALE 2:1**




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 2.90 | 3.10 | 0.114 | 0.122 |
| B | 2.90 | 3.10 | 0.114 | 0.122 |
| C | 0.80 | 1.10 | 0.031 | 0.043 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.40 | 0.70 | 0.016 | 0.028 |
| G | 0.65 BSC | | 0.026 BSC | |
| K | 0.25 | 0.40 | 0.010 | 0.016 |
| L | 4.90 BSC | | 0.193 BSC | |
| M | 0° | 6° | 0° | 6° |

| | | |
|---|---|---|
| **DOCUMENT NUMBER:** | **98AON00236D** | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
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