

# CAT24C64BC4, CAT24C64BAC4

## EEPROM Serial 64-Kb I<sup>2</sup>C in a 4-ball WLCSP

### Description

The CAT24C64BC4 and CAT24C64BAC4 are EEPROM Serial 64-Kb I<sup>2</sup>C devices available in a 4-ball WLCSP package. Both devices are internally organized as 8192 words of 8 bits each.

They feature a 32-byte page write buffer and support the Standard (100 kHz), Fast (400 kHz) and Fast-Plus (1 MHz) I<sup>2</sup>C protocol. The CAT24C64BC4 and CAT24C64BAC4 respond to a different Slave Address and are therefore suitable in applications that require two serial EEPROM devices with 4-ball WLCSP on the same I<sup>2</sup>C bus.

### Features

- Supports Standard, Fast and Fast-Plus I<sup>2</sup>C Protocol
- 1.7 V to 5.5 V Supply Voltage Range
- 32-Byte Page Write Buffer
- Schmitt Triggers and Noise Suppression Filters on I<sup>2</sup>C Bus Inputs (SCL and SDA)
- Low Power CMOS Technology
- 1,000,000 Program/Erase Cycles
- 100 Year Data Retention
- Industrial Temperature Range
- 4-ball WLCSP Package
- This Device is Pb-Free, Halogen Free/BFR Free, and RoHS Compliant

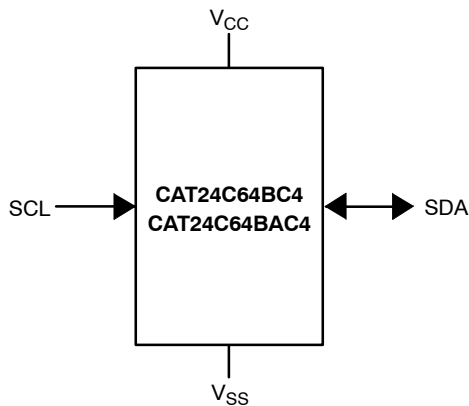


Figure 1. Functional Symbol



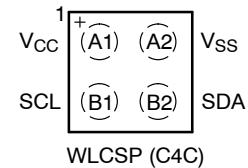
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WLCSP-4  
C4C SUFFIX  
CASE 567JY

### PIN CONFIGURATION (Top View)



### MARKING DIAGRAM



- X = Specific Device Code  
A: CAT24C64BC4  
D: CAT24C64BAC4
- Y = Production Year (Last Digit)
- W = Work Week

For the location of Pin 1, please consult the corresponding package drawing.

### PIN FUNCTION

Pin Name	Function
SDA	Serial Data
SCL	Serial Clock
V <sub>CC</sub>	Power Supply
V <sub>SS</sub>	Ground

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 8 of this data sheet.

# CAT24C64BC4, CAT24C64BAC4

**Table 1. ABSOLUTE MAXIMUM RATINGS**

Parameters	Ratings	Units
Storage Temperature	-65 to +150	°C
Voltage on Any Pin with Respect to Ground (Note 1)	-0.5 to +6.5	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- The DC input voltage on any pin should not be lower than -0.5 V or higher than  $V_{CC} + 0.5$  V. During transitions, the voltage on any pin may undershoot to no less than -1.5 V or overshoot to no more than  $V_{CC} + 1.5$  V, for periods of less than 20 ns.

**Table 2. RELIABILITY CHARACTERISTICS** (Note 2)

Symbol	Parameter	Min	Units
$N_{END}$ (Note 3)	Endurance	1,000,000	Program/Erase Cycles
$T_{DR}$	Data Retention	100	Years

- These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC-Q100 and JEDEC test methods.
- Page Mode,  $V_{CC} = 5$  V, 25°C.

**Table 3. D.C. OPERATING CHARACTERISTICS** ( $V_{CC} = 1.7$  V to 5.5 V,  $T_A = -40$ °C to +85°C, unless otherwise specified.)

Symbol	Parameter	Test Conditions	Min	Max	Units
$I_{CCR}$	Read Current	Read, $f_{SCL} = 1$ MHz		0.4	mA
$I_{CCW}$	Write Current	Write		0.6	mA
$I_{SB}$	Standby Current	All I/O Pins at GND or $V_{CC}$		1	μA
$I_L$	I/O Pin Leakage	Pin at GND or $V_{CC}$		2	μA
$V_{IL}$	Input Low Voltage	$V_{CC} \geq 2.2$ V	-0.5	$V_{CC} \times 0.3$	V
		$V_{CC} < 2.2$ V	-0.5	$V_{CC} \times 0.25$	V
$V_{IH}$	Input High Voltage	$V_{CC} \geq 2.2$ V	$V_{CC} \times 0.7$	$V_{CC} + 0.5$	V
		$V_{CC} < 2.2$ V	$V_{CC} \times 0.75$	$V_{CC} + 0.5$	V
$V_{OL}$	Output Low Voltage	$V_{CC} \geq 2.2$ V, $I_{OL} = 3.0$ mA		0.4	V
		$V_{CC} < 2.2$ V, $I_{OL} = 1.0$ mA		0.2	V

**Table 4. PIN IMPEDANCE CHARACTERISTICS** ( $V_{CC} = 1.7$  V to 5.5 V,  $T_A = -40$ °C to +85°C, unless otherwise specified.)

Symbol	Parameter	Conditions	Max	Units
$C_{IN}$ (Note 4)	SDA I/O Pin Capacitance	$V_{IN} = 0$ V	8	pF
$C_{IN}$ (Note 4)	Input Capacitance (other pins)	$V_{IN} = 0$ V	6	pF

- These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC-Q100 and JEDEC test methods.

## CAT24C64BC4, CAT24C64BAC4

**Table 5. A.C. CHARACTERISTICS** ( $V_{CC} = 1.7\text{ V to }5.5\text{ V}$ ,  $T_A = -40^\circ\text{C to }+85^\circ\text{C}$ ) (Note 5)

Symbol	Parameter	Standard		Fast		Fast-Plus		Units
		Min	Max	Min	Max	Min	Max	
$F_{SCL}$	Clock Frequency		100		400		1,000	kHz
$t_{HD:STA}$	START Condition Hold Time	4		0.6		0.25		$\mu\text{s}$
$t_{LOW}$	Low Period of SCL Clock	4.7		1.3		0.45		$\mu\text{s}$
$t_{HIGH}$	High Period of SCL Clock	4		0.6		0.35		$\mu\text{s}$
$t_{SU:STA}$	START Condition Setup Time	4.7		0.6		0.25		$\mu\text{s}$
$t_{HD:DAT}$	Data In Hold Time	0		0		0		$\mu\text{s}$
$t_{SU:DAT}$	Data In Setup Time	250		100		50		ns
$t_R$ (Note 6)	SDA and SCL Rise Time		1,000		300		100	ns
$t_F$ (Note 6)	SDA and SCL Fall Time		300		300		100	ns
$t_{SU:STO}$	STOP Condition Setup Time	4		0.6		0.25		$\mu\text{s}$
$t_{BUF}$	Bus Free Time Between STOP and START	4.7		1.3		0.5		$\mu\text{s}$
$t_{AA}$	SCL Low to Data Out Valid		3.5		0.9		0.40	$\mu\text{s}$
$t_{DH}$ (Note 6)	Data Out Hold Time	100		100		50		ns
$T_i$ (Note 6)	Noise Pulse Filtered at SCL and SDA Inputs		50		50		50	ns
$t_{WR}$	Write Cycle Time		4		4		4	ms
$t_{PU}$ (Notes 6, 7)	Power-up to Ready Mode		0.35		0.35		0.35	ms

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Test conditions according to "A.C. Test Conditions" table.

6. Tested initially and after a design or process change that affects this parameter.

7.  $t_{PU}$  is the delay between the time  $V_{CC}$  is stable and the device is ready to accept commands.

**Table 6. A.C. TEST CONDITIONS**

Input Levels	$V_{CC} \geq 2.2\text{ V}$ : $0.2 \times V_{CC}$ to $0.8 \times V_{CC}$ $V_{CC} < 2.2\text{ V}$ : $0.15 \times V_{CC}$ to $0.85 \times V_{CC}$
Input Rise and Fall Times	$\leq 50\text{ ns}$
Input Reference Levels	$0.3 \times V_{CC}$ , $0.7 \times V_{CC}$
Output Reference Levels	$0.3 \times V_{CC}$ , $0.7 \times V_{CC}$
Output Load	Current Source: $I_{OL} = 3\text{ mA}$ ( $V_{CC} \geq 2.2\text{ V}$ ); $I_{OL} = 1\text{ mA}$ ( $V_{CC} < 2.2\text{ V}$ ); $C_L = 100\text{ pF}$

# CAT24C64BC4, CAT24C64BAC4

## Power-On Reset (POR)

Each CAT24C64BC4/CAT24C64BAC4 incorporates Power-On Reset (POR) circuitry which protects the internal logic against powering up in the wrong state. The device will power up into Standby mode after  $V_{CC}$  exceeds the POR trigger level and will power down into Reset mode when  $V_{CC}$  drops below the POR trigger level. This bi-directional POR behavior protects the device against 'brown-out' failure following a temporary loss of power.

## Pin Description

**SCL:** The Serial Clock input pin accepts the clock signal generated by the Master.

**SDA:** The Serial Data I/O pin accepts input data and delivers output data. In transmit mode, this pin is open drain. Data is acquired on the positive edge, and is delivered on the negative edge of SCL.

## Functional Description

The CAT24C64BC4/CAT24C64BAC4 supports the Inter-Integrated Circuit ( $I^2C$ ) Bus protocol. The protocol relies on the use of a Master device, which provides the clock and directs bus traffic, and Slave devices which execute requests. The CAT24C64BC4/CAT24C64BAC4 operates as a Slave device. Both Master and Slave can transmit or receive, but only the Master can assign those roles.

## $I^2C$ Bus Protocol

The 2-wire  $I^2C$  bus consists of two lines, SCL and SDA, connected to the  $V_{CC}$  supply via pull-up resistors. The

Master provides the clock to the SCL line, and either the Master or the Slaves drive the SDA line. A '0' is transmitted by pulling a line LOW and a '1' by letting it stay HIGH. Data transfer may be initiated only when the bus is not busy (see A.C. Characteristics). During data transfer, SDA must remain stable while SCL is HIGH.

## START/STOP Condition

An SDA transition while SCL is HIGH creates a START or STOP condition (Figure 2). The START consists of a HIGH to LOW SDA transition, while SCL is HIGH. Absent the START, a Slave will not respond to the Master. The STOP completes all commands, and consists of a LOW to HIGH SDA transition, while SCL is HIGH.

## Device Addressing

The Master addresses a Slave by creating a START condition and then broadcasting an 8-bit Slave address (Figure 3). The first 4 bits of the Slave address are set to 1010. The next 3 bits are set to 000 (CAT24C64BC4) or to 100 (CAT24C64BAC4). The last bit, R/W, specifies whether a Read (1) or Write (0) operation is to be performed.

## Acknowledge

During the 9<sup>th</sup> clock cycle following every byte sent to the bus, the transmitter releases the SDA line, allowing the receiver to respond. The receiver then either acknowledges (ACK) by pulling SDA LOW, or does not acknowledge (NoACK) by letting SDA stay HIGH (Figure 4). Bus timing is illustrated in Figure 5.

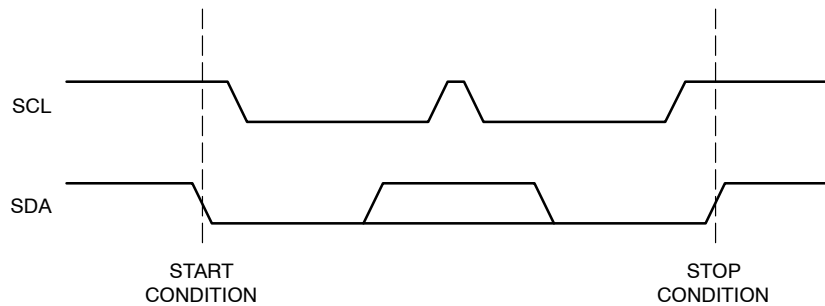


Figure 2. Start/Stop Timing

1	0	1	0	0	0	0	R/W	CAT24C64BC4
1	0	1	0	1	0	0	R/W	CAT24C64BAC4

Figure 3. Slave Address Bits

## CAT24C64BC4, CAT24C64BAC4

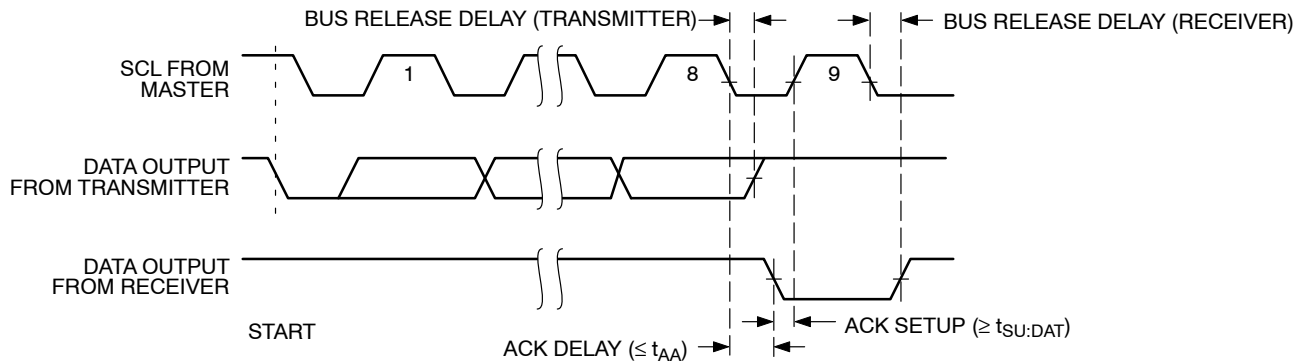


Figure 4. Acknowledge Timing

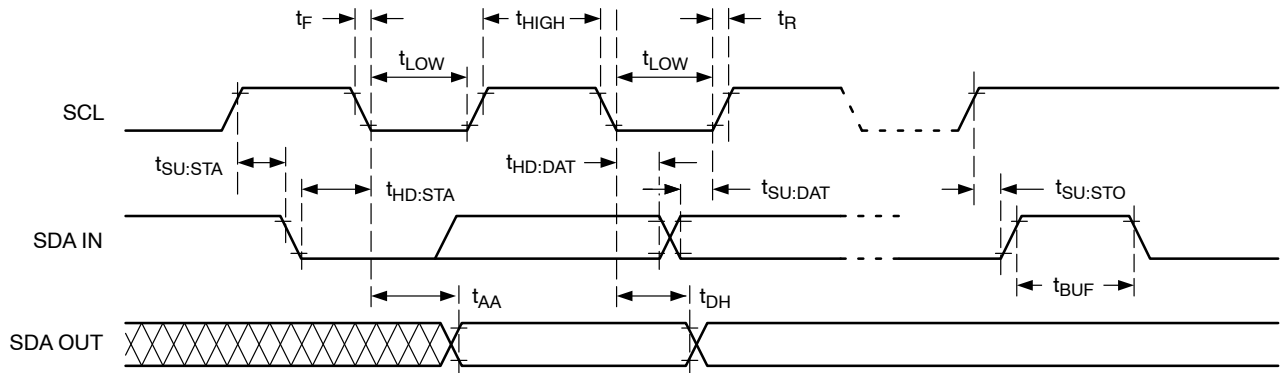


Figure 5. Bus Timing

## WRITE OPERATIONS

### Byte Write

To write data to memory, the Master creates a START condition on the bus and then broadcasts a Slave address with the  $R/\overline{W}$  bit set to '0'. The Master then sends two address bytes and a data byte and concludes the session by creating a STOP condition on the bus. The Slave responds with ACK after every byte sent by the Master (Figure 6). The STOP starts the internal Write cycle, and while this operation is in progress ( $t_{WR}$ ), the SDA output is tri-stated and the Slave does not acknowledge the Master (Figure 7).

### Page Write

The Byte Write operation can be expanded to Page Write, by sending more than one data byte to the Slave before issuing the STOP condition (Figure 8). Up to 32 distinct data bytes can be loaded into the internal Page Write Buffer starting at the address provided by the Master. The page address is latched, and as long as the Master keeps sending

data, the internal byte address is incremented up to the end of page, where it then wraps around (within the page). New data can therefore replace data loaded earlier. Following the STOP, data loaded during the Page Write session will be written to memory in a single internal Write cycle ( $t_{WR}$ ).

### Acknowledge Polling

As soon (and as long) as internal Write is in progress, the Slave will not acknowledge the Master. This feature enables the Master to immediately follow-up with a new Read or Write request, rather than wait for the maximum specified Write time ( $t_{WR}$ ) to elapse. Upon receiving a NoACK response from the Slave, the Master simply repeats the request until the Slave responds with ACK.

### Delivery State

The CAT24C64BC4/CAT24C64BAC4 is shipped erased, i.e., all bytes are FFh.

# CAT24C64BC4, CAT24C64BAC4



Figure 6. Byte Write Sequence

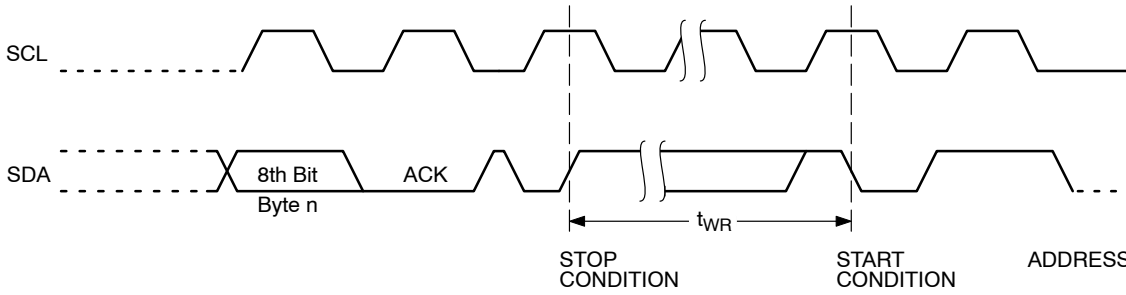


Figure 7. Write Cycle Timing

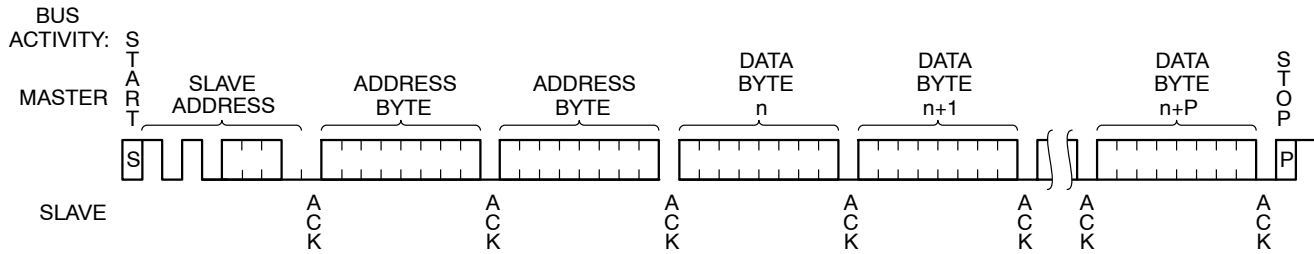


Figure 8. Page Write Sequence

# CAT24C64BC4, CAT24C64BAC4

## READ OPERATIONS

### Immediate Read

To read data from memory, the Master creates a START condition on the bus and then broadcasts a Slave address with the  $R/\overline{W}$  bit set to '1'. The Slave responds with ACK and starts shifting out data residing at the current address. After receiving the data, the Master responds with NoACK and terminates the session by creating a STOP condition on the bus (Figure 9). The Slave then returns to Standby mode.

### Selective Read

To read data residing at a specific address, the selected address must first be loaded into the internal address register. This is done by starting a Byte Write sequence, whereby the Master creates a START condition, then broadcasts a Slave address with the  $R/\overline{W}$  bit set to '0' and then sends two address bytes to the Slave. Rather than completing the Byte

Write sequence by sending data, the Master then creates a START condition and broadcasts a Slave address with the  $R/\overline{W}$  bit set to '1'. The Slave responds with ACK after every byte sent by the Master and then sends out data residing at the selected address. After receiving the data, the Master responds with NoACK and then terminates the session by creating a STOP condition on the bus (Figure 10).

### Sequential Read

If, after receiving data sent by the Slave, the Master responds with ACK, then the Slave will continue transmitting until the Master responds with NoACK followed by STOP (Figure 11). During Sequential Read the internal byte address is automatically incremented up to the end of memory, where it then wraps around to the beginning of memory.

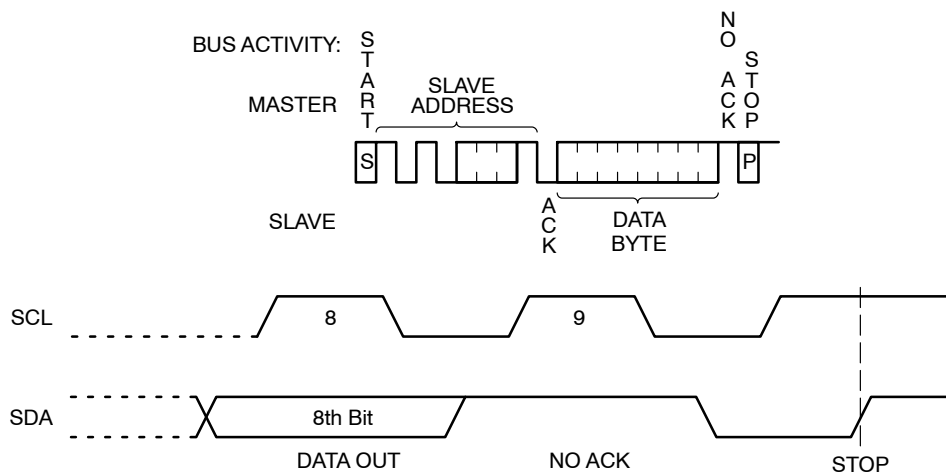


Figure 9. Immediate Read Sequence and Timing

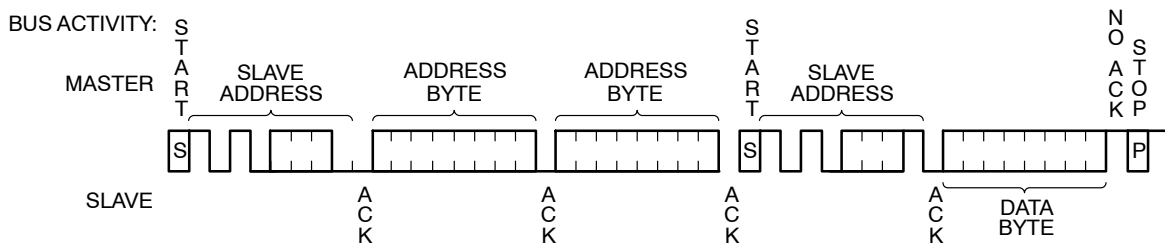


Figure 10. Selective Read Sequence

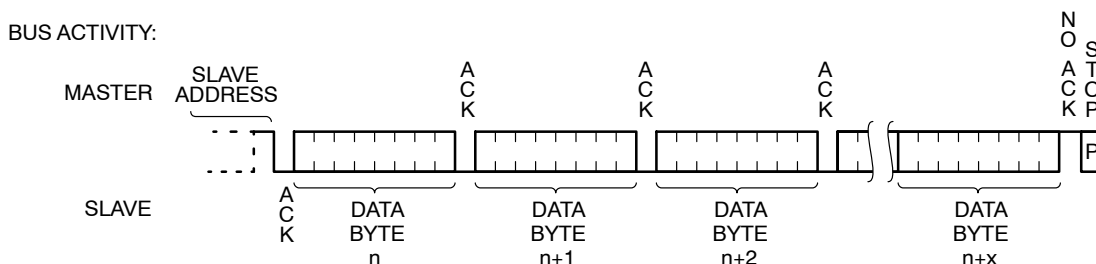


Figure 11. Sequential Read Sequence

## CAT24C64BC4, CAT24C64BAC4

### ORDERING INFORMATION

Device Order Number	Specific Device Marking	Package Type	Temperature Range	Lead Finish	Shipping†
CAT24C64BC4CTR	A	WLCSP-4 with Die Coat	I = Industrial (-40°C to +85°C)	SnAg	Tape & Reel, 5,000 Units / Reel
CAT24C64BAC4CTR (Note 9)	D	WLCSP-4 with Die Coat	I = Industrial (-40°C to +85°C)	SnAg	Tape & Reel, 5,000 Units / Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

8. All packages are RoHS-compliant (Lead-free, Halogen-free).

9. This WLCSP-4 option responds to a different Slave Address compared to CAT24C64BC4CTR.

10. **Caution: The EEPROM devices delivered in WLCSP must never be exposed to ultra violet light. When exposed to ultra violet light the EEPROM cells lose their stored data.**

ON Semiconductor is licensed by the Philips Corporation to carry the I<sup>2</sup>C bus protocol.

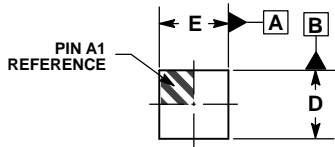




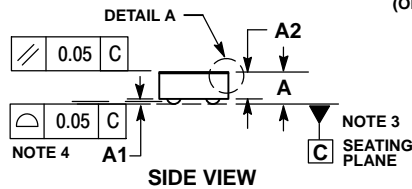
SCALE 4:1

**WLCSP4, 0.77x0.77**  
**CASE 567JY**  
**ISSUE C**

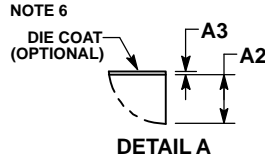
DATE 07 MAR 2017



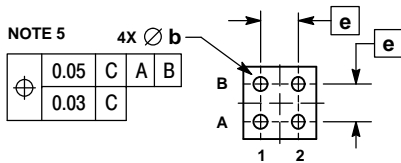
TOP VIEW



SIDE VIEW

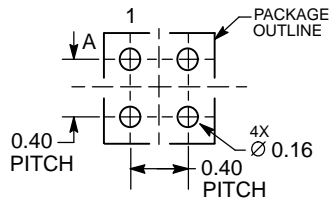


DETAIL A



BOTTOM VIEW

**RECOMMENDED SOLDERING FOOTPRINT\***



DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DATUM C, THE SEATING PLANE, IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
4. COPLANARITY APPLIES TO SPHERICAL CROWNS OF THE SOLDER BALLS.
5. DIMENSION b IS MEASURED AT THE MAXIMUM CONTACT BALL DIAMETER PARALLEL TO DATUM C.
6. BACKSIDE COATING IS OPTIONAL.

MILLIMETERS			
DIM	MIN	NOM	MAX
A	---	---	0.35
A1	0.04	0.06	0.08
A2	0.23 REF		
A3	0.025 REF		
b	0.15	0.155	0.16
D	0.75	0.77	0.79
E	0.75	0.77	0.79
e	0.40 BSC		

**GENERIC MARKING DIAGRAM\***




- X = Specific Device Code
- Y = Year
- W = Work Week

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

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<b>STATUS:</b>	<b>ON SEMICONDUCTOR STANDARD</b>	
<b>NEW STANDARD:</b>		
<b>DESCRIPTION:</b>	<b>WLCSP4, 0.77X0.77</b>	<b>PAGE 1 OF 2</b>



ISSUE	REVISION	DATE
O	RELEASED FOR PRODUCTION. REQ. BY I. MARIANO.	06 MAY 2014
A	CORRECTED DETAIL A AND DIMENSION A1, ADDED NOMINAL VALUES. REQ. BY V. CRACIUNOIU.	23 JUN 2016
B	MODIFIED DIMENSIONS D AND E TO 0.77X0.77. REQ. BY V. CRACIUNOIU.	02 AUG 2016
C	MODIFIED DIMENSIONS A1 AND A2 VALUES. REQ. BY V. CRACIUNOIU.	07 MAR 2017

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