

NSPM1041B

ESD Protection Diode

Features

- Protection for the following IEC Standards:
 - IEC61000-4-2 Level 4: ± 30 kV Contact Discharge
 - IEC61000-4-5 (Lightning) 125 A (8/20 μ s)
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
IEC 61000-4-2 (ESD) Contact Air		± 30 ± 30	kV
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-65 to +150	$^{\circ}$ C
Maximum Peak Pulse Current 8/20 μ s @ $T_A = 25^{\circ}$ C, Pin 2 to Pin 1	I_{PP}	125	A

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.



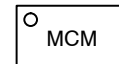
ON Semiconductor[®]

www.onsemi.com



UDFN2
CASE 517DF

MARKING DIAGRAM



MC = Specific Device Code
M = Date Code

ORDERING INFORMATION

Device	Package	Shipping [†]
NSPM1041BMUTBG	UDFN2 (Pb-Free)	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

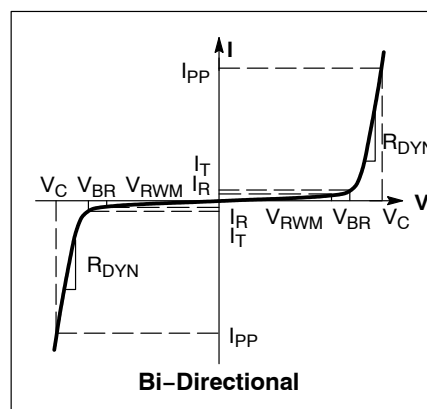
NSPM1041B

ELECTRICAL CHARACTERISTICS

($T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter
I_{PP}	Maximum Reverse Peak Pulse Current
V_C	Clamping Voltage @ I_{PP}
V_{RWM}	Working Peak Reverse Voltage
I_R	Maximum Reverse Leakage Current @ V_{RWM}
V_{BR}	Breakdown Voltage @ I_T
I_T	Test Current

*See Application Note AND8308/D for detailed explanations of datasheet parameters.



ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Reverse Working Voltage	V_{RWM}	Pin 1 to Pin 2			3.3	V
Reverse Working Voltage	V_{RWM}	Pin 2 to Pin 1			4.8	V
Breakdown Voltage	V_{BR}	$I_T = 1\text{ mA}$, Pin 1 to Pin 2	4.5		6.0	V
Breakdown Voltage	V_{BR}	$I_T = 1\text{ mA}$, Pin 2 to Pin 1	4.85		6.0	V
Reverse Leakage Current	I_R	$V_{RWM} = 3.3\text{ V}$, Pin 1 to Pin 2			1.0	μA
Reverse Leakage Current	I_R	$V_{RWM} = 4.8\text{ V}$, Pin 2 to Pin 1			1.0	μA
Clamping Voltage (Note 1)	V_C	$I_{PP} = 1\text{ A}$, $t_p = 8 \times 20\ \mu\text{s}$			5.6	V
Clamping Voltage (Note 1)	V_C	$I_{PP} = 35\text{ A}$, $t_p = 8 \times 20\ \mu\text{s}$			7.2	V
Clamping Voltage (Note 1)	V_C	$I_{PP} = 80\text{ A}$, $t_p = 8 \times 20\ \mu\text{s}$			8.0	V
Clamping Voltage (Note 1)	V_C	$I_{PP} = 125\text{ A}$, $t_p = 8 \times 20\ \mu\text{s}$			10.8	V
Clamping Voltage TLP (Note 2)	V_C	$I_{PP} = 8\text{ A}$ } IEC 61000-4-2 Level 2 equivalent (±4 kV Contact, ±8 kV Air) $I_{PP} = 16\text{ A}$ } IEC 61000-4-2 Level 4 equivalent (±8 kV Contact, ±16 kV Air)		5.6 5.8		V
Dynamic Resistance	R_{DYN}	TLP Pulse, Pin 1 to Pin 2		0.022		Ω
Dynamic Resistance	R_{DYN}	TLP Pulse, Pin 2 to Pin 1		0.018		Ω
Junction Capacitance	C_J	$V_R = 0\text{ V}$, $f = 1\text{ MHz}$			480	pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

- Non-repetitive current pulse at $T_A = 25^\circ\text{C}$, per IEC61000-4-5 waveform.
- ANSI/ESD STM5.5.1 – Electrostatic Discharge Sensitivity Testing using Transmission Line Pulse (TLP) Model.
TLP conditions: $Z_0 = 50\ \Omega$, $t_p = 100\text{ ns}$, $t_r = 4\text{ ns}$, averaging window; $t_1 = 30\text{ ns}$ to $t_2 = 60\text{ ns}$.

NSPM1041B

TYPICAL CHARACTERISTICS

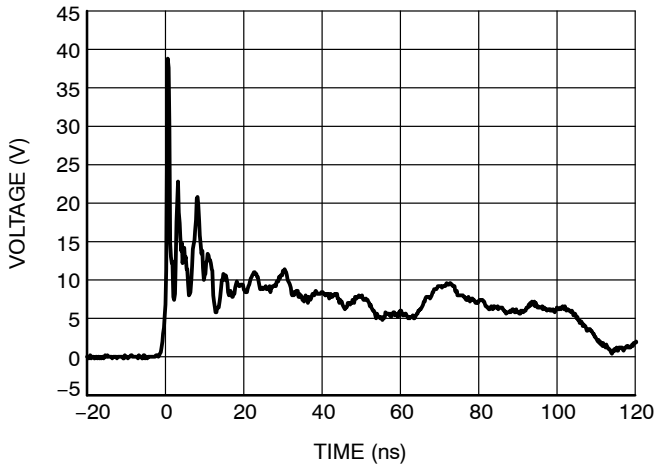


Figure 1. ESD Clamping Voltage Screenshot P2 to P1, 8 kV Contact per IEC61000-4-2

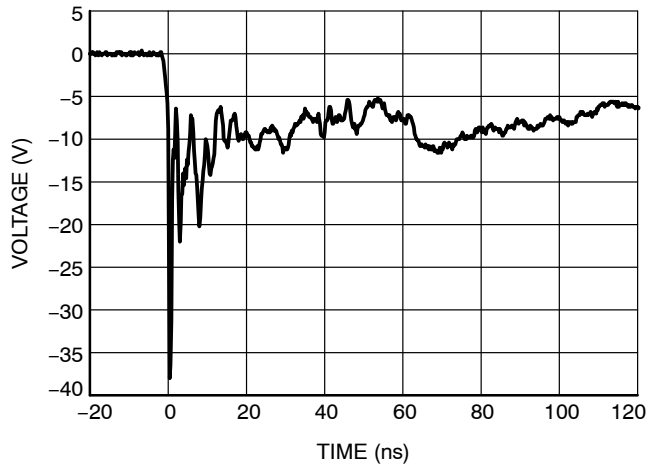


Figure 2. ESD Clamping Voltage Screenshot P1 to P2, 8 kV Contact per IEC61000-4-2

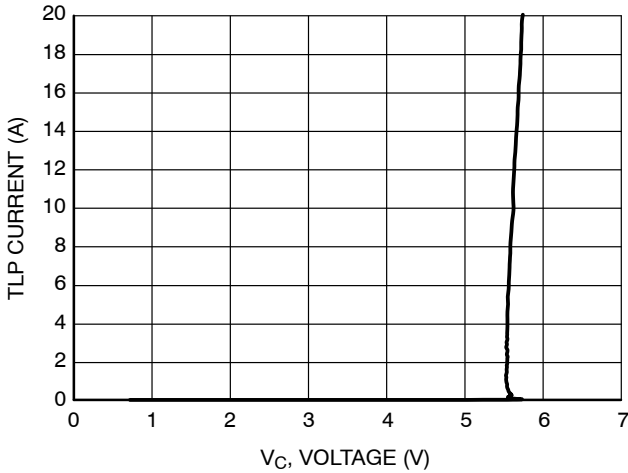


Figure 3. Positive TLP I-V Curve, Pin 2 to Pin 1

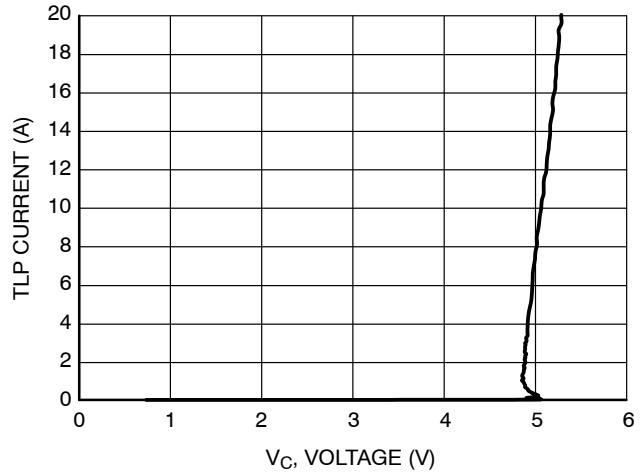


Figure 4. Negative TLP I-V Curve, Pin 1 to Pin 2

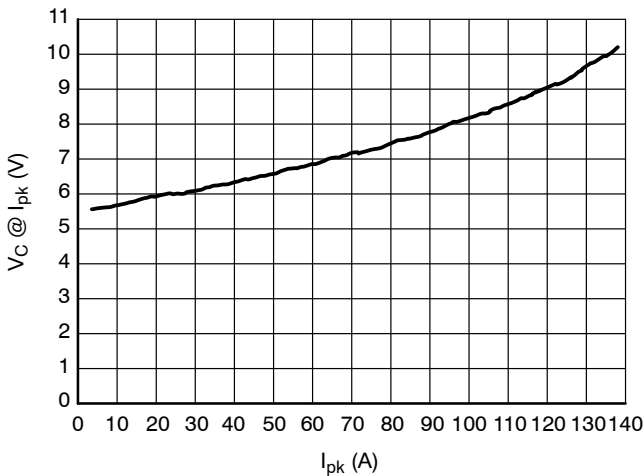


Figure 5. Clamping Voltage vs. Peak Pulse Current ($t_p = 8/20 \mu s$), Pin 2 to Pin 1

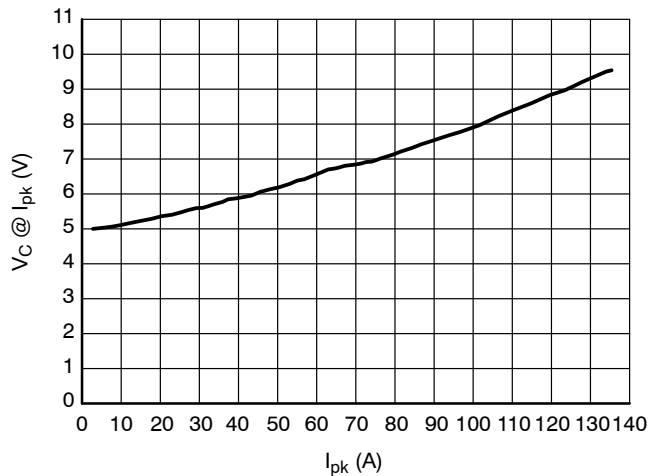


Figure 6. Clamping Voltage vs. Peak Pulse Current ($t_p = 8/20 \mu s$), Pin 1 to Pin 2

NSPM1041B

TYPICAL CHARACTERISTICS

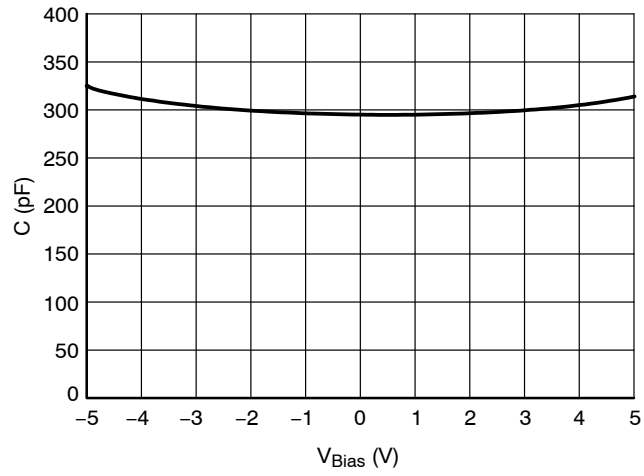


Figure 7. CV Characteristics

Transmission Line Pulse (TLP) Measurement

Transmission Line Pulse (TLP) provides current versus voltage (I-V) curves in which each data point is obtained from a 100 ns long rectangular pulse from a charged transmission line. A simplified schematic of a typical TLP system is shown in Figure 8. TLP I-V curves of ESD protection devices accurately demonstrate the product’s ESD capability because the 10s of amps current levels and under 100 ns time scale match those of an ESD event. This is illustrated in Figure 9 where an 8 kV IEC 61000-4-2 current waveform is compared with TLP current pulses at 8 A and 16 A. A TLP I-V curve shows the voltage at which the device turns on as well as how well the device clamps voltage over a range of current levels. For more information on TLP measurements and how to interpret them please refer to AND9007/D.

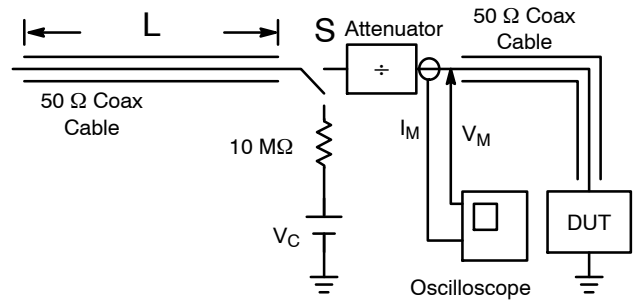


Figure 8. Simplified Schematic of a Typical TLP System

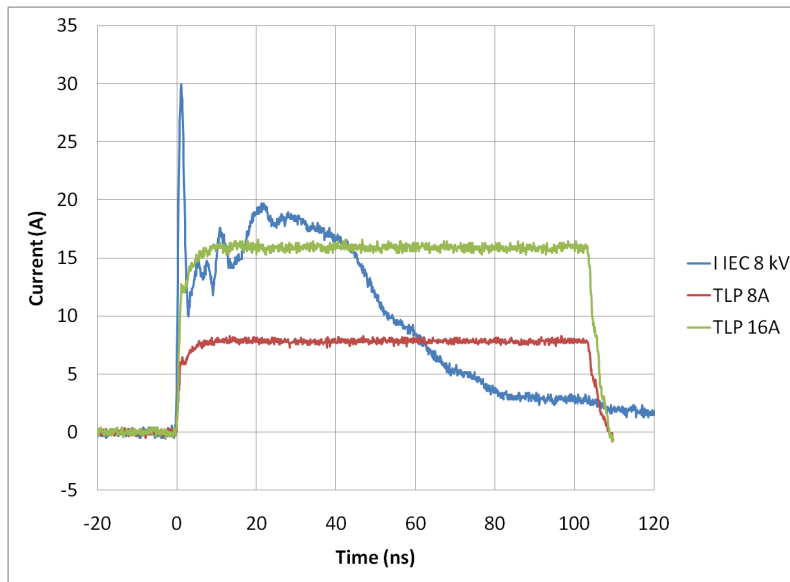


Figure 9. Comparison Between 8 kV IEC 61000-4-2 and 8 A and 16 A TLP Waveforms

NSPM1041B

IEC 61000-4-2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8



Figure 10. IEC61000-4-2 Spec

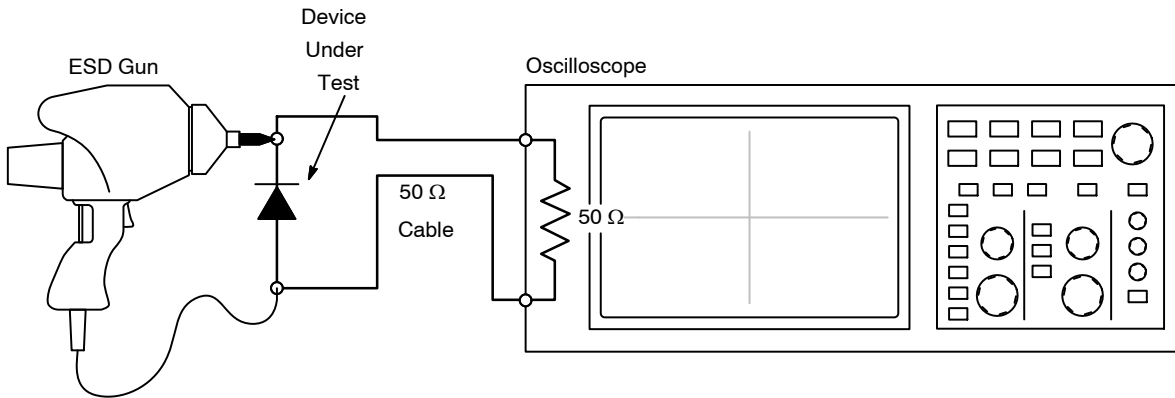


Figure 11. Diagram of ESD Test Setup

ESD Voltage Clamping

For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000-4-2 waveform. Since the IEC61000-4-2 was written as a pass/fail spec for larger systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage

at the device level. ON Semiconductor has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the datasheets for all ESD protection diodes. For more information on how ON Semiconductor creates these screenshots and how to interpret them please refer to AND8307/D.

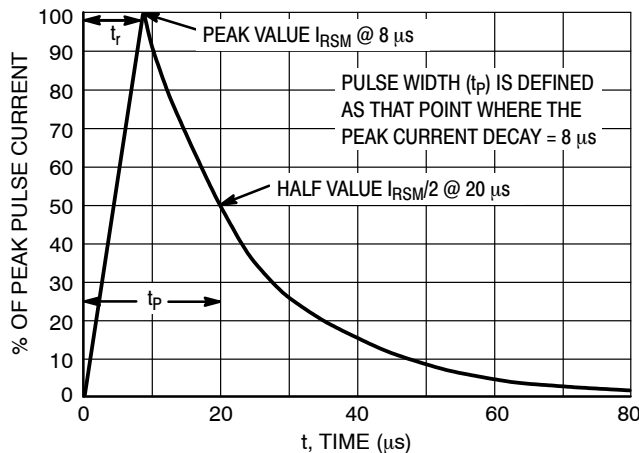


Figure 12. 8 x 20 μs Pulse Waveform

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

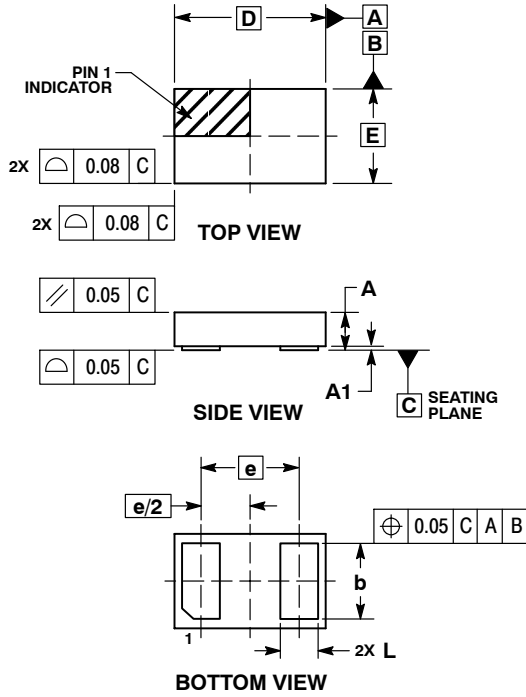
ON Semiconductor®



SCALE 4:1

UDFN2 2.0x1.25, 1.3P
CASE 517DF
ISSUE A

DATE 06 JUL 2016



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.

DIM	MILLIMETERS	
	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
b	0.95	1.05
D	2.00 BSC	
E	1.25 BSC	
e	1.30 BSC	
L	0.45	0.55

GENERIC MARKING DIAGRAMS*

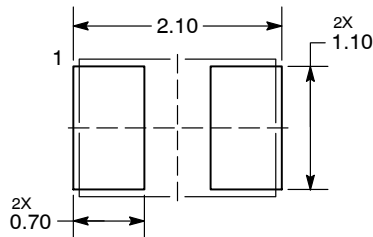


- XX = Specific Device Code
 M = Date Code

- STYLE 1:
 PIN 1. CATHODE (POLARITY BAND)
 2. ANODE
- STYLE 2:
 . NO POLARITY

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G", may or not be present.

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DOCUMENT NUMBER:	98AON04628G	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	UDFN2 2.0X1.25, 1.3P	PAGE 1 OF 1

ON Semiconductor and are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Email Requests to: orderlit@onsemi.com

onsemi Website: www.onsemi.com

TECHNICAL SUPPORT

North American Technical Support:

Voice Mail: 1 800-282-9855 Toll Free USA/Canada

Phone: 011 421 33 790 2910

Europe, Middle East and Africa Technical Support:

Phone: 00421 33 790 2910

For additional information, please contact your local Sales Representative

